Frequency and Phase settling time measurements on PLL circuits

Application Note

Products:

- R&S®FSWP8
- R&S®FSWP26
- R&S®FSWP50

Frequency hopping is one of the most common methods to avoid interference and to increase security. As data throughput is a key parameter for wireless transmission systems, the time for a frequency change or hop is essential. Frequency settling time is therefore a very important measurement for the synthesizer developers.

This application note provides basic information about frequency and phase settling time measurements and how the measurement is implemented inside modern phase noise analyzers.

Measurement examples show the possibilities of this measurement feature and help the user to understand and use this method.

ROHDE&SCHWARZ

Application Note
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1 Introduction

Modern radio communication systems regularly employ frequency-hopping methods to better suppress interference or prevent fading. Since such a frequency hop influences data throughput, the time for it is limited. Quick frequency settling is thus one of the key characteristic.

Up to now, complex test setups have been necessary to determine the settling time of a frequency hop. However, the time pressure on communications systems developers requires an easy and efficient measurement method.

This application note describes different techniques for this measurement. The R&S®FSWP phase noise analyzer performs frequency and phase settling time measurements using a modern wideband concept, and results are obtained easily and convenient with an integrated transient analysis capability.

2 Settling time measurement overview

2.1 Theoretical background of frequency settling time

Frequency settling is typically measured during the development of components for modern communications systems such as mobile phones or radar systems. The measured quantity is the time the circuit needs to hop from one frequency to another frequency. Data transmission can start only after the circuit settles on the new frequency. In most communication systems, the internal frequency oscillators are frequency locked to a common frequency reference via a PLL to ensure frequency accuracy and compliance with timing requirements for frequency hopping.

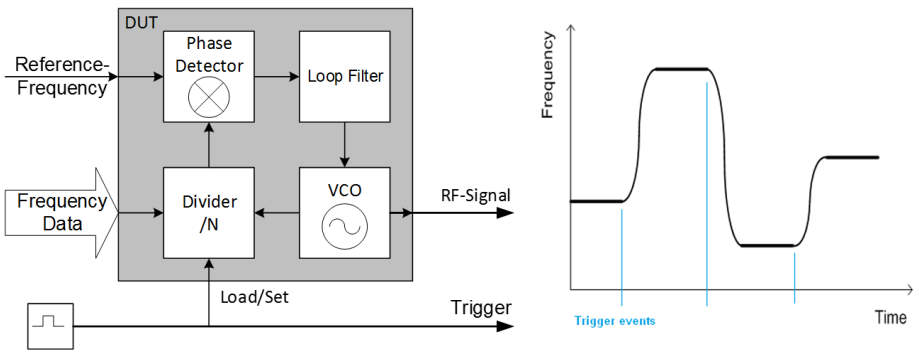

Fig. 2.1-1: Simplified block diagram of a frequency-hopping synthesizer

The characteristics of the PLL determines the phase noise of the entire system. Besides the influence on the phase noise, the loop filter in the PLL has great influence on the amount of time that the system requires for frequency and phase settling after a frequency or channel change.

A certain degree of frequency and phase deviation is acceptable after the hop. This deviation is taken into account to precisely determine the settling time.

Frequency settling measurement in the past

2.2 Frequency settling measurement in the past

Many standards recommend a frequency settling time measurement that is based on a frequency discriminator. The measurement of the settling time is performed on an oscilloscope connected to the video output of the discriminator, since this was the only way to get good resolution and automated measurement functions for timing measurements.

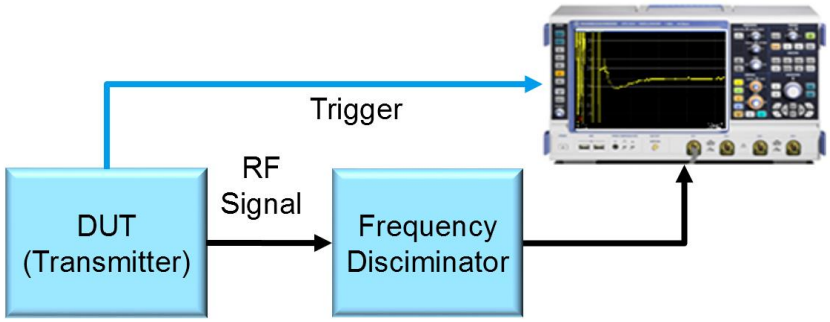

Fig. 2.2-1: Test setup with a Frequency discriminator

The measurement method relies on the availability of a frequency discriminator that fit´s to the RF frequency and bandwidth of the device under test.

2.2.1 Measurement with signal analyzers

As a simple way around the availability of a discriminator, the use of signal analyzers with digital sampling allows broadband measurement of wide frequency ranges. High-speed analog/digital converters (ADC) sample the input signal and save the measurement data (samples) in large memories. The bandwidth and sampling rate of the A/D converters, plus the available memory, determine the acquisition time, possible frequency resolution, and the range over which frequency settling can be measured.

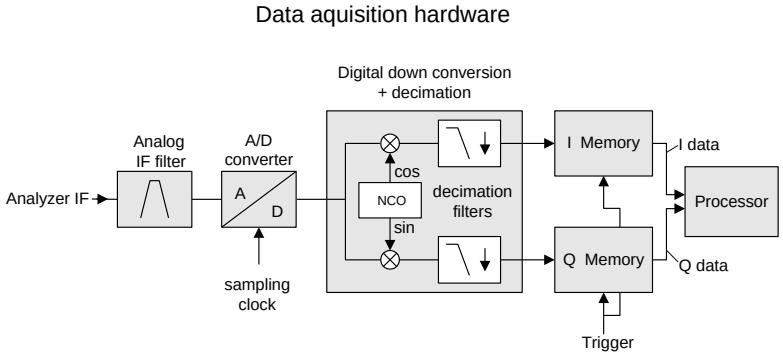

Fig. 2.2-2: Block diagram of the IF digitization in the signal analyzer

Frequency settling measurement in the past

The block diagram shows the implementation of IF sampling in a typical signal analyzer. The analog IF filter limits the IF signal to adhere to the Nyquist theorem. Typical bandwidths are in the range of 10 MHz and up to 2 GHz. The A/D converter samples the analog IF signal. To achieve data rate decimation and reduce the data volume, the sampling output signal is filtered digitally based on the defined bandwidth, thus reducing the sampling rate. The bandwidth determines the time resolution of the subsequent frequency settling measurement. The filtered I/Q samples are stored in memory for further processing. Internal or external trigger signals can be used to control the storage process, and thus optimally adjust the available storage length to the measurement task. The processor in the signal analyzer includes software that handles the entire demodulation process. All calculations are based on the same I/Q data set stored in the measurement data memory.

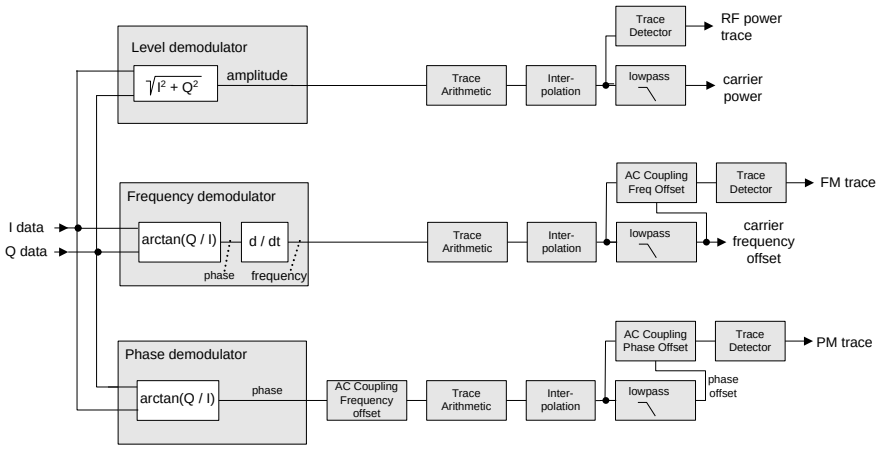

Fig. 2.2-3: Block diagram of the demodulators

The above block diagram shows how the saved measurement data is processed to calculate frequency or phase information. The digital (I/Q) samples contain information about all signals that occur within the recorded spectral range. These samples can be used to calculate the input signal frequency versus time during acquisition time. The outputs of the digital demodulators supply information about frequency, phase, and amplitude versus time. The signal analyzer represents amplitude, phase, and frequency versus time in the form of a measurement trace, and all normal functions such as MaxHold, MinHold, and Averaging are available.

Frequency settling measurements can usually be set up in such a way that the instrument is actuated by a trigger signal that also starts the frequency hop in the DUT. Recording of measurement data is started either directly by the trigger event or, when pre- or post-triggers are used, at an optimized, definable point in time before or after the trigger event occurs.

The strength of this architecture thus lies in the analysis of narrowband signals. It is less suited, however, for frequency-agile applications or for measurements over very large frequency ranges.

3 R&S FSWP Phase Noise Analyzer

Modern phase noise analyzers are not only able to measure phase noise with excellent performance; they also offer a transient analysis function that enables them to measure frequency and phase settling time.

The R&S®FSWP Phase noise analyzer uses a signal analyzer concept based on digital signal processing techniques. The functional units used for the phase noise measurement allow frequency and phase demodulation and show frequency or phase variations over time. The advantage of this new design lies in the direct sampling of the IF and the digital conversion to the baseband (digital I/Q signals). The baseband data thus obtained allows measurements with maximum precision. The digital implementation of the demodulators makes modulation errors and drift negligible. The only sources of error that remain are the characteristics of the analog signal path in front of the A/D converter.

The use of a frequency divider that is available as part of the phase noise analyzer hardware increases the frequency transient measurement to a much wider bandwidth and thus captures signal transients with up to 8 GHz wide frequency hops.

In addition, the R&S®FSWP offers a real-time frequency demodulator and trigger circuit to identify the transition across a defined trigger frequency to start the measurement. This is a very helpful feature for frequency hopping or phase settling time measurements, as a trigger signal that marks the frequency change is often not available from the device under test.

3.1 Phase noise analyzer architecture

The use of signal analyzers allows broadband measurement over wide frequency ranges. This is a better approach for measuring frequency and phase settling than the use of a signal analyzer or FM discriminator. High-speed analog digital (A/D) converters sample the input signal and the measurement data (samples) is then processed in real-time hardware to determine the frequency and level variations of the input signal. The bandwidth and sampling rate of the A/D converters determine the input frequency range over which the frequency settling can be measured.

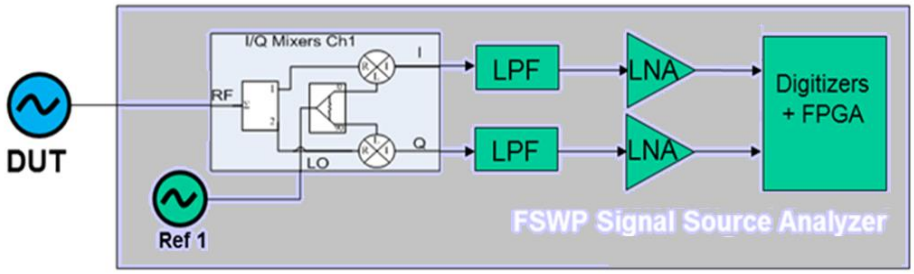

Fig. 3.1-1: Block diagram of the IF digitization in the signal analyzer

Phase noise analyzer architecture

The implementation of IF sampling in the R&S®FSWP phase noise analyzer in its narrowband transient mode (Span setting < 40 MHz) is shown in the above block diagram. The analog I/Q mixer uses an extremely low noise internal reference oscillator and shifts the RF input signal to a low IF frequency. The I/Q mixer outputs are fed to a very low-noise amplifier and then into 100 Ms/s A/D-converters (ADC). The outputs of the ADCs are then fed to an FPGA and digital signal processing is performed in real time.

The signals from the I and Q digitizers are next equalized and fed to a digital down converter that provides an I-Q data stream for subsequent signal processing. The digital down converter provides precise I and Q signals that are not corrupted by common I/Q demodulator impairments such as I/Q imbalance and quadrature errors.

To achieve data rate decimation and reduce the data volume, the sampling output signal is digitally filtered based on the defined bandwidth, thus reducing the sampling rate. The bandwidth determines the time resolution of the subsequent frequency settling measurement. Unnecessary oversampling should be avoided, as this significantly increases noise during the measurement and increases the time required for calculations. Internal or external trigger signals can be used to control the measurement process, and thus optimally adjust the available measurement time to the task.

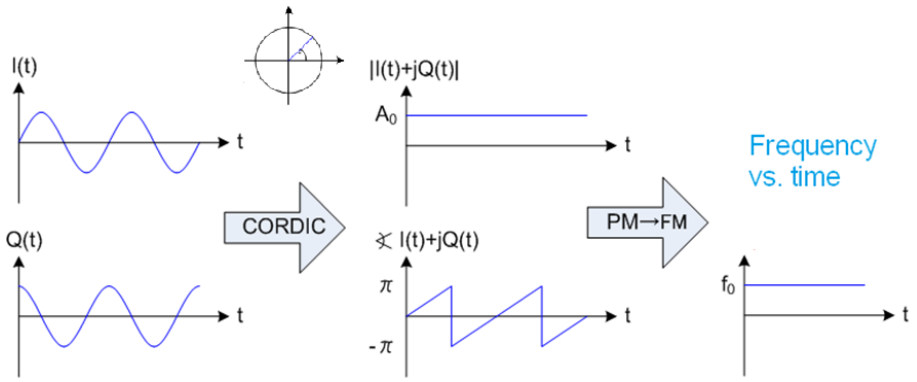

Fig. 3.1-2: Block diagram of the demodulators

The above block diagram shows the processing of I/Q measurement data to calculate frequency and phase information. The digital (I/Q) samples are converted into phase and amplitude versus time data, in the next step the frequency information is derived from the phase data.

While the phase noise analyzer normally uses a FFT to convert the level and frequency information into the phase noise and amplitude noise results, the raw frequency and phase data versus time can be used in the transient mode in the form of a measurement trace to measure frequency and phase settling.

The analog I/Q-mixer together with the 100 Ms/s ADC limits the analyzer's bandwidth to 40 MHz to fulfill to the Nyquist theorem.

Typical test setup for settling time measurements

3.1.1 Measurement with wide bandwidth

A special wide band signal path in the R&S®FSWP Phase Noise analyzer includes a RF frequency divider.

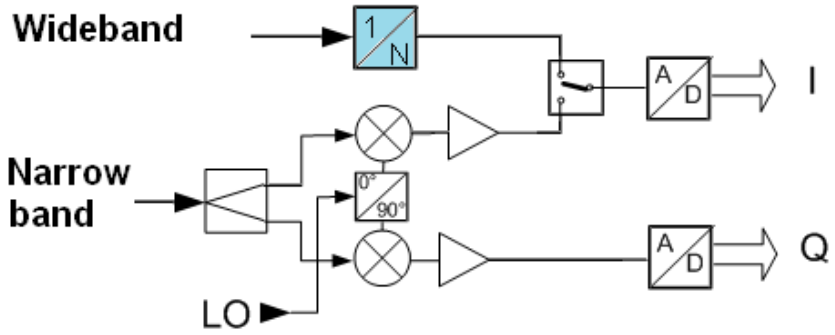

Fig. 3.1-3: Block diagram of the R&S®FSWP wideband mode

In the wideband transient mode (Span setting > 40 MHz) the input signal frequency range from 256 MHz to 8 GHz is divided by 256 in a first step, and the output signal from the divider (1 MHz to 31.25 MHz) is then sampled and converted to perform the digital I/Q signal processing as in the narrowband mode.

3.2 Typical test setup for settling time measurements

Most designs use a programmable divider in the PLL to set the frequency. The following block circuit shows the typical test setup for measuring frequency settling on a PLL-controlled oscillator:

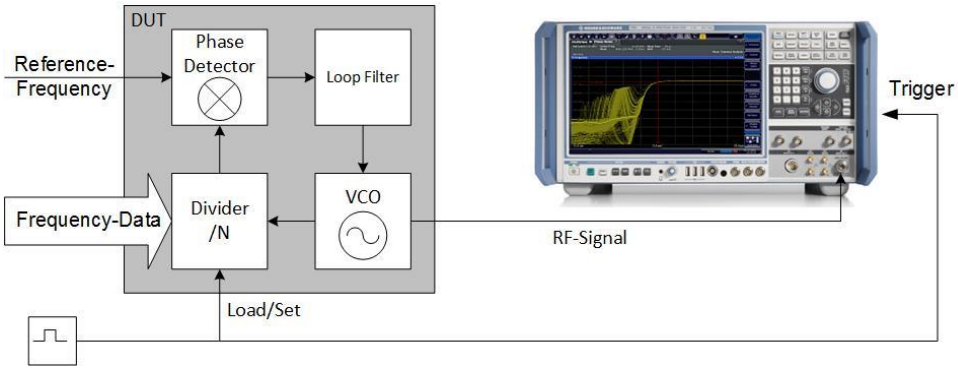

Fig. 3.2-1: Setup for measuring frequency settling on a synthesizer

The programming signal for loading the frequency divider is used directly as a trigger signal for the analyzer. It marks the start of the frequency hop. The analyzer starts to

Typical test setup for settling time measurements

record the measurement data with the trigger event. Pre- or post-triggers can be used to adjust the start of the recording so that frequency versus time can also be observed before the hop, for example. After the measurement data is recorded, it is used to calculate and display amplitude, frequency, or phase versus time.

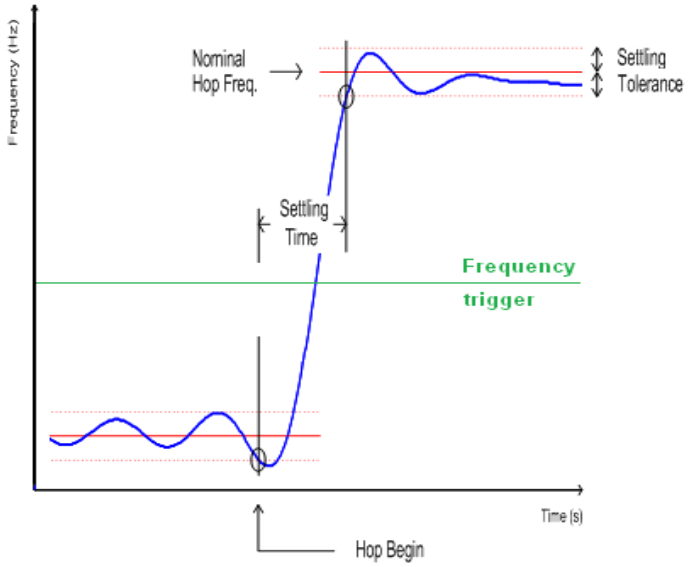

Fig. 3.2-2: Frequency trigger and timing measurements on a hopping signal

In case of the R&S®FSWP phase noise analyzer the measurement can also be triggered by the signal frequency itself. The instrument monitors the output signal of the frequency demodulator and includes a trigger circuit to identify the transition across a defined trigger (frequency) to start the measurement. This feature allows the hopping time measurement for signals that do not allow accessing the trigger inside of the circuits of the device under test.

4 Frequency hopping and settling time measurements in practice

The previous chapters describes the fundamentals of frequency hopping and the requirements for practical measurements on these signals. This section describes the use of the R&S®FSWP phase noise analyzer to perform measurements on frequency hopping signals and show the capabilities in RF test scenarios.

4.1 Trigger on wideband frequency hopping signals

To verify the performance of a frequency hopping signal it is necessary to trigger the measurement instrument on the signal hop of interest. In many cases, the RF circuit design does not offer a trigger signal connection of the device under test.

The R&S®FSWP offers the possibility to trigger the measurement on the frequency transition through a defined trigger position (trigger frequency). Whenever the signal frequency passes this threshold, the R&S®FSWP triggers and records the frequency versus time information.

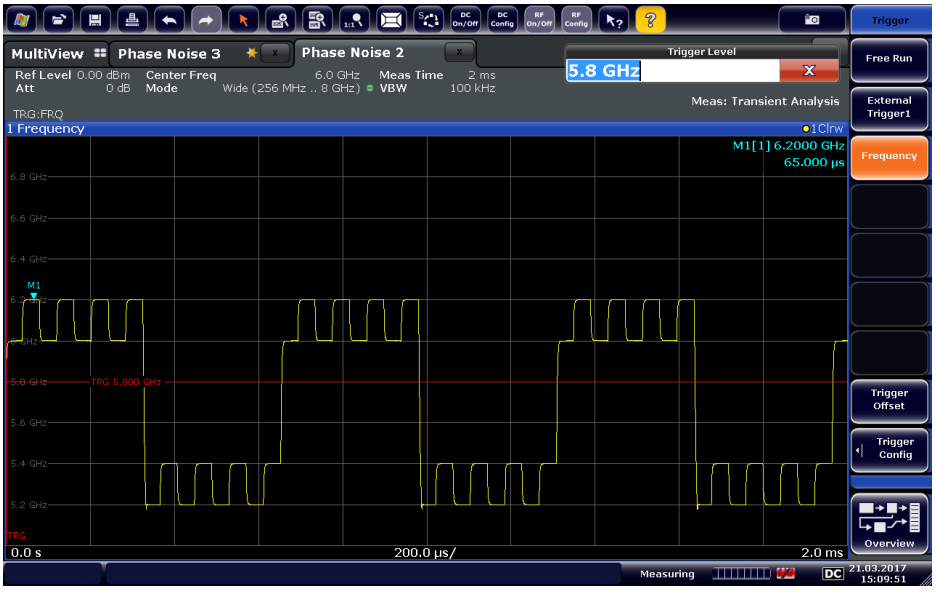

Fig. 4.1-1: Frequency Trigger with the R&S®FSWP phase noise analyzer

In this example, the oscillator generates wideband frequency hops with 200 and 800 MHz hop width. The phase noise analyzer is set to the wideband mode (with 2 GHz span on the screen) and monitors the full frequency range from 256 MHz to 8 GHz, and triggers when the signal frequency passes the trigger level that is set to 5800 MHz. Markers permit readings of measured values at any time position. All measurement values are, of course, also available via remote operation.

Frequency and phase settling time measurement

In the next example, the same signal is measured in the narrowband mode to get a more detailed view about the frequency settling process. In this case, the frequency trigger is set close to the highest frequency of 6200 MHz (see the marker position in the previous measurement).

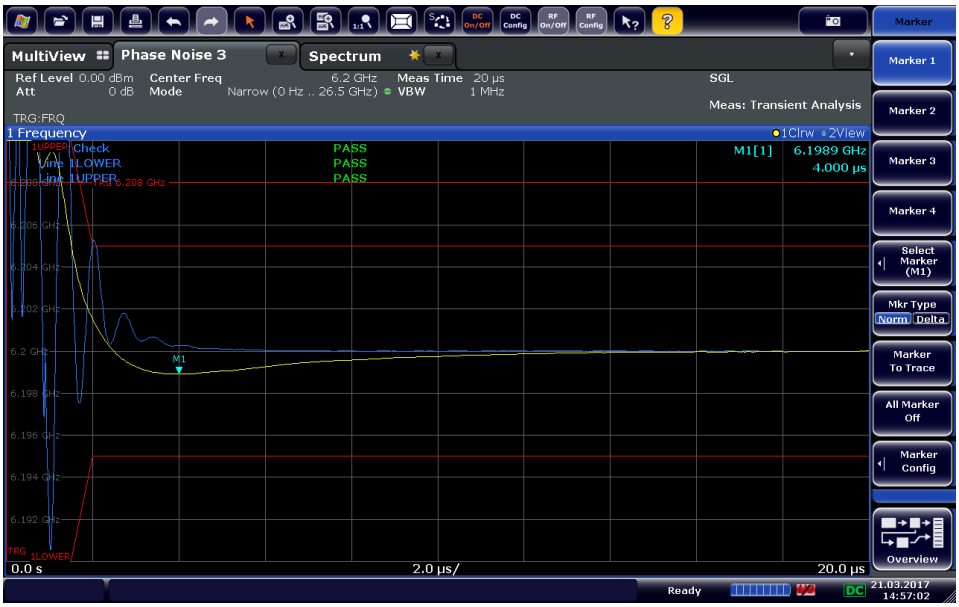

Fig. 4.1-2: Frequency settling time measurement with active limit verification

The specification for this DUT defines a maximum settling time of 2 us. Limit lines are used to observe these limits. The phase noise analyzer automatically monitors compliance with the limit values and outputs them as PASS/FAIL indication. As explained in the previous sections, the loop bandwidth of the PLL circuit is one of the main part that defines the settling time. To visualize the influence of the PLL loop bandwidth, the device under test was modified to create different frequency settling results. Trace 1 (yellow) in the above screen shot shows a slow but smooth settling with a small overshoot, while trace 2 (blue) was using a higher bandwidth and thus settles faster. The R&S®FSWP offers the possibility to check the measured data against a predefined limit line. In the above plot the limit verification indicates that the oscillator passes it´s requirement and reaches the target frequency after about 2 us, and then settles into the target frequency after about 10 us.

4.2 Frequency and phase settling time measurement

In the previous examples, all measurements were performed with the frequency trigger function of the R&S®FSWP. In this case, the measurement starts when the actual frequency of the DUT is already changing to a new value.

In many cases the designer of a synthesizer needs to know the absolute time between the frequency settling command and the real output of the DUT. In this case the programming signal for the frequency divider must be used directly as a trigger signal for the analyzer as it marks the start of the frequency change.

Frequency and phase settling time measurement

Another important parameter of the settling time for a frequency hopping PLL is the phase settling of the RF signal. This is especially true for RF communication systems that use phase modulation, as the settling of the phase has a direct impact on the modulation quality.

Fig. 4.2-1: Frequency and phase settling time measurement in parallel

In the above screen shot, the DUT is programmed to hop to a target frequency of 6000 MHz. The phase noise analyzer measures the frequency versus time in the upper screen, while the phase versus time is displayed in the lower screen. The frequency settling process seems to be almost finished within 10 us, the phase gives a more detailed view that can reveal behavior that is not visible with any other type of view. As long as the frequency is not completely settled, the RF phase vector will rotate and the phase versus time display covers the full range from -180 to +180 degree. This effect is very typical for PLL circuits with large capacitors in the loop filter that need to be charged for the fully phase locked position of the oscillator.

The effect of this phase rotation may have an influence on the earliest point in time when the data transmission can reliably start. In a QPSK design, the symbol points are spaced 90 degrees apart, and there is a tolerance of no more one-half the distance between any two quadrature points or 45 degrees. It is important to know about the presence of the phase drift that can only be seen in the phase-versus time analysis.

Since the phase noise analyzer starts to capture the incoming signal at a random point in time after the trigger event, the phase of the sampled signal may vary from measurement to measurement. To get a stable phase settling time measurement a point in time needs to be defined that represents zero phase deviation in the result. On a phase settling measurement, this will usually be the point when the phase settling is expected to be finalized. This allows a direct measurement of the phase deviation relative to this point using a marker on the displayed trace data.

4.3 Finding glitches in settling time measurement

In the previous examples, all measurements are performed on a single frequency hop, with the measurement results concentrating on the final part of the frequency or phase settling phase. For frequency hopping systems it is also important to monitor the frequency transition between the hop frequencies. The output signal of a PLL based synthesizer might differ significantly over different hops or time. It is therefore often important to monitor many hops and overlay the time-correlated views of the frequency settling in one screen.

The R&S®FSWP offers a special trace mode called persistence that allows overlying indefinite amounts of measurement traces in one screen. In this mode, the actual measured trace is written in deep color saturation, while older traces fade out from the screen with a defined persistence time.

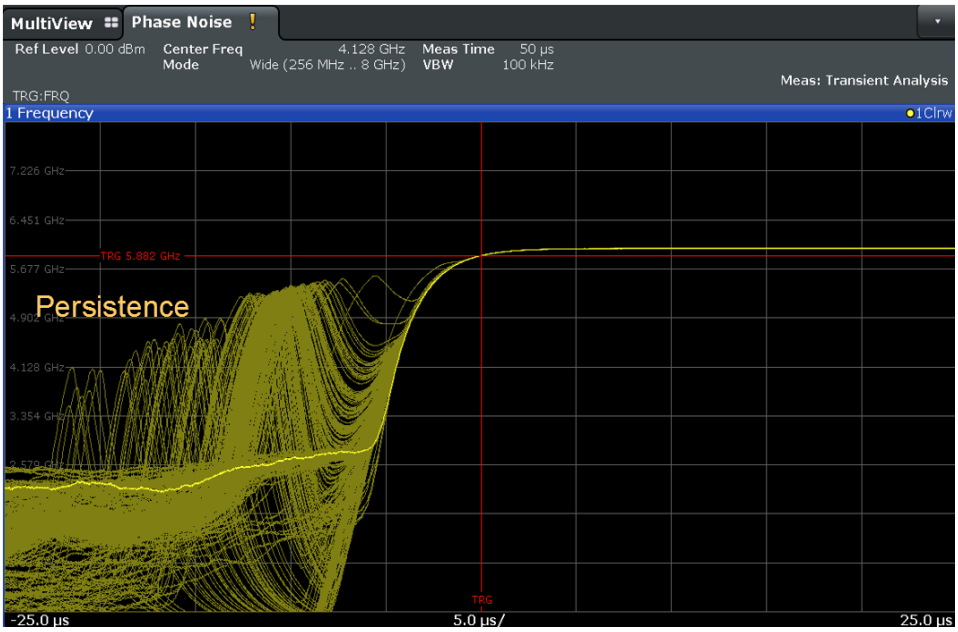

Fig. 4.3-1: Finding glitches in the frequency settling time measurement

The above screen shot shows an example of the persistence trace measuring the frequency settling of a synthesizer. The measurement triggers on the real-time frequency trigger to start and capture the settling of the frequency. The trigger uses a trigger offset of 25 us to monitor the time before the frequency settles to the final value.

In the above example we see that there are events where the frequency is ringing heavily before settling to the final value. In the normal trace mode, it would be very hard to identify these bumps as the user would have to stop the measurement manually once such a result is visible on the screen. Persistence mode keeps these events on the screen for a defined amount of time before they fade out.

The persistence view is extremely helpful to find intermittent problems or rare events of a frequency settling measurement, as it makes short glitches visible even if subsequent trigger events would overwrite them in the normal clear/write trace mode.

5 Conclusion

Frequency settling time measurements were very complex with some traditional methods. For example, the resolution filter must be calibrated if it is to be used as a demodulator. The measurement range is significantly limited, and accuracy is very difficult to assess.

The new generation of Phase Noise analyzers like the R&S®FSWP perform the measurement of settling procedures with less effort and provide rapid results. In addition to measuring frequency-settling time, modern Phase Noise analyzers also record phase settling time – a very important measurement for phase-modulated transmission methods and one that is extremely difficult to perform using conventional methods.

Because of the digital architecture, no calibration is required; the measurement is carried out immediately, with extremely high accuracy and resolution. Modern Phase Noise analyzers help developers to obtain more measurement data quicker, thus allowing them to complete their tasks faster.

6 Literature

[1] R&S®FSWP Phase Noise Analyzer and VCO Tester – Product Brochure

[2] R&S®FSWP Phase Noise Analyzer – Data Sheet

[3] Application Note 1EF94, Pulsed Phase Noise Measurements

7 Ordering Information

Designation	Type	**Order Nr**
Phase Noise Analyzer, 1 MHz to 8 GHz	R&S®FSWP8	1322.8003.08
Phase Noise Analyzer, 1 MHz to 26.5 GHz	R&S®FSWP26	1322.8003.26
Phase Noise Analyzer, 1 MHz to 50 GHz	R&S®FSWP50	1322.8003.50

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