Application Note

SETTLING TIME MEASUREMENTS WITH SIGNAL ANALYZERS

Products:

- R&S®FSxx-K7
- R&S®FSW
- R&S®FSWP
- R&S®FSPN
- R&S®FSMR3000
- R&S®FSVA3000
- R&S®FSV3000
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1 Overview

Accurate frequency and timing are very important characteristics in wireless communication systems. In most applications PLL circuits are used to lock the system frequency to a reference. The PLL characteristics not only will define the overall system performance like phase noise, but are the key part that defines the settling time needed to lock the frequency and phase after a frequency change. The settling time is the time interval the PLL needs to lock the local oscillator from one frequency to another. The definition of the settling period also requires knowledge about the acceptable tolerance in frequency and phase.

This application note provides basic information about settling time measurements and describes how frequency settling time measurements can be easily and convenient performed using a modern spectrum analyzer with integrated signal analysis capabilities.

The analog demodulation measurement application R&S®FSxx-K7 performs frequency and phase settling time measurements using a modern wideband concept, and results are obtained easily and convenient with an integrated settling time measurement capability.

2 Signal analyzer architecture

The digital signal processing in modern signal analyzers is used to offer digital IF filters, but this capability is also ideally suited to measure frequency or phase settling time.

High-speed analog/digital converters (ADC) sample the input signal and save the measurement data (samples) in large memories. The bandwidth and sampling rate of the A/D converters, plus the available memory, determine the acquisition time, possible frequency resolution, and the range over which frequency settling can be measured.

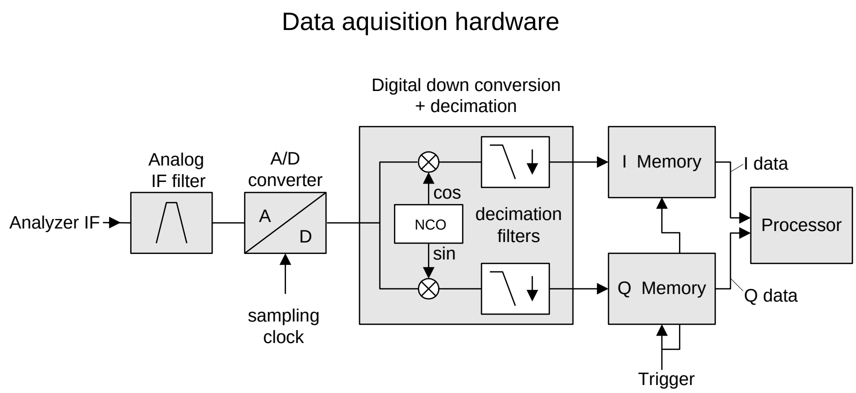

Fig.1: Block diagram of the IF digitization in the signal analyzer

The block diagram shows the implementation of IF sampling in a typical signal analyzer. The analog IF filter limits the IF signal to adhere to the Nyquist theorem. Typical bandwidths are in the range of 10 MHz to 8 GHz. The A/D converter samples the analog IF signal. To achieve data rate decimation and reduce the data volume, the sampling output signal is filtered digitally based on the defined bandwidth, thus reducing the sampling rate. The filtered I/Q samples are stored in memory for further processing.

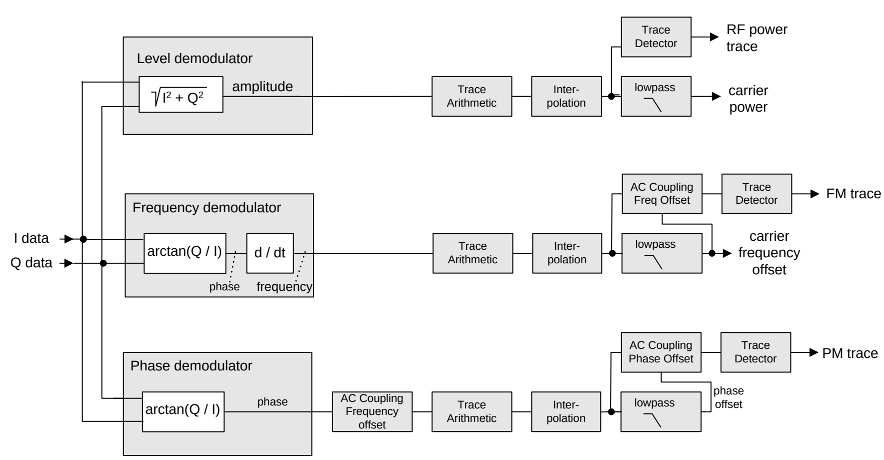

Fig. 2: Block diagram of the demodulators

The above block diagram shows how the saved measurement data is processed to calculate frequency or phase information. The digital (I/Q) samples contain information about all signals that occur within the recorded spectral range. These samples can be used to calculate the input signal frequency versus time during acquisition time. The signal analyzer displays amplitude, phase, and frequency versus time in the form of a measurement trace.

3 Settling time measurement overview

3.1 Theoretical background of settling time

Frequency settling is typically measured during the development of components for modern communication systems such as mobile phones or radar systems. In most communication systems, the internal frequency oscillators are frequency locked to a common frequency reference via a PLL to ensure frequency accuracy and compliance with timing requirements for frequency changes. Most designs use a programmable divider in the PLL to set the frequency. The characteristics of the PLL determines the phase noise of the entire system. Besides the influence on the phase noise, the loop filter in the PLL has great influence on the amount of time that the system requires for frequency and phase settling after a frequency or channel change.

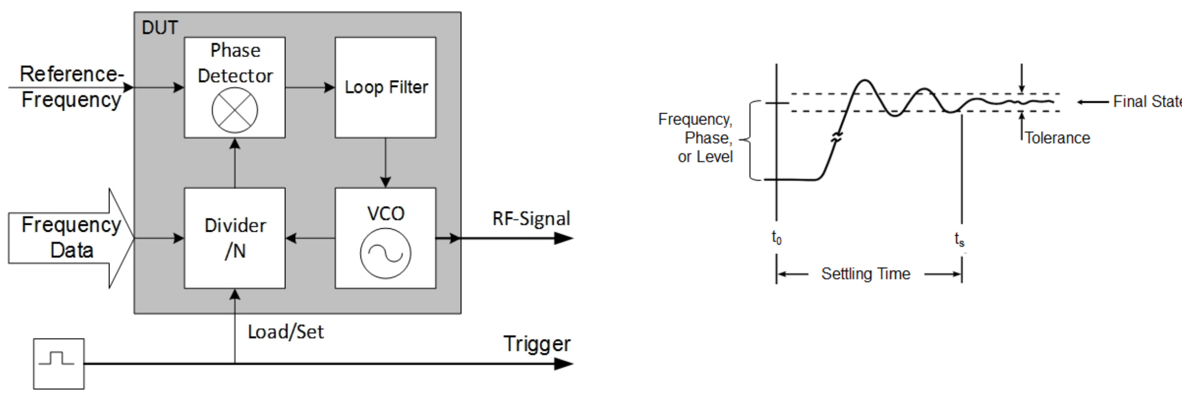

Fig. 3: Simplified block diagram and definition for measuring settling time on a synthesizer

The block circuit shows the typical DUT setup for measuring settling time on a PLL-controlled oscillator.

Frequency settling measurements can usually be set up in such a way that the instrument is actuated by a trigger signal that also starts the frequency settling in the DUT. Recording of measurement data is started either directly by the trigger event or, when pre- or post-triggers are used, at an optimized, definable point in time before or after the trigger event occurs.

The programming signal for loading the frequency divider is used directly as a trigger signal for the analyzer. It marks the start of the measurement. The analyzer starts to record the measurement data with the trigger event. Pre-Trigger can be used to adjust the start of the recording so that frequency versus time can also be observed before the frequency change, for example. After the measurement data is recorded, it is used to calculate and display amplitude, frequency, or phase versus time.

In case of a typical radio where the signal is only enabled in the transmit phase the measurement can also be triggered by the signal power. The RF power trigger starts the measurement in the spectrum analyzer. This feature allows the frequency settling time measurements for signals that do not allow accessing the trigger inside of the circuit of the device under test.

4 Settling time measurements in practice

The previous chapters describe the fundamentals of frequency settling and the concept of the signal and spectrum analyzer. This section describes the use of the R&S®FSxx-K7 analog modulation analysis function to perform these measurements.

4.1 Measuring the Frequency Settling Time of Synthesizers

This measurement would previously have been done using a modulation analyzer as FM discriminator. This setup however requires an extra external oscilloscope to record the frequency transient. Using the spectrum analyzer equipped with R&S®FSxx-K7 analog demodulation no separate scope is needed. This also eliminates the need to calibrate the vertical scaling for kHz/Div.

An external trigger is most appropriate for measuring frequency transients. This can be either a trigger used to initiate a frequency step in the synthesizer under test, or a trigger from the synthesizer's circuitry such as a strobe signal. In this example the setup as shown in the block diagram is used to demonstrate the measurement, using a trigger signal from the DUT. Before connecting the DUT make sure that the maximum power at the analyzer's input is below 30 dBm. For very precise frequency settling measurements and for phase settling measurements the reference from the DUT shall be connected to the analyzer (not shown here).

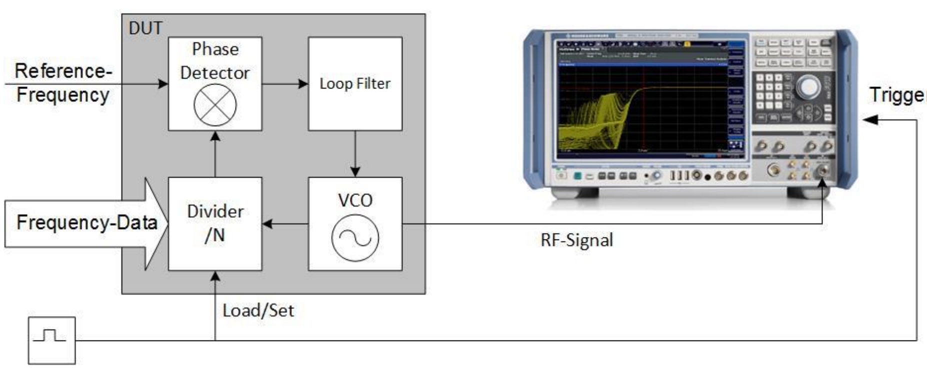

Fig. 4: Test setup for measuring settling time on a synthesizer

The following steps are performed to prepare the measurement:

Bring the analyzer to a predefined state: PRESET

Start the analog demodulation application: MODE: ANALOG DEMOD

Set reference level according to the source level (e.g. 0 dBm): AMPT - REF LEVEL 0 dBm

Set the analyzer to the frequency the DUT is settling to: FREQUENCY xxxx.xx MHz

Select external trigger as trigger source TRIGGER: EXTERNAL

Select DC coupling of the demodulator: MEAS CONFIG: DEMOD CONFIG: AF COUPLING DC

Adjust the vertical scaling to match the resolution needed: AMPT: RANGE: Y PER DIV xxx MHz

The next steps are to select the best measurement bandwidth and the measurement time.

4.1.1 Demodulation bandwidth setting

The analog demodulator uses digital filters determine the demodulation bandwidth. The default demodulation bandwidth setting is a channel filter which is distortion-free with regard to phase and amplitude. Due to the filter design these types of filters will generate some ringing or overshoot in case of a transient signal. For the settling measurement it is recommended to change the filter mode to the gaussian shaped filters as used in the spectrum analyzer mode as these filters are optimized for settling.

Set the bandwidth filter to gaussian: BW: BANDWIDTH CONFIG - Demodulation Filter GAUSS

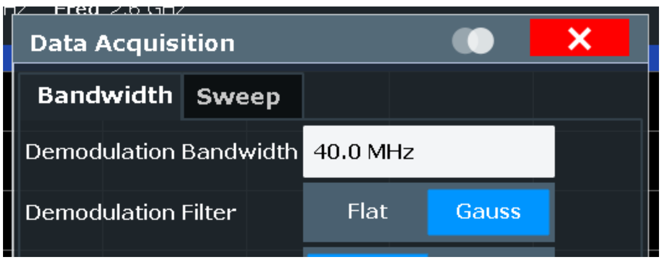

Fig. 5: Demodulation bandwidth setting dialog

The maximum frequency deviation which can be measured is half of the demodulation bandwidth, which also influences the demodulator inherent settling time. The inherent settling time is inversely proportional to the demodulation bandwidth and additionally dependent on the AF lowpass filter.

The demodulation bandwidth must fulfil the following requirements:

- ► Wide enough that the inherent settling time does not influence the settling time to be measured (DBW ≥ 1/settling time is a good starting point)
- ► DBW must be set low enough so that the noise in the frequency versus time plot is well below the defined deviation when ‘settled’.

In general, the demodulation bandwidth should be as narrow as possible to improve the S/N ratio. The residual FM caused by noise floor and phase noise increases dramatically with the bandwidth. The optimum DBW value may have to be determined by experimentation

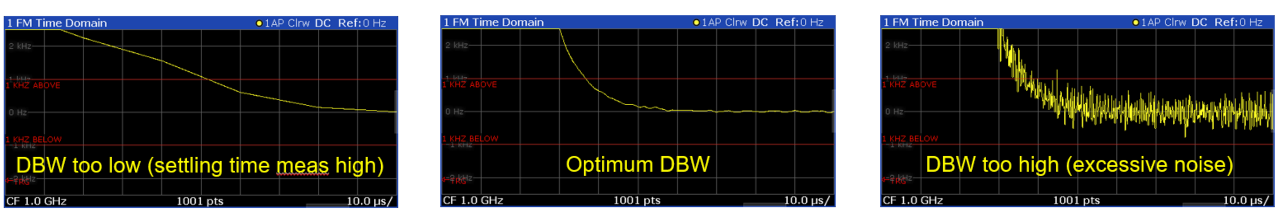

Fig. 6: Demodulation bandwidth setting examples

To reduce the residual FM the analog measurement demodulation offers low pass filters to reduce the bandwidth after the demodulation process. Although the influence of the filter LP 25 % (of the DEMOD BW) on the inherent settling time can be ignored, it reduces the residual FM by a factor of 2. The LP 10 % reduces the residual FM by a factor of 4, increasing the inherent settling time by a factor of approximately 2. Besides the noise reduction and the inherent settling time of the low pass filter, a small amount of ringing or overshoot from these filters will occur that must be considered in the filter bandwidth selection.

4.1.2 Measurement time and vertical scale settings

Settling time is defined as the interval between the time t_0 marking the begin of the state change (frequency, phase, and/or level) to the time t_s at which the device is settled. The characteristics used to define 'settled' can be phase, frequency, level, or any combination of these. Settled is defined as the time at which a characteristic of the signal is within a certain tolerance or does not change any further and has reached the final state.

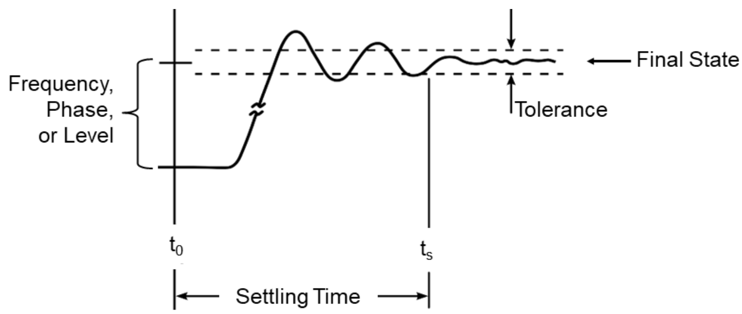

Fig. 7: Definition of the settling time

For the automatic evaluation of the settling time in the analog demodulation function it is important to set the sweep time is such a way that the settled state is at the end of the sweep and no further changes appear. This is very important in setups where more than one or periodic frequency settings are performed.

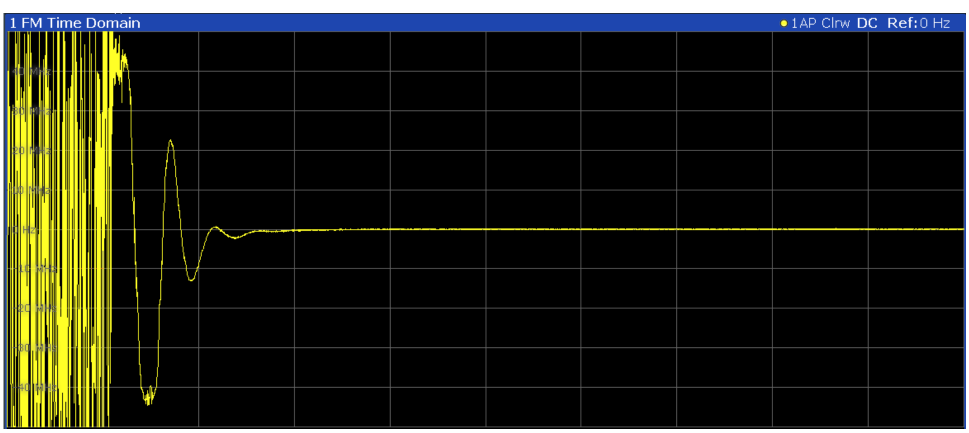

Fig. 8: Setting of the measurement time and scaling

Set the sweep time in such a way that the settling of the DUT can be recognized in the beginning of the sweep and no further change of the signal appears until the end of the sweep is reached.

The vertical scaling shall be set in such a way that the settling clearly appears on the screen. The maximum deviation is limited to half of the demodulation bandwidth. The DUT frequency step must or may not be fully visible on the measurement screen.

The measurement of the settling time is now possible by placing a marker on the trace at a position where the signal is within a defined limit (e.g. frequency tolerance). This measurement is also available as an automated function inside the analog demodulator application R&S®FSxx-K7.

4.1.3 Automatic determination of the settling time

This automated settling time measurement inside the analog demodulator application R&S®FSxx-K7 reduces the effort in the evaluation of transient measurements. The function is available in the measurement configuration:

Activate the settling time measurement: MEAS CONFIG: DEMOD CONFIG: SETTLING TIME: State ON

This step activates a routine that searches for the point in the measurement trace after which no trace value is outside a defined tolerance. These limits can be set individually for the upper and lower tolerance.

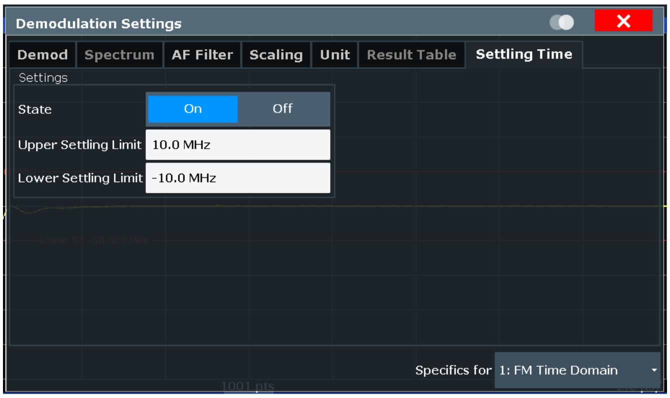

Fig. 9: Settling time tab within the demodulation configuration dialog

Once the settling time measurement is activated the result is shown on the screen:

Fig. 10: Result screen of the settling time measurement

The numerical result for the settling time is displayed in the result summary table marked in the screen shot. In addition, a marker "ST" is positioned on the trace to visually mark the determined trace point where the signal is within the defined tolerance.

5 Literature

[1] R&S®FSW Signal and Spectrum Analyzer – Product Brochure

[2] R&S®FSW Signal and Spectrum Analyzer – Data Sheet

[3] R&S®FSW-K7 Analog Modulation Analysis (AM/FM/φM) – Data Sheet

[4] Application Note 1EF102, Frequency and Phase settling time measurements on PLL circuits

6 Conclusion

Modern communication systems rely on the capability for fast frequency settling to optimize their data throughput and avoid interference or fading conditions. Fast frequency settling is one the key parameters the PLL designers will have to ensure. The time pressure on developers force them to optimize the way how circuit characteristics are measured and optimized. The traditional way using discriminators and oscilloscopes for these measurements no longer gives the best results. With the new generation of signal analyzers, the measurements can be performed in a fraction of the time needed for the setup of the old equipment. Using modern signal analyzers, much more data is collected and offers the user different views on his signal of interest, allowing him to get his job done with much less pain than in the past.

The automated determination of the settling time with the measurement demodulator further simplifies this measurement task. No complicated marker or delta marker settings are required to read the settling time anymore, a simple and straightforward measurement function gives reliable results.

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