Application Note

TESTING TRUE PERFORMANCE OF ADCs USING R&S®SMA100B SIGNAL GENERATOR

Products:

► R&S®SMA100B

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Contents

1 Overview

Analog-to-digital converters (ADCs) have taken giant steps in speed and accuracy over the past years: Such devices allow high-speed video processing and even software defined radio (SDR) applications, where digitization is being performed at ever-higher intermediate frequencies (IF). This has clearly raised the bar for ADC test equipment, especially regarding the noise performance of the analog input signal and sample clock sources used in the test setup. The R&S®SMA100B offers outputs for the analog input signal of the ADC as well as the clock input signal in one single instrument - both with outstanding signal purity.

2 Introduction

Many performance parameters for analog-to-digital converters (ADC) are identical to those for analog circuits in general. These include the well-known signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), signal to noise-and-distortion (SINAD), total harmonic distortion (THD) and third-order input intercept (TOII or IIP3).

With high-speed ADC products, where 16 bits at a few hundred MSPS are quite common and sampling rates can easily reach multiple GSPS, very pure signal sources are necessary. With current high-performance ADCs, SNRs of more than 90 dBFS become possible, requiring an input signal with an SNR of greater than 100 dB. With sampling rates surpassing the 10 GSPS mark, phase noise performance becomes even more important. Typically, the pure phase noise performance and phase noise induced SNR for a fixed input bandwidth gets worse with increasing carrier frequency. In addition to that, the higher the clock frequency, the harder it gets to realize very narrow bandpass filters. Thus, not only the phase noise performance gets worse, but the ADC also is affected by noise with a larger bandwidth, increasing the relevance of a low-phase noise signal source even more.

Figure 1 depicts a traditional test setup to determine the performance of an ADC. It consists of two signal sources and, depending on the application, sometimes one or two bandpass filters. To minimize measurement error, the specifications of the signal sources should always exceed those of the ADC itself.

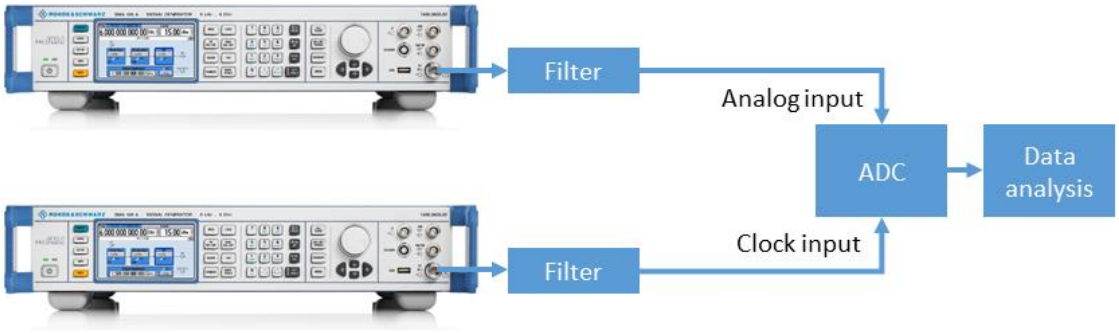

Figure 1 Traditional ADC performance test setup

In Figure 2, a modern test setup is shown. Instead of two signal generators, only one R&S®SMA100B is used to excite the ADC under test. The R&S®SMA100B not only offers an RF output, but also an optional clock output within the same instrument. Both, the RF output and the clock output, provide signals with highest purity. Therefore, in many cases neither a second signal generator, nor filters are needed to obtain accurate measurements.

Figure 2 Modern ADC performance test setup

This document outlines the most important aspects concerning ADC noise and distortion performance and presents some typical performance data such as jitter and SNR for the analog high-end signal generator R&S®SMA100B when used as signal or clock source.

3 Fundamentals

3.1 Ideal Signal-to-Noise Ratio (SNR in dB)

The signal-to-noise ratio (SNR) is the ratio of the RMS signal amplitude to the RMS value of the sum of all spectral components except the desired signal, the first six harmonics and DC. As the signal level is decreased, SNR typically decreases decibel-for-decibel in a linear fashion.

For an ideal ADC with a full scale sinusoidal at the input and exact rounding, the SNR is determined by the quantization noise of the converter and can be estimated as:

$$SNR = 20\log_{10}\left(\sqrt{1.5}\cdot 2^{n}\right) \approx 6.02\cdot n + 1.76\ dB \quad (1)$$

where:

n number of bits.

The ideal SNR for typical ADC resolutions is provided below:

Number of bits	8	10	12	14	16
SNR/dB	50	62	74	86	98

For oversampled systems, where the sampling frequency is higher than twice the Nyquist frequency and with adequate filtering after AD conversion, the SNR must be calculated as:

$$SNR = 20\log_{10}\left(\sqrt{3}\cdot 2^{n-1}\cdot\sqrt{\frac{f_{clk}}{f_{analog}}}\right) \quad (2)$$

$$SNR \approx 6.02\cdot n + 1.76\ dB + 10\log_{10}\left(\frac{f_{clk}}{2\cdot f_{analog}}\right) \quad (3)$$

where:

f_{clk} sampling or clock frequency

f_{analog} analog input frequency

A detailed derivation for equations (1) and (2) can be found in [1].

3.2 Jitter

Jitter is one of the most critical parameters when discussing the SNR performance of a real ADC [2], [3]. It describes the stability of a signal in the time domain and specifies the signal's fluctuations of zero crossings as shown in Figure 3 for a 10 MHz sine signal with very high jitter (yellow trace $t_{jitter1}$) and lower jitter (blue trace $t_{jitter2}$).

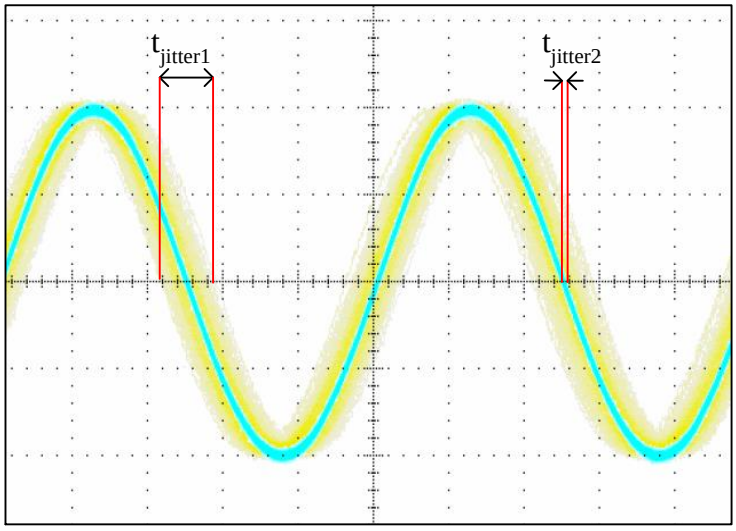

Figure 3 10 MHz signal with very high jitter (yellow trace) and with lower jitter (blue trace)

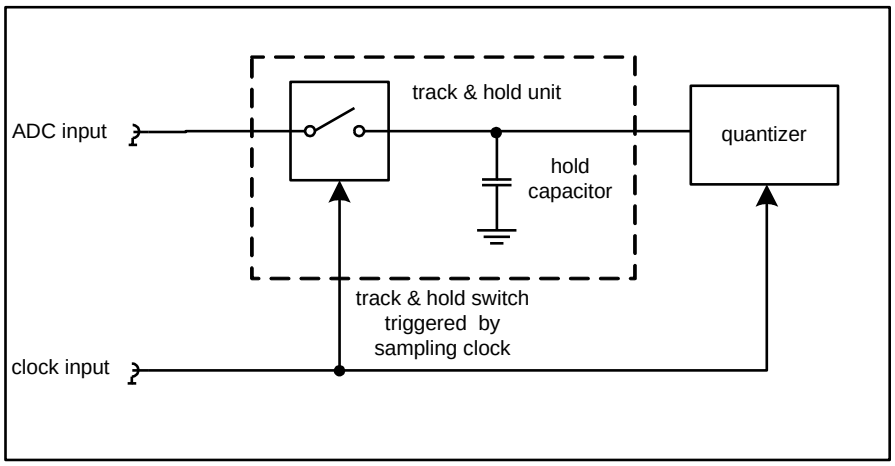

Figure 4 Basic block diagram of track & hold unit of an ADC input stage

Figure 4 is a basic block diagram of the track & hold unit of an ADC input stage. At the beginning of the sampling process, the track & hold switch is closed and the voltage at the hold capacitor follows the input voltage. The zero crossing of the ADC's clock signal opens the track & hold switch, and the voltage across the capacitor is held. The conversion process in the quantizer is then performed. Any error in the zero crossing point may therefore translate to a voltage error at the hold capacitor in general. In a first-order approximation, the voltage error is proportional to the jitter and input slope of the signal as shown in Figure 5 below:

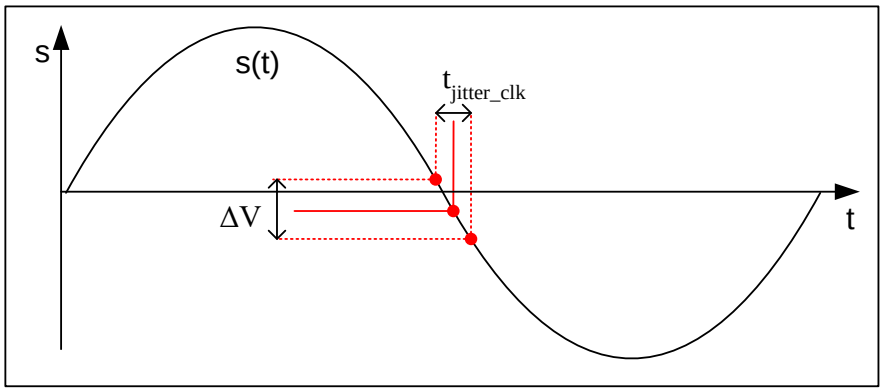

Figure 5 Voltage error ΔV due to jitter on the sampling clock $t_{jitter,clk}$

The approximate voltage error ΔV of a signal $s(t)$ due to sampling jitter in Figure 5 can be expressed as:

$$\Delta V = slewrate\big(s(t)\big) \cdot t_{jitter} = \frac{d}{dt} s(t) \cdot t_{jitter,clk} \tag{4}$$

For a sine wave signal, $s(t)$ is determined as follows:

$$s(t) = A \cdot \sin\big(2\pi \cdot f_{analog} \cdot t\big) \tag{5}$$

This yields a voltage error ΔV of:

$$\Delta V = A \cdot 2\pi \cdot f_{analog} \cdot \cos\big(2\pi \cdot f_{analog} \cdot t\big) \cdot t_{jitter} \tag{6}$$

Its RMS value can be expressed as:

$$\Delta V_{RMS} = \sqrt{\frac{1}{T} \cdot \int_0^T \Delta V(t)^2 dt} = \frac{A}{\sqrt{2}} \cdot 2\pi \cdot f_{analog} \cdot t_{jitter,clk} \tag{7}$$

The SNR due to clock jitter is then the relation between the RMS signal voltage and the RMS voltage error:

$$SNR_{jitter,clk} = 20 \log\left(\frac{\frac{A}{\sqrt{2}}}{\frac{A}{\sqrt{2}} \cdot 2\pi \cdot f_{analog} \cdot t_{jitter,clk}}\right) = -20 \log\big(2\pi \cdot f_{analog} \cdot t_{jitter,clk}\big) \tag{8}$$

where:

f_{analog}	analog input frequency to the ADC
$t_{jitter,clk}$	RMS clock jitter

The RMS jitter of a signal is the most commonly used expression and is usually also used for SNR calculation. If a signal with a Gaussian-distributed jitter is considered, the RMS value for the jitter is equal to the standard deviation.

In case the jitter is given as peak-to-peak measure, the RMS jitter equates to $t_{jitter,rms} = \frac{t_{jitter,clk}}{2 \cdot \sqrt{2}}$. For some digital data transmission standards working with different data rates (e.g. SONET/SDH), the so-called *unit interval* (UI) jitter is typically used instead of the RMS jitter. This normalized jitter allows a consistent comparison of jitter for different data rates. In this case, the RMS jitter can be recovered using $t_{jitter,rms} = \frac{t_{jitter,UI}}{f_0}$ with the signal frequency f_0.

3.3 Relation between Phase Noise and Jitter

Generally, the phase noise performance of a signal generator is described in terms of the single sideband phase noise (SSB phase noise) $L(f_{off})$, as shown in Figure 6 for the R&S®SMA100B at 1 GHz.

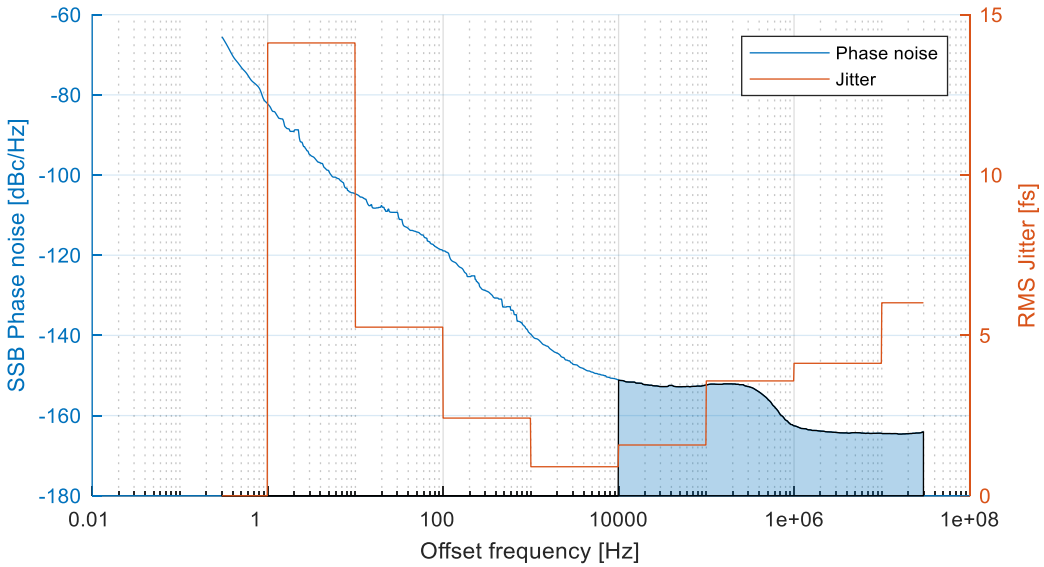

Figure 6 Measured SSB phase noise and RMS jitter from the R&S®SMA100B with option B711 at $f = 1\ GHz$

The SSB phase noise $L(f_{off})$ is defined as the ratio of the phase noise power spectral density in 1 Hz bandwidth at a carrier offset f_{off} to the carrier power. The SSB phase noise describes the signal quality in the frequency domain.

There is a direct relationship between phase noise and jitter. RMS jitter is evaluated by integrating the phase noise within a defined bandwidth, as graphically illustrated by the blue area in Figure 6 for each decade from 1 Hz to 10 MHz and the last half decade. The RMS jitter can be calculated from the SSB phase noise using the expression:

$$t_{jitter} = \frac{1}{2\pi f_0}\sqrt{2\int_{f_1}^{f_2} 10^{\frac{L(f_{off})}{10}}\, df_{off}} \qquad (9)$$

where:

f_0	carrier frequency
f_1	lower offset frequency for integration
f_2	upper offset frequency for integration
$L(f_{off})$	SSB phase noise at offset f_{off}

The factor 2 in front of the integral in equation (9) represents the contributions from both sidebands, as the integrand $L(f_{off})$ only describes the SSB phase noise.

In Figure 6, the RMS jitter for the SSB phase noise is calculated for each decade and plotted as the red trace. As the figure clearly shows, the jitter contribution close to the carrier rises since the phase noise increases very rapidly for decreasing offsets in this area. However, a question remains: Why does the jitter per decade increase again for offsets above 1 kHz while the phase noise decreases in this area? The reason is the increasing integration bandwidth used for the jitter calculation. For example, the bandwidth for jitter calculation from 1 MHz to 10 MHz is 9 MHz as compared to 90 kHz for the decade from 10 kHz to 100 kHz. For this example, the integration bandwidth has increased by a factor of 100 (= 20 dB) whereas the phase noise contribution is only approx. 10 dB lower.

Since frequency offsets close to the carrier are of no consequence to high-speed applications (see also the next section), it becomes clear that wideband noise is the most significant parameter affecting jitter performance for high-speed ADCs.

If the total jitter contribution for multiple decades or for jitter sources is needed, it is necessary to take the root sum square of the individual jitter contributors per decade or adapt the integration limits accordingly.

3.4 Jitter Bandwidth

One important aspect when calculating jitter is the clock bandwidth (difference in offset frequencies f_1 and f_2 in equation (9)), which should be considered for integration.

The lower offset frequency f_1 depends on the frequency resolution of the system under consideration. Phase fluctuations, which are slower than the observation time for one FFT shot, do not add to the measurement result when evaluated in the frequency domain. Alternatively, looking upon this fact from the time domain perspective, phase error contributions with sufficiently low frequencies look roughly constant for short time periods. This roughly constant phase error can be ignored, as the non-coherent sampling viewed here is not phase-locked to any signal, so that the constant phase difference between analog input and clock is unknown. With those considerations, the lower frequency for jitter integration can be calculated as:

$$f_1 = \frac{f_{clk}}{FFT\ length} \tag{10}$$

where:

f_{clk}	clock or sampling frequency of the ADC
$FFT\ length$	number of FFT samples, e.g. 65536 for a 64k FFT

Example: A 64k FFT performed with an ADC running at 1 GSPS encode rate leads to a frequency resolution of

$$f_1 = \frac{1\ GHz}{65536} = 15.2\ kHz$$

Thus, for most high-speed ADC applications, the phase noise close to the carrier brings no significant distortion to the sampling process. It becomes more dominant, though, in systems with longer capturing durations and thus higher frequency resolutions or in systems with lower sampling rate.

The upper offset frequency f_2 depends on the maximum bandwidth of the clock signal path. The analog input bandwidth usually equals the Nyquist band edge ($f_{clk}/2$), but could be much lower for narrowband applications. The bandwidth of the clock path depends on the filtering used and can range from several MHz up to a few GHz. Since equation (9) performs the integration for both sidebands of SSB phase noise, the upper offset frequency f_2 is always half the clock bandwidth, assuming symmetric phase noise sidebands. This will integrate the noise from the carrier, which is assumed to be in the middle of the clock path pass band, to the edge of the clock path pass band.

Example: For an ADC running at 125 MSPS encode rate and a clock bandwidth of 200 MHz, the upper offset frequency for jitter calculation is 100 MHz.

Example: The SONET communications standard [4] states its jitter requirements in terms of an integration bandwidth from 12 kHz to 20 MHz.

Although those values are aimed at data transmissions with rates up to 2488.32 Mbps using 155.32 MHz reference clocks, they are still widely used to characterize and specify jitter based on phase noise. For RF sampling applications with input frequencies up to 10 GHz and higher, IC package and technology for the ADC need to allow appropriate bandwidths. This also enables increasing clock bandwidths, in case there is no additional filtering implemented in the clock path.

Regardless of jitter bandwidth, the lowest possible jitter – and therefore the best SNR – can only be achieved by using proper filtering on both the analog input and clock paths.

One important aspect needs to be mentioned here: Since an ADC is a sampled system, the analog input signal is convolved with the clock signal in the frequency domain. This means that the spectral distribution of the clock signal shapes the sampled signal at the ADC output. If the bandwidth of the clock signal is greater than the Nyquist band, the wideband noise of the clock signal will be aliased completely into the Nyquist band [5] as graphically shown in Figure 7.

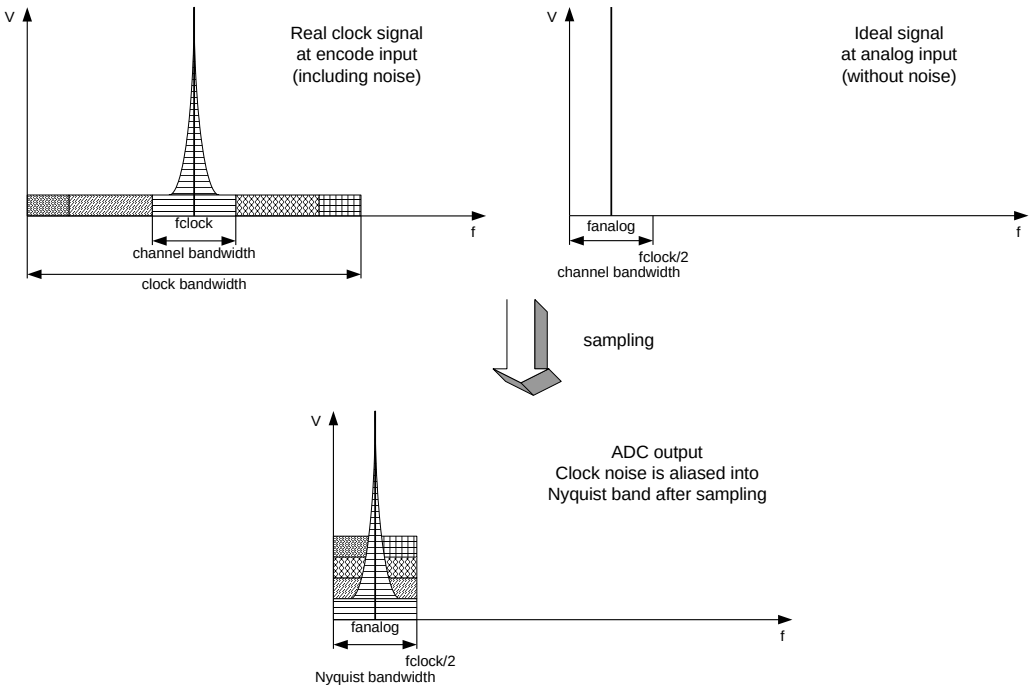

Figure 7 Graphical illustration of clock noise aliasing into Nyquist band

As a result, the energy of the clock signal's wideband noise is accumulated many times within the Nyquist band, thus reducing the SNR significantly.

Example: For an ADC running at a clock rate of 80 MSPS and a clock bandwidth of 160 MHz, the wideband noise of the clock signal is aliased 4 times into the Nyquist band (40 MHz), causing a degradation of the SNR contribution due to the clock source of 6 dB.

3.5 Real Signal-to-Noise Ratio (SNR in dB)

The SNR of a real ADC is degraded from the imperfections explained above, and it is illustrated for an arbitrarily chosen 14-bit ADC in Figure 8 below.

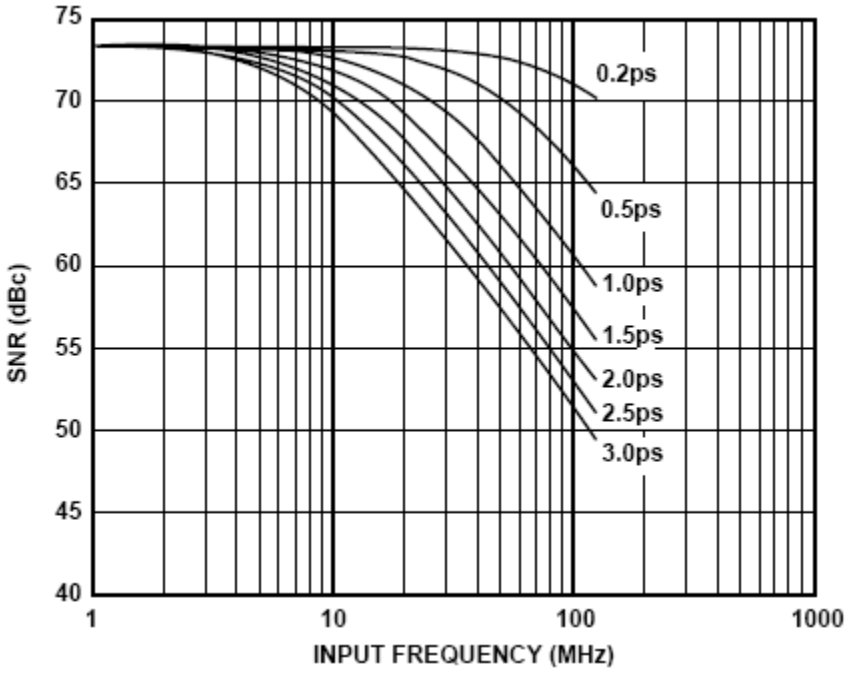

Figure 8 SNR vs. analog input frequency and clock jitter [6]

Figure 8 shows that for a real 14-bit converter, it is not possible to reach the ideal SNR of 86 dB even at very low input frequencies. This is due to factors such as jitter on the clock and analog input signals as well as factors associated with ADC design, including intrinsic aperture jitter, differential nonlinearities (DNL) in the ADC quantizer and other internal noise such as thermal noise.

The real signal-to-noise ratio due to these effects can be approximated and summed together as:

$$SNR_{ADC,real} = -10\log_{10}\left(10^{-\frac{SNR_{ADC,Noise}}{10}} + 10^{-\frac{SNR_{jitter}}{10}}\right) \quad (11)$$

with

$$SNR_{ADC,Noise} = -20\log_{10}\sqrt{\left(\frac{U_{thermal}}{2^n}\right)^2 + \left(\frac{1+e}{2^n}\right)^2} \quad (12)$$

and

$$SNR_{jitter} = -20\log_{10}\sqrt{\left(2\pi f_{analog}\right)^2 \cdot \left(t_{jitter,ADC}^2 + t_{jitter,clk}^2 + t_{jitter,ana}^2\right)} \quad (13)$$

where:

$SNR_{ADC,Noise}$	signal-to-noise contribution due to ADC noise and nonlinearities
SNR_{jitter}	signal-to-noise contribution due to jitter
$U_{thermal}$	internal thermal noise of the converter
n	number of bits
e	average DNL of the converter
f_{analog}	analog input frequency
$t_{jitter,ADC}$	intrinsic aperture RMS jitter of the converter
$t_{jitter,clk}$	RMS jitter of the clock source
$t_{jitter,ana}$	RMS jitter of the analog signal source

Equation (12) describes the device's intrinsic noise floor due to thermal noise and converter nonlinearities. This noise floor is constant over input frequency and can therefore be neglected at high signal frequencies,

where SNR degradation due to jitter becomes dominant. However, at low input frequencies, these effects determine the maximum available SNR, e.g. 73 dB for the ADC shown in Figure 8.

At higher frequencies, the SNR performance of a converter is determined mainly by jitter as seen in the set of curves in Figure 8. Equation (13) provides the mathematical description for the SNR performance of an ADC due to jitter and shows that the impact of jitter increases with higher signal input frequency.

Substituting (13) and (12) into (11) yields [2]:

$$SNR_{ADC,real} = -20\log_{10}\sqrt{\left(2\pi f_{analog} t_{jitter}\right)^2 + \left(\frac{U_{thermal}}{2^n}\right)^2 + \left(\frac{1+e}{2^n}\right)^2} \quad (14)$$

where:

t_{jitter} RMS sum of all jitter contributions

$$t_{jitter} = \sqrt{t_{jitter,clk}^2 + t_{jitter,ana}^2 + t_{jitter,ADC}^2} \quad (15)$$

or in exponential form

$$SNR_{ADC,real} = -10\log_{10}\left(10^{-\frac{SNR_{ADC,Noise}}{10}} + 10^{-\frac{SNR_{jitter,ADC}}{10}} + 10^{-\frac{SNR_{jitter,clk}}{10}} + 10^{-\frac{SNR_{jitter,ana}}{10}}\right) \quad (16)$$

One common way to isolate the SNR contributors of an ADC is to perform an SNR measurement at a specific clock rate with a very low input frequency (yielding $SNR_{ADC,Noise}$) and a second SNR measurement with the same clock rate but at a very high input frequency (yielding $SNR_{ADC,real}$). Using equation (13), the SNR due to jitter can be calculated, but it is not possible to determine which part is from the ADC and which part is from the clock or analog source. If the jitter contribution of the analog source and clock source is known, it is possible to isolate the ADC jitter using equation (16).

Of course, this technique does not provide exact values of the ADC's noise and jitter. All individual considered noise sources and their relation to the SNR inside the ADC as well as from the signal generator are only approximations. As such, an input signal with high purity is desirable for ADC testing. In this case, SNR calculations for the ADC are less affected by modeling inaccuracies (e.g. simplifications like averaging over DNL effects or ignoring non-linearities) between SNR contribution and signal impurity, as the latter becomes smaller.

3.6 Relation between Wideband Phase Noise, Jitter and SNR at Clock Input

For most ADCs, the amplitude of the clock signal is hard-limited by the use of internal differential input and buffer stages. This minimizes amplitude effects. Therefore, only fluctuations of zero crossings (= phase noise) of the clock signal influence the sampling process.

As already pointed out, the close-in phase noise is negligible for most high-speed applications. Thus, often only the wideband phase noise contributes to the SNR performance of the ADC induced by clock imperfections in a significant way. The spectral density of the wideband phase noise is often assumed to remain constant for offsets >10 MHz to simplify jitter estimations. As this estimation can often turn out to be incorrect, other estimations or upper bounds are preferable for system design and evaluation.

Assuming that the overall wideband noise has equal parts of phase noise and amplitude noise, the wideband phase noise can be estimated to be 3 dB below the overall wideband noise. Thus, to obtain an upper bound for the actual wideband phase noise, the specified overall wideband noise level of the signal generator can be divided in half. For tighter estimations, the signal generator's overall wideband noise can be measured directly over the relevant frequency range. In addition, when considering sufficiently large integration bands, it is recommended to check the assumption, that the left and the right sideband contribute equally to the jitter. For further details on this matter, see also the explanations in section 4.2 regarding the overall wideband noise performance of the R&S®SMA100B.

In the case that the wideband phase noise shall be estimated from the overall wideband noise specifications of the signal generator, the integrated noise for the jitter calculation (see equation (9)) can be expressed as:

$$Noise_{integrated} \lesssim BBNoise_{clk} + 10\log_{10} BW_{clk} - 3dB \quad (17)$$

where:

$BBNoise_{clk}$ specified maximum broadband/wideband noise of the clock signal
BW_{clk} clock bandwidth

Replacing the integral in equation (9) by equation (17), the clock jitter can be calculated by:

$$t_{jitter} = \frac{1}{2\pi f_{clk}} \sqrt{10^{\frac{Noise_{integrated}}{10}}} \quad (18)$$

The multiplier of 2 for the integral, representing both SSB phase noise sidebands, is already included in $Noise_{integrated}$ in equation (17) as the complete clock bandwidth is used for integration.

Substituting t_{jitter} in equation (13) by equation (18) yields:

$$SNR_{jitter,clk} = -20\log_{10}\left(2\pi f_{analog} \frac{1}{2\pi f_{clk}} \sqrt{10^{\frac{Noise_{integrated}}{10}}}\right)$$

$$SNR_{jitter,clk} = -Noise_{integrated} - 20\log_{10}\frac{f_{analog}}{f_{clk}}$$

Substituting $Noise_{integrated}$ by equation (17) yields:

$$SNR_{jitter,clk} \gtrsim -BBNoise_{clk} - 10\log_{10} BW_{clk} + 3dB - 20\log_{10}\frac{f_{analog}}{f_{clk}} \quad (19)$$

where:

$BBNoise_{clk}$ specified maximum broadband/wideband noise of the clock signal
BW_{clk} clock bandwidth
f_{analog} analog input frequency of the ADC
f_{clk} clock/sampling frequency of the ADC

Equation (19) estimates the SNR of an ADC in the frequency domain using the wideband phase noise spectral density, whereas equation (8) calculates the SNR in the time domain using the jitter. Nevertheless, both equations should yield the very close results for operating regions where the approximation of constant wideband phase noise is adequate. For good approximations accuracies, both results are usually within 1 dB.

3.7 Effects in Under- or Oversampled Systems

More and more modern communication systems implement direct conversion of high IF frequencies into the digital domain. To support lower clock frequencies, a technique called undersampling is used. In this case, the sampling rate is lower than the signal frequency and the aliasing effect is used to downconvert the signal to the baseband. For this, the spectral purity requirements of the clock signal that is used are considerably higher in such systems as shown below.

An important factor here is the last term of the equation (19): $-20\log\left(\frac{f_{analog}}{f_{clk}}\right)$. It causes the SNR of a sampled system to degrade with 6 dB every time the analog input frequency doubles.

The reason for this becomes clear by graphically showing the effect of jitter for both oversampling and undersampling. In the case of undersampling, the slightest delay in sampling generates a huge variation in the sampled value. In contrast, oversampled systems experience only small sample variations for a given clock delay. This is depicted below.

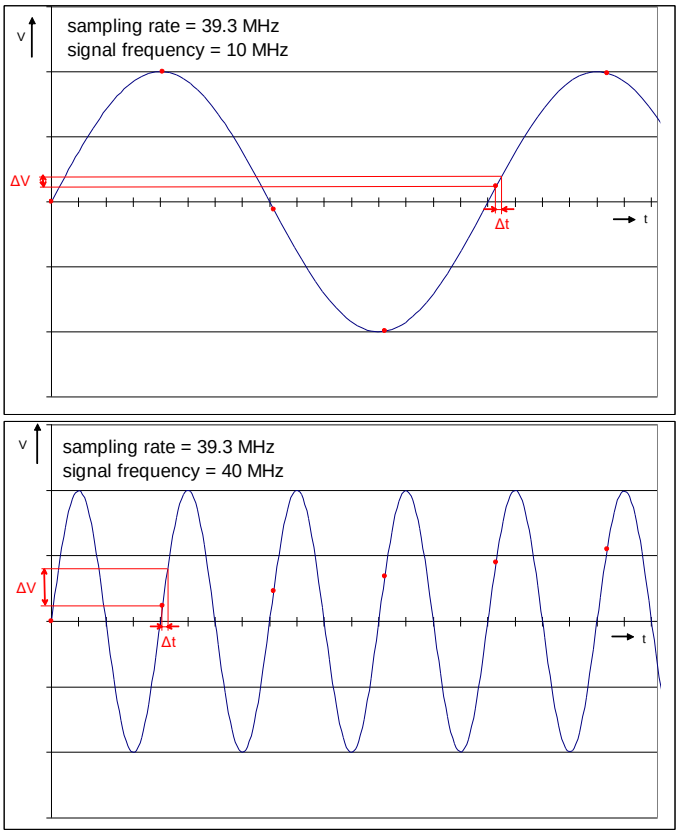

Figure 9 Effect of jitter on over- and undersampled systems

This is an important element for ADCs used in undersampled IF stage systems since the SNR can deteriorate considerably. It is necessary to verify whether the performance of the clock source complies with the required specification. The requirements for the phase noise of the clock source in undersampled systems are much higher than in baseband systems. The performance in many IF-sampling radio architectures is limited by clock phase noise, not data converter performance.

3.8 Relation between Wideband Noise, Jitter and SNR at Analog Input

Any calculation of the SNR contribution of an ADC's analog signal input must take the amplitude and phase noise of the analog signal source into account since no amplitude-limiting input stages are present at the analog input.

As with the clock input, calculating the SNR at the analog input requires to integrate over the signal generator's overall noise spectral density. This is often assumed to remain constant for offsets >10 MHz or to remain below a specified wideband noise spectral density. Alternatively, it can be measured for different frequencies throughout the integration range.

In order to determine a lower bound of SNR_{analog} and therefore an upper bound of its contribution to the total SNR, we can once again use the generator's wideband noise specification. Equation (19) describes an estimate for the SNR due to phase noise at the clock input. For the analog signal input, the relation must be changed to:

$$SNR_{analog} \gtrsim -BBNoise_{analog} - 10\ \log_{10} BW_{analog} \qquad (20)$$

where:

$BBNoise_{analog}$ specified maximum overall wideband noise spectral density of the analog signal

BW_{analog} bandwidth of the ADC analog input signal (usually $\frac{f_{clk}}{2}$ or below)

As the term $\frac{f_{analog}}{f_{clk}}$ was only relevant for jitter calculation, the relation of input and clock frequency has no effect on the SNR contribution of the analog signal source to the ADC's performance.

3.9 Distortion and Spurious

Besides noise performance, the spectral purity due to spurious and signal distortion is the most important parameter of an ADC. Definitions of some commonly used expressions are listed below [7]:

- Signal-to-noise and distortion (SINAD in dB)

  The signal-to-noise and distortion (SINAD) value is the ratio of the RMS signal amplitude to the RMS level of the sum of all spectral components, including harmonics but excluding DC and the desired signal. The difference between SNR and SINAD is the energy contained in the first six harmonics.

- Total harmonic distortion (THD in dBc)

  Total harmonic distortion (THD) is the ratio of the RMS signal energy to the RMS value of the sum of the first six harmonics.

- Spurious-free dynamic range (SFDR)

  The spurious-free dynamic range (SFDR) is the ratio of the RMS level of the signal to the RMS level of the peak spurious spectral component at the ADC output.

To measure these parameters, an analog signal source with very low harmonic distortion and non-harmonics is required.

- Third-order input intercept point (IIP3 in dBm)

  The third-order input intercept point (IIP3) is determined by applying a two-tone signal to the analog input of the ADC and measuring the emerging intermodulation products.

  The IIP3 is normally far beyond the maximum input level of the analog input, but it is a measure of the linearity of the ADC's input stage.

3.9.1 Harmonics

Harmonics are integer multiples of the fundamental signal frequency that might be generated at any active stage within the RF path due to semiconductor nonlinearities. The offset frequency to the carrier can be evaluated exactly, and it makes the use of suitable filters for suppression possible in those cases, where the range of input frequencies is sufficiently small.

Generally, the signal generator's harmonic distortion is less critical than the non-harmonic performance since the frequencies of the harmonic spurs are known (integer multiple of the fundamental signal) and since these spurs are located far from the carrier in the case of most high-speed applications.

Harmonics applied to the ADC's clock input normally do not influence the performance of the converter since the zero crossing of the clock signal is not shifted by harmonic signal components. Furthermore, the ADC's clock input stage normally converts an applied sine signal into a square signal containing strong harmonic signal components in any case.

For the analog input signal, harmonic distortion is still critical to the ADC's performance, as it aliases into the sampled signal. However, for many applications the out-of-the-box harmonics performance of the R&S®SMA100B may be already sufficient. If this is the case, no additional filtering is needed and there is no restriction on the analog input frequency due to any fixed filter pass or stop bands. As the harmonics of the R&S®SMA100B reach levels around and well below -70 dBc or even lower for higher order harmonics, this is the preferable route for many applications.

In case the harmonic distortion has to be even less than what the signal generator already provides, additional filtering is required for the input signal. For this, typically lowpass or bandpass filters or combinations of both are used, depending on the specific requirements [7]. With the high performance of the R&S®SMA100B, the requirements for the filters can be lowered.

Lowpass filters suppress the harmonics effectively and have the advantage that the frequency of the source signal can still be varied across a specific range. However, part of the wideband noise is still passed to the ADC and the noise contribution of the analog signal source can only be improved partially.

Bandpass filters have an identical effect on the harmonics, but they also have the additional advantage that the noise and subharmonics are suppressed more effectively. The disadvantage is that the test can only take place within a narrow frequency range, so several filters are needed in order to perform tests over a wide frequency range.

For both filter types, the high frequency suppression of the used filter must be examined carefully in order to eliminate high-order harmonics of the input signal. This signal could possibly cross the clock frequency, or even a multiple of it and could alias back to the Nyquist band. If multiple filters are combined in series, a fixed attenuator between the filters should be used to improve the matching between these filters. Otherwise, the filter characteristic may become much worse than expected.

Example: Assume that an ADC is running at a clock rate of 1 GSPS and that the analog input frequency is 428 MHz. Due to insufficient filtering, the 6th harmonic of the input signal at 2568 MHz is only suppressed by 5 dB. Therefore, it is applied with a level of, for example, –90 dBc to the input of the converter. As a result, an alias product might appear in the output spectrum of the converter. This harmonic at 2568 MHz lies between 2.5 GHz and 3 GHz and therefore between two and a half and three times the sample rate:

$$f_{\text{alias}} = (3 \cdot f_{\text{clk}}) - \left(6 \cdot f_{\text{analog}}\right) = 432\ \text{MHz}$$

3.9.2 Non-Harmonics

For signal generators, non-harmonic signal components are more critical than harmonics because adequate filtering is generally not possible. The frequency of a non-harmonic spurious cannot easily be predicted, which means that the offset to the carrier is unknown. A spurious line can appear very close to the carrier (e.g. 20 kHz) for one frequency and very far from the carrier (e.g. 100 MHz) at another frequency.

Non-harmonics are critical to both the clock and the analog signal input of an ADC. In the general case, a single non-harmonic spur is equivalent to amplitude modulation as well as phase modulation of the carrier due to its complex nature in the baseband. Thus, the zero crossings of the clock signal at the ADC input stage fluctuate as well.

For the special case of a pair of spurs that is symmetric around the carrier, a modulation of only the amplitude or only the phase is possible depending on the phase difference between the two spurs as well as between spur and carrier. If the spurs are added in-phase to the carrier, only amplitude modulation occurs. When the spurs are added in quadrature to the carrier instead, the baseband signal has almost unity

magnitude but a sinusoidally modulated phase. In the general case, the pair of spurs modulates both the amplitude as well as the phase of the carrier with distorted sinusoidals, though.

For a spurious at the clock input, the level of this non-harmonic at the ADC output signal depends on the relation between the clock and analog signal frequency, just like for the phase noise of the clock signal. Therefore, the spur level of the clock signal must be corrected by the following expression:

$$k = 20\log\left(\frac{f_{analog}}{f_{clk}}\right) \tag{21}$$

Example: A spur at -80 dBc is present at the clock signal of an ADC running with 20 MSPS clock rate and an analog input frequency of 50 MHz. According to equation (21), the spurious appears at the converter output at a level of -72 dBc, reducing the SFDR performance of the ADC drastically.

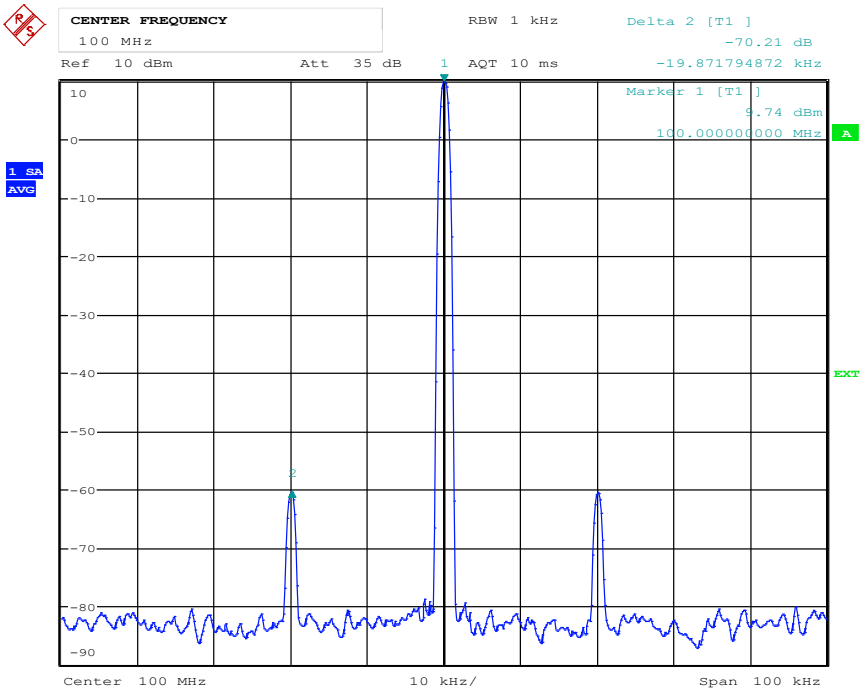

Figure 10 Symmetrical pair of non-harmonic spurs at 20 kHz carrier offset

Figure 10 shows a symmetrical pair of spurs for a 100 MHz carrier frequency at 20 kHz offset generated by a low-performance signal source with a (single sideband) spur level of -70 dBc. Without knowing the relative phase difference between both spurs and to the carrier, it is not possible to predict the exact nature of the modulation. Nevertheless, an upper bound for the generated distortion is possible. Additionally, expressions for SNR and SFDR are valid regardless of the exact modulation, as both only consider the spurious energy. For jitter induced by spurs, it is possible to assume that the symmetric pair is added in quadrature and will cause the maximum possible phase modulation.

When selecting an appropriate signal source for ADC testing, the spurious specification of the source must be carefully considered over the complete frequency range. As a first approach, the performance of the signal source should be approx. 10 dB better than the performance of the tested DUT.

3.9.3 Signal deterioration from Non-Harmonics

To obtain the RMS jitter of such a symmetrical pair of spurs that cause pure phase modulation, one can evaluate equation (9) for these spurs and gets:

$$t_{jitter,rms} = \frac{\Delta\varphi_{rms}}{\omega_0} = \frac{\frac{1}{\sqrt{2}} \cdot 2 \cdot 10^{\frac{a_{spur}}{20}}}{2\pi \cdot f_0} = \frac{10^{\frac{a_{spur}}{20}}}{\sqrt{2}\pi f_0} \tag{22}$$

where:

a_{spur} the (SSB) level of the spur pair in dBc

f_0 the carrier frequency

The SNR contribution of a phase modulating pair of non-harmonic spurs at the clock input of an ADC can be calculated by substituting equation (22) into equation (8):

$$SNR_{spur,clk} = -20\log\left(\frac{10^{\frac{a_{spur}}{20}} \cdot 2\pi \cdot f_{analog}}{2\sqrt{2}\pi \cdot f_{clk}}\right) = -a_{spur} - 3\,\text{dB} - 20\log\left(\frac{f_{analog}}{f_{clk}}\right) \quad (23)$$

For a symmetric pair of spurs at the analog input of an ADC, equation (23) simplifies to:

$$SNR_{spur,analog} = -a_{spur} - 3\,\text{dB} \quad (24)$$

The SFDR due to a non-harmonic spurious at the analog signal input of an ADC is equal to the spurious distance of the signal source, which is the relation of spur level to signal level.

For a non-harmonic applied to the clock input, again the relation between analog frequency and clock rate must be considered by applying the correction factor k (see equation (21)) to the influence of the spurs on the SFDR value.

3.9.4 Intermodulation

For testing the third-order intercept point (IIP3) of a DUT, a two-tone signal at the analog ADC input is required. A common way to generate a two-tone signal is to combine the output signals of two signal generators, working at different frequencies, by using a power combiner. However, issues can arise with modern signal generators, which are equipped with an automatic level control (ALC) loop. This can happen due to limited isolation of the power combiner. A small portion of the signal generated by one signal generator travels through the combiner to the output of the other signal generator. Consequently, this part of the signal couples to the signal generator's output detector, resulting in an amplitude modulation of this generator's output signal with the difference frequency of the two generators. Figure 11 shows an example with the corresponding AM sidebands visible in the power combiner's output spectrum.

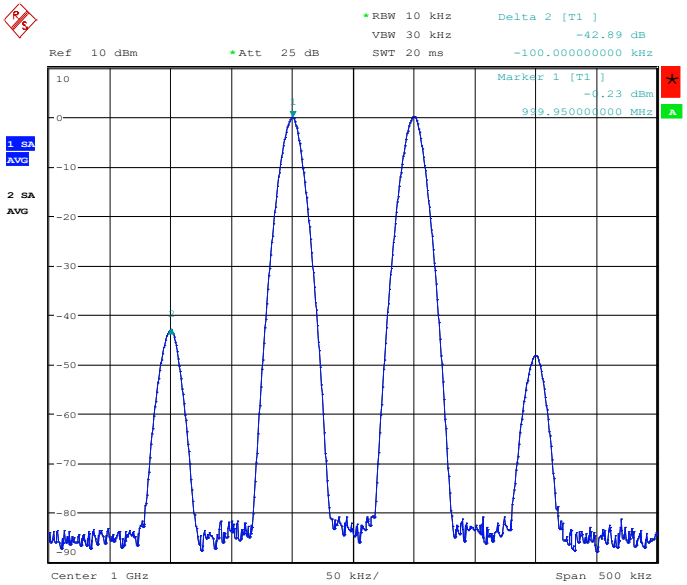

Figure 11 Example output spectrum showing interacting ALC loops

This can be problematic in cases where the signal generator's IM3 products are so high, that they distort the ADC measurement. Depending on accuracy requirements, one might consider a margin of 10 dB between the generator's IM3 products and the ones from the ADC. Often, the ALC has to be switched off in order to achieve this.

The R&S®SMA100B is able to prevent this problem in many situations. Depending on the hardware options and the configured settings, you can take advantage of the ALC while still getting very low IM3 artifacts at the same time for carrier distances of a few 100 kHz already. The dynamically adapted ALC bandwidth greatly reduces the amount by which the two ALC loops interact with each other. During transient, the ALC bandwidth allows fast settling behavior. After the desired level is reached, the bandwidth is reduced in order to filter out spectral components from other sources. Therefore, the ALCs produce much smaller IM3 artifacts that could distort the two-tone test-signal. Figure 12 shows the output spectrum for two R&S®SMA100B signal generators combined with a power combiner. As showcased in Figure 13 the used R&S®SMA100B was measured with a minimum IM3 attenuation of 75 dB over its frequency range, using a coupler with 20 dB isolation and a carrier spacing of 10 MHz.

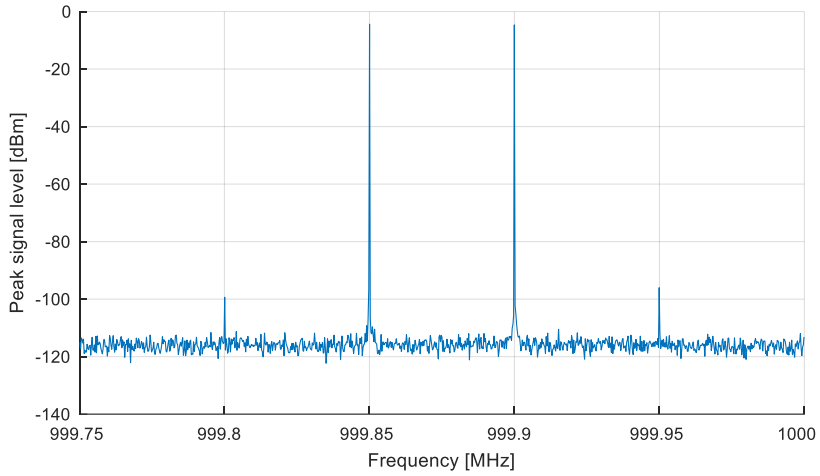

Figure 12 Output Spectrum for two R&S®SMA100B

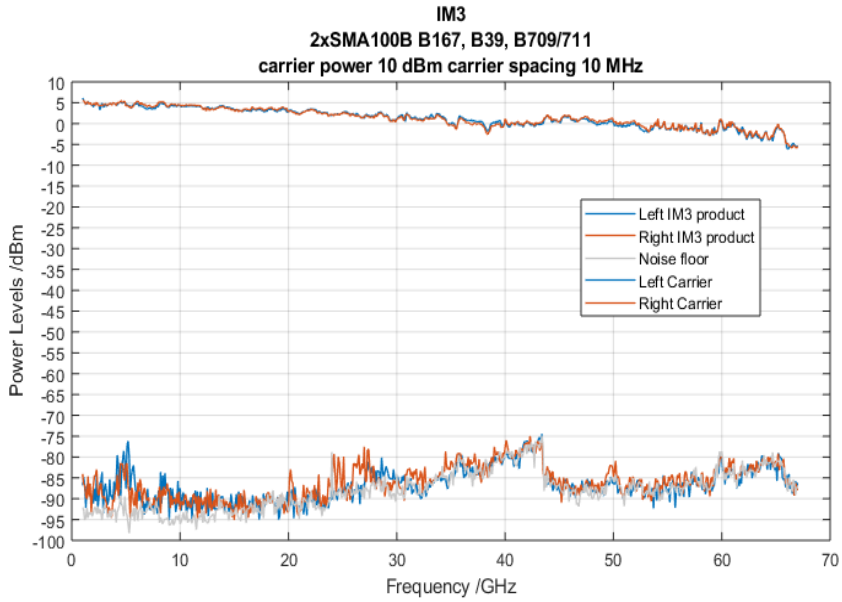

Figure 13 IM3 products vs. frequency

4 Performance of the R&S®SMA100B for ADC Testing

Spectral purity is by far the most limiting factor for a potential signal source and is deteriorated mainly by noise, harmonics and non-harmonic spurs. Thus, this application note focuses predominantly on the generator's performance in each of those metrics.

Ultimately, these factors determine a potential candidate for signal or clock source for an ADC test setup.

This section provides data for the spectral purity of an R&S®SMA100B analog signal generator with the R&S®SMAB-B711 ultra low phase noise option installed. The impact on ADC performance measurements is described by means of examples.

4.1 Phase Noise Performance

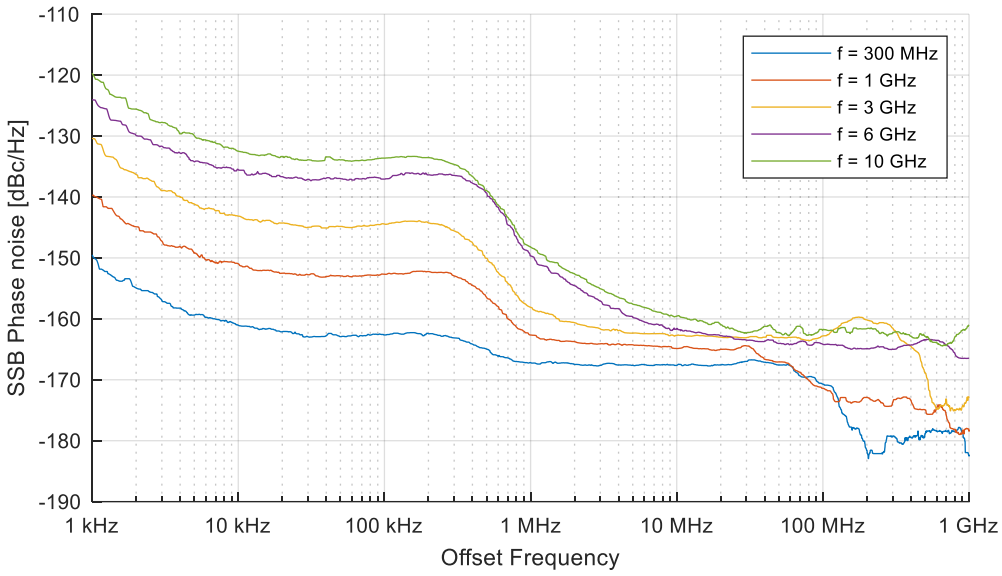

Figure 14 R&S®SMA100B (with B711) SSB phase noise (meas.)

Figure 14 highlights the outstanding phase noise characteristic of the R&S®SMA100B measured with the R&S®FSWP50.

As explained in section 3.3, the jitter is mostly dominated by the wideband phase noise. As noise measurements for large bandwidths can be time consuming and difficult to calculate with in early design stages, section 3.6 introduced the approximation of a constant wideband phase noise. Inspecting the R&S®SMA100B's SSB phase noise performance, it becomes clear that the phase noise is not constant for large offsets either. Thus, to obtain accurate phase noise and jitter figures, a phase noise measurement for the full band in question can often be necessary.

Nevertheless, wideband approximations are still possible in many cases. Those approximations estimate the wideband noise to be constant starting at a given frequency offset. To find this offset, a compromise has to be found. If the offset frequency is chosen too low, the approximated noise density is unreasonably high. If on the other hand the offset frequency is chosen too high, the approximated noise density might be too low of an estimate. In Figure 14 above, the phase noise density at 10 MHz is chosen as a compromise between those two aspects. For most of the carrier frequencies and offset frequencies, the noise density at 10 MHz serves as an upper bound, while still being on the lower side of the slope after 1 MHz. The quality of the approximation always depends on the relevant carrier frequencies and clock bands.

To provide guidance for when the constant wideband phase noise approximation might be feasible, Figure 15 compares the SSB phase noise density at 10 MHz to the peak phase noise at offsets larger than 10 MHz and to the phase noise power average in the upper band between 10 MHz and 1 GHz away from the carrier.

The figure shows, that for most applications, the phase noise density at 10 MHz is a reliable upper bound for the wideband phase noise. However, the figure also shows that for a few carrier frequencies, the approximation obtained from the phase noise at 10 MHz might be a little low for an upper bound, as it is the case for a carrier frequency of 5.5 GHz for example. For carrier frequencies above 10 GHz, the phase noise density at 100 MHz is a viable candidate for the wideband performance evaluation as well.

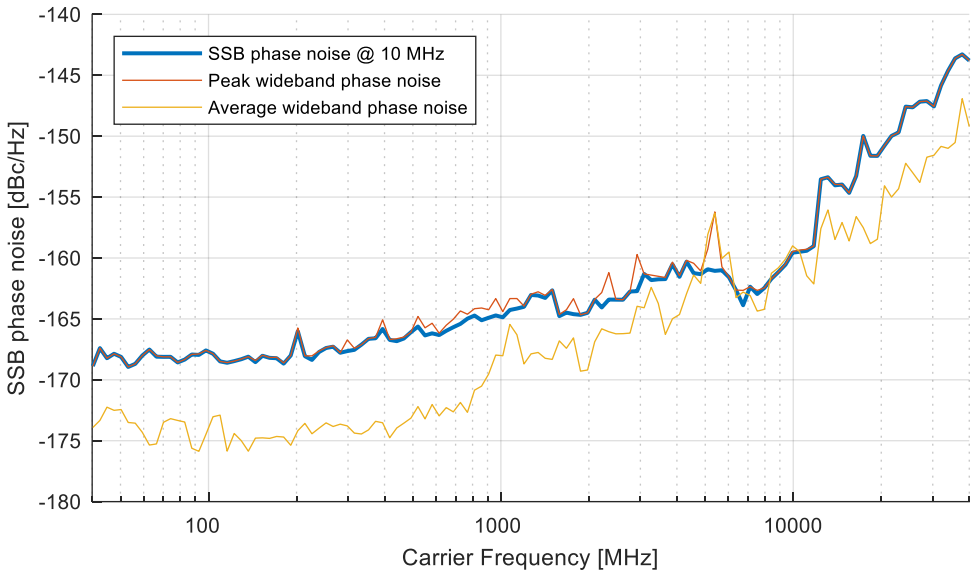

Figure 15 R&S®SMA100B (with B711) wideband phase noise (meas.)

For the clock synthesizer, the SSB phase noise power spectral density at 10 MHz can be a conservative approximation without estimating the noise performance too high as well, as visible in Figure 16 below.

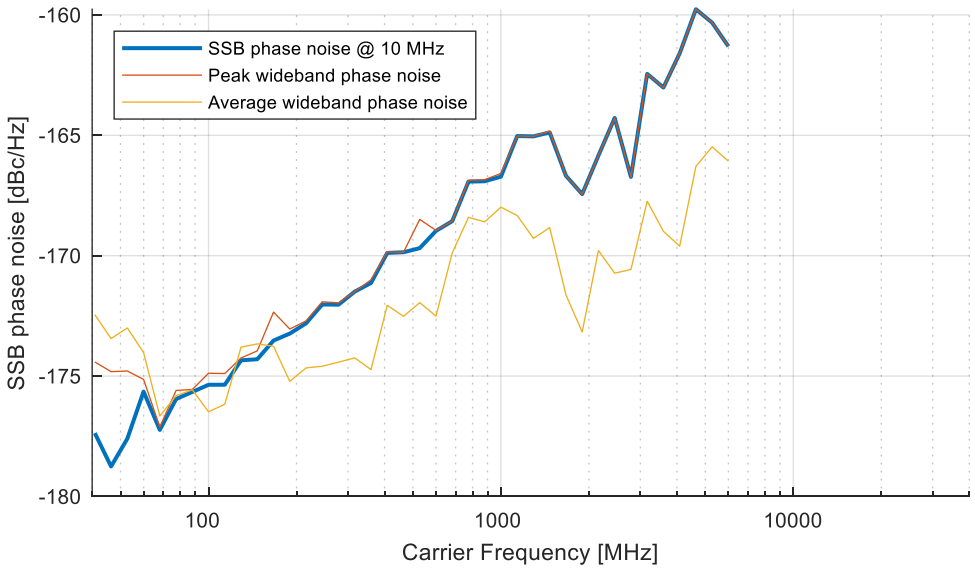

Figure 16 R&S®SMA100B (with B711) B29 Clock Synthesizer wideband phase noise (meas.)

In case of clock inputs with very large bandwidths, see the next section for a more in-depth depiction of the R&S®SMA100B's wideband noise characteristics.

4.2 Wideband Noise Performance

To discuss the wideband noise performance of a signal generator, a distinction must be made between wideband phase noise, wideband amplitude noise and overall wideband noise, which is the sum of both.

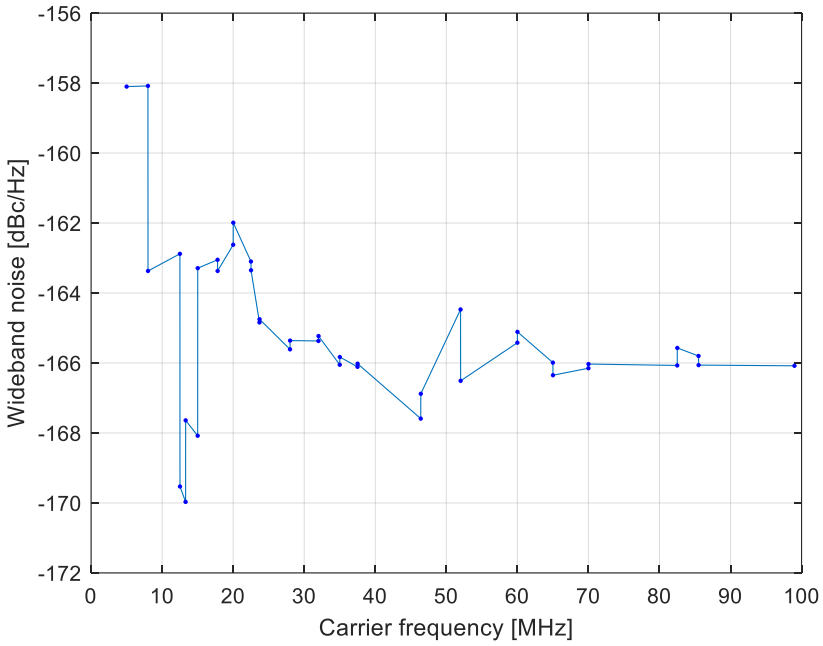

Figure 17 Measured wideband noise at 10% (of carrier frequency) offset and 10 dBm of an R&S®SMA100B with B711

Figure 17 shows measured wideband noise for carrier frequencies up to approximately 100 MHz. The R&S®SMA100B datasheet contains plots showing measured wideband noise for higher carrier frequencies.

As described in the previous section, the noise spectral density for large offsets may deviate from the wideband noise specification at a given offset. This section contains measurements of the noise distribution over large offset frequency ranges.

Usually, for large offsets one assumes that amplitude and phase noise contribute equally to the overall noise. Therefore, the wideband phase noise is normally 3 dB lower than the overall wideband noise.

As the R&S®SMA100B has different subassemblies for the frequency ranges 8 kHz to 6 GHz, 6 GHz to 20 GHz and 20 GHz to 40 GHz, it is advantageous to evaluate the wideband noise performance for every board each to observe the different behaviors in the respective bands. Due to the band-pass behavior of each of those subassemblies, they do not produce significant noise energy in frequency regions outside of their respective operating ranges.

For this, we show an R&S®SMA100B's generator noise spectral density for selected carriers as well as the specified wideband noise power spectral density from the datasheet. The appendix will show families of curves for the different frequency ranges for additional carrier frequencies. In the plots below, the carrier frequency as well as both noise spectral densities are shown as in Figure 18. The vertical line represents the carrier frequency with a small horizontal bar indicating the specified wideband noise at an offset of 10 MHz to 40 MHz depending on the carrier frequency. The measured noise power spectral density is plotted in the same color in dBc/Hz vs. the measured frequency.

Thanks to the R&S®SMA100B's excellent noise performance, the measured power spectral densities are far below -150 dBc/Hz, often by large margins. This also means, that the measured noise power spectral densities can and most likely will contain contributions from the signal analyzer's noise and distortion, too. Furthermore, the wideband noise behavior of the R&S®SMA100B also depends on the hardware options built into the signal generator, as different RF modules and chains may have different frequency responses, noise figures and nonlinearities.

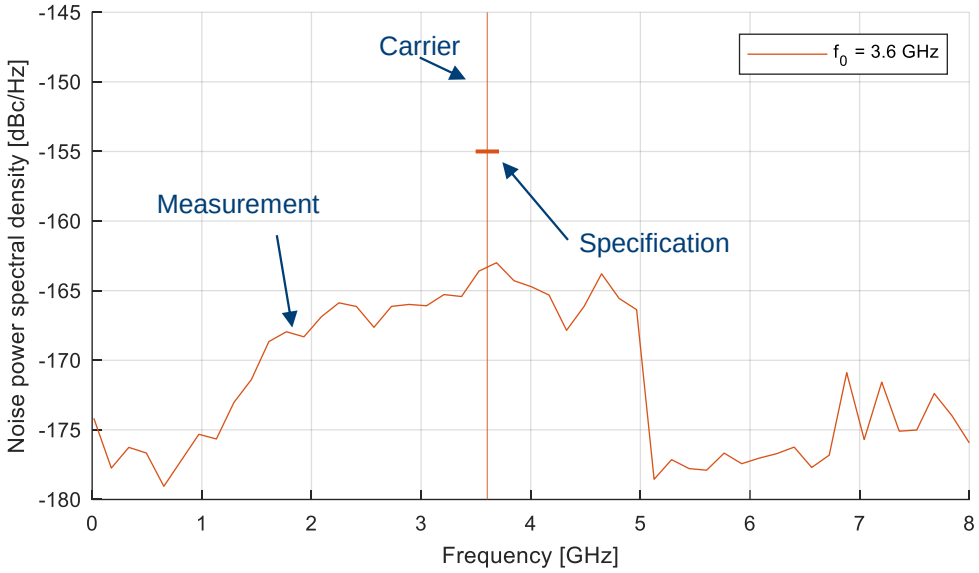

Figure 18 Example noise characteristic of an R&S®SMA100B (with B711) for a carrier of 3.6 GHz and an output level of 10 dBm (meas.)

Figure 19 demonstrates the wideband noise characteristics for carrier frequencies chosen arbitrarily throughout the different sub-paths in the 8 kHz to 6 GHz range. For each carrier frequency, the carrier, its measured noise power spectral density as well as the wideband noise specification is visible.

The measurement shows, that typically the actual wideband noise is neither flat nor constant. Often, it is also not symmetric around the carrier and in many cases the noise power spectral density will rise above values actually measured at 10 MHz to 40 MHz around the carrier for the phase noise plots. Although the measured noise at 10 MHz or 40 MHz is always below the instrument's specified maximum noise level at this offset, it might be possible that at large offsets for some carrier frequencies, the noise level is above its value at the specified frequency offset. This depends heavily on the frequency response of the RF chain and thus on the carrier frequency. Using the specified wideband noise as an upper bound for the whole bandwidth of interest, one obtains a safe upper bound for the integrated noise, as in many cases the noise power spectral density is 10 dB to 20 dB below the specification.

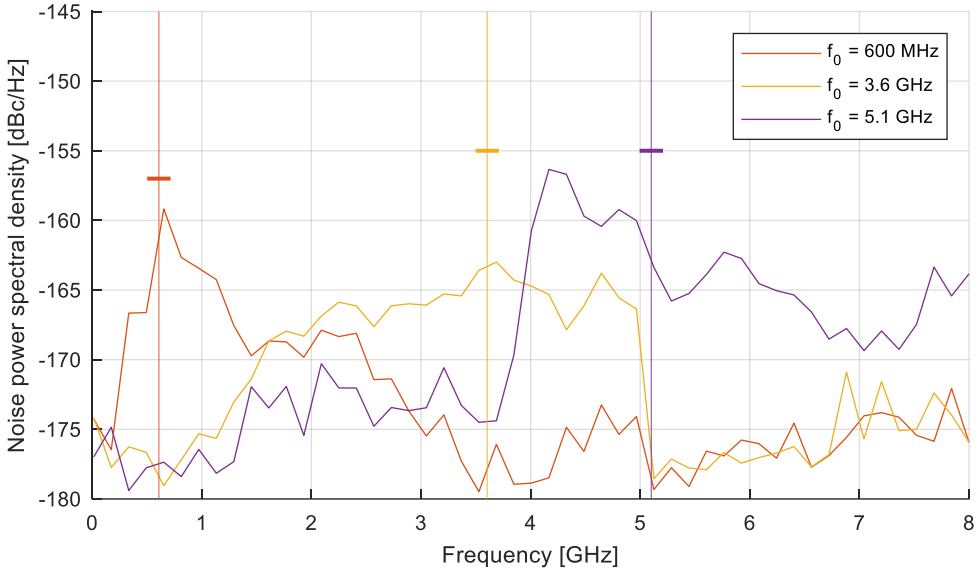

Figure 19 Wideband noise characteristic of an R&S®SMA100B (with B711) in the 8 kHz to 6 GHz range at an output level of 10 dBm (meas.)

The same characteristic for the 6 GHz to 20 GHz range can be seen in Figure 20. As in the range up to 6 GHz, the noise power spectral density usually is neither constant over the frequency, nor symmetric around the carrier. Again, using the specified wideband noise at the given offsets provides a conservative upper bound for the integrated noise for the same reasons. The increased noise at roughly 4 GHz to 6 GHz from Figure 19 does not appear for carrier frequencies above 6 GHz. As those carriers are created by different subassemblies, they also exhibit different noise characteristics. All RF chains have approximately passband behavior. They do not produce a significantly higher noise density in frequency bands of other RF chains than shown in the figures at the band edges. For Figure 20, this means for example that the noise power spectral density of carriers between 6 GHz and 20 GHz measured at frequencies below 4 GHz stay well below -170 dBc/Hz.

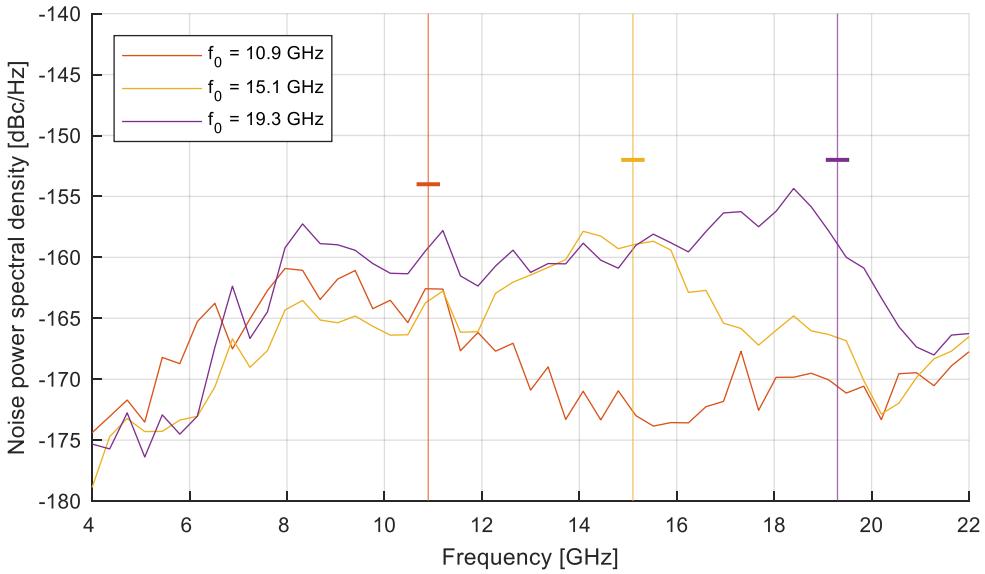

Figure 20 Wideband noise characteristic of an R&S®SMA100B (with B711) in the 6 GHz to 20 GHz range at an output level of 10 dBm (meas.)

For frequencies above 20 GHz, in Figure 21 a wideband noise behavior as expected can be seen. The noise power spectral density directly around the carrier is at its maximum, although typically still 5 to 10 dB below the 40 MHz offset specification. At offsets >2 GHz, the noise often reaches its wideband level at approximately 5 to 10 dB lower again. In this frequency range, the assumption of flat and constant wideband noise power spectral density allows for conservative upper bounds of the integrated noise. Also for the carrier frequencies where this is not the case, as for example for the 20 GHz curve, the noise characteristic still allows flat and constant wideband noise assumptions.

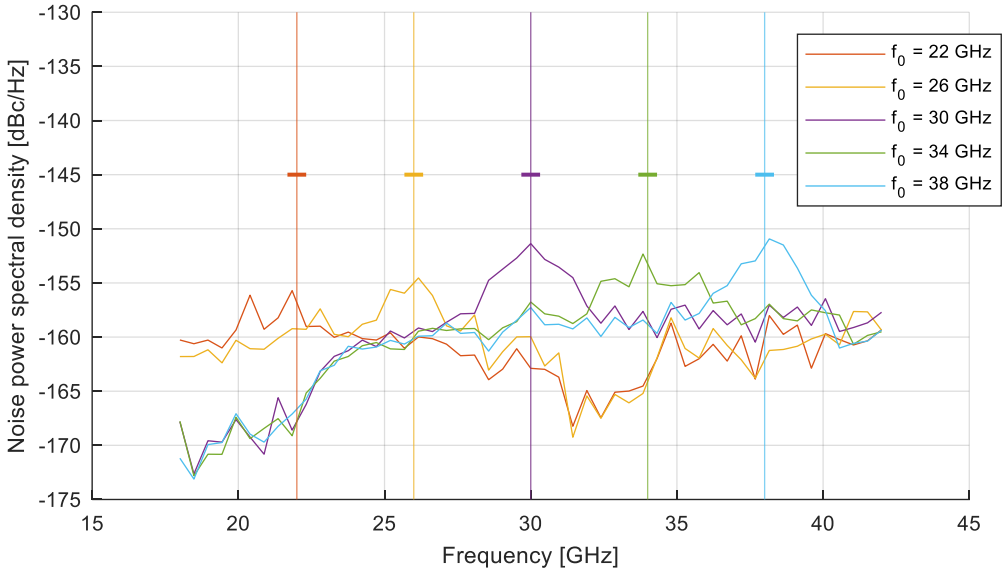

Figure 21 Wideband noise characteristic of an R&S®SMA100B (with B711) in the 20 GHz to 40 GHz range at an output level of 10 dBm (meas.)

Finally, Figure 22 depicts the wideband noise characteristic of the B29 Clock Synthesizer.

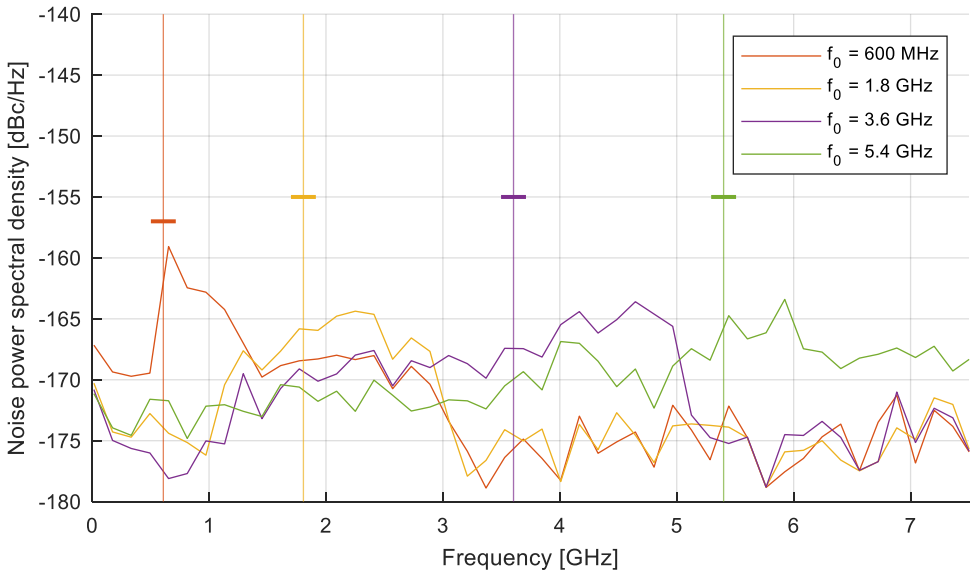

Figure 22 Wideband noise characteristic of an R&S®SMA100B (with B711) B29 Clock Synthesizer for a single-ended sine with power 10 dBm (meas.)

All measurements clearly show different characteristics for different sub-paths. To help a rough overview over the observable characteristics and the variations therein, more measurements are provided in the appendix.

The measurement results presented in this chapter are not only relevant for wideband noise considerations at the analog input. Assuming that for large offsets, the phase noise is 3 dB below the overall noise, the noise characteristics are also relevant when estimating SNR degradations due to jitter at the clock input. For large clock bandwidths, both sidebands are relevant and should be considered individually instead of just assuming symmetry around the carrier.

4.3 Jitter and SNR Performance of the R&S®SMA100B as a Clock Source

Figure 23 and Figure 24 show the RMS jitter derived from phase noise measurements for the two clock bandwidths of 20 MHz and 80 MHz for the R&S®SMA100B and its clock synthesizer respectively. Although the phase noise decreases for decreasing frequencies, the RMS jitter rises for decreasing frequencies.

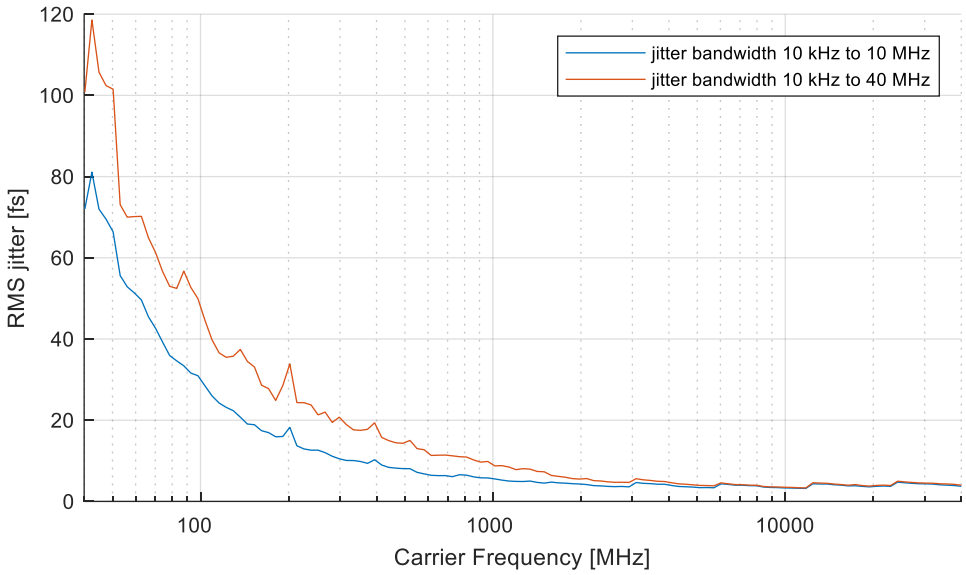

Figure 23 RMS jitter vs. clock frequency for the RF output of an R&S®SMA100B (with B711) (meas.)

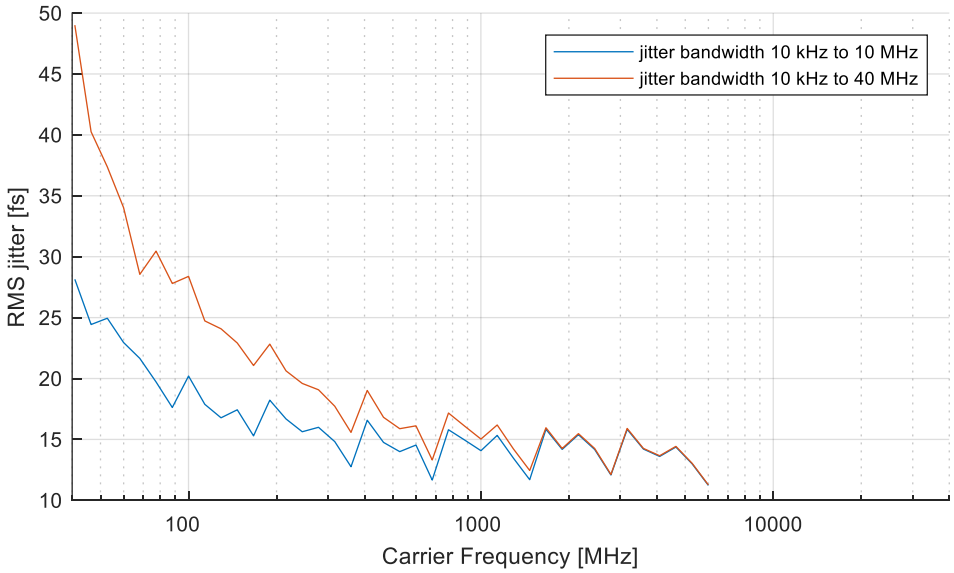

Figure 24 RMS jitter vs. clock frequency for an R&S®SMA100B (with B711) B29 Clock Synthesizer (meas.)

While the clock synthesizer's phase noise and jitter are inferior to the main synthesizer's performance for high frequencies, the B29 clock synthesizer is clearly the better choice for narrow-band clock inputs with clock frequencies not rising above a few hundred MHz. In this region, the clock synthesizer shows largely improved jitter performances.

The following figure shows the SNR contribution due to clock jitter derived from the RMS jitter as shown above in Figure 23 using equation (8). The SNR is shown vs. the clock frequency for three different analog input frequencies (10 MHz, 100MHz and 1 GHz) and for clock bandwidths of 20 MHz and 80 MHz.

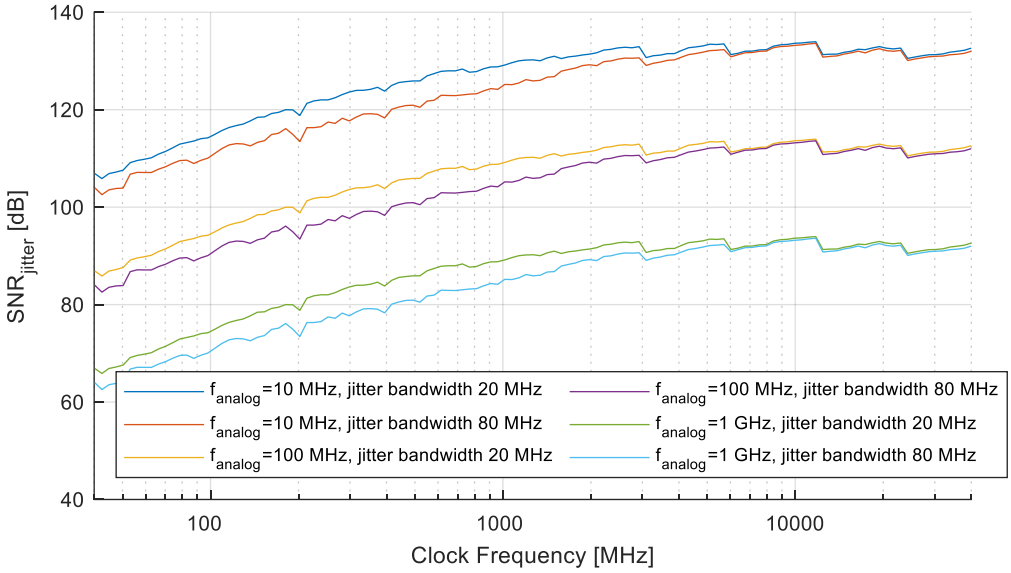

Figure 25 SNR contribution from clock jitter vs clock frequency and analog input frequency for an R&S®SMA100B (with B711) (meas.)

The B29 clock synthesizer's performance, which is depicted in Figure 26, again exhibits similar behavior as when comparing the RMS jitter in Figure 23 and Figure 24 above.

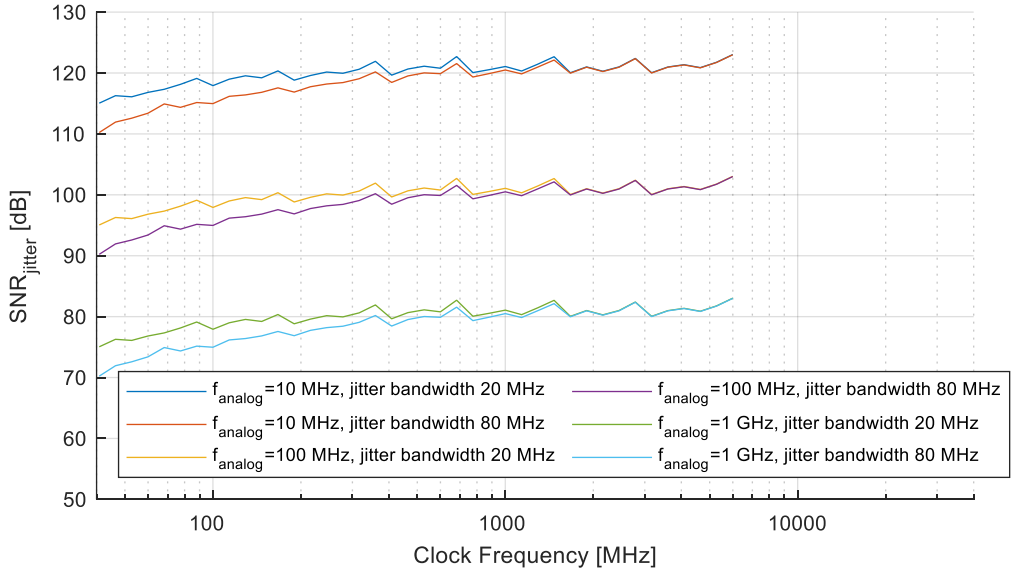

Figure 26 SNR contribution from clock jitter vs clock frequency and analog input frequency for an R&S®SMA100B (with B711) B29 Clock Synthesizer (meas.)

4.4 SNR Performance from wideband approximations of the R&S®SMA100B as a Clock Source

In many applications, the relevant clock bandwidth is much higher than the 20 MHz or 80 MHz used for SNR calculation in the figure above. For such wideband applications, the wideband phase noise of the clock source must be considered for SNR calculation as shown in section 3.6. Equation (19), which we derived there, describes the relation between wideband phase noise, clock bandwidth, clock and signal frequency and SNR. It is repeated here for clarity:

$$SNR_{jitter,clk} \gtrsim -BBNoise_{clk} - 10\log_{10}(BW_{clk}) + 3dB - 20\log_{10}\left(\frac{f_{analog}}{f_{clk}}\right)$$

The following diagram provides SNR characteristic vs. clock bandwidth for various wideband phase noise power levels and under the assumptions that the wideband phase noise is constant and that the analog signal frequency is equal to the clock rate.

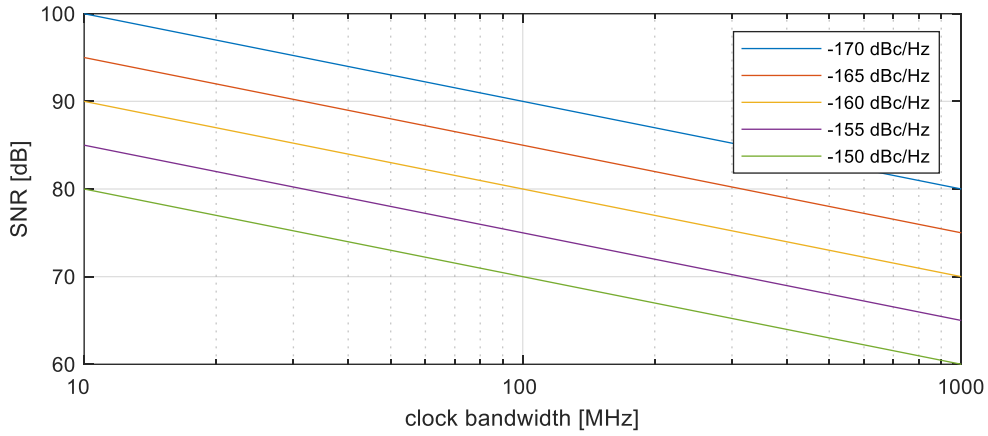

Figure 27 SNR vs. clock frequency bandwidth and wideband phase noise, $f_{analog} = f_{clk}$

Knowing the implemented clock bandwidth and the estimated wideband phase noise performance of the implemented clock source, the SNR contribution due to clock jitter can be estimated using Figure 27.

If the SNR for different analog input frequencies is needed, it is required to correct the values taken from Figure 27 using the factor $\frac{f_{analog}}{f_{clk}}$.

Example: A 14-bit ADC running at a clock rate of 200 MSPS and an analog input frequency of 100 MHz is specified with a max. SNR of 73 dB (see Figure 8). With a clock bandwidth of 500 MHz and a wideband phase noise from the clock source of -160 dBc/Hz, Figure 27 yields an SNR value of 73 dB. Since the analog input frequency at the ADC is half the clock rate, according to equation (21), a correction value of 6 dB must be added, resulting in an SNR contribution from the clock source of 79 dB. According to equation (16) and Figure 28 below, the total SNR performance of the ADC is reduced – as a result of the non-ideal clock source – by 1 dB to 72 dB. Improving the wideband phase noise performance of the clock source by 5 dB would reduce this SNR deterioration to 0.33 dB. The same SNR improvement could be achieved by reducing the clock bandwidth from 500 MHz to 155 MHz.

The SNR deterioration due to the addition of two SNR contributors is graphically illustrated in Figure 28.

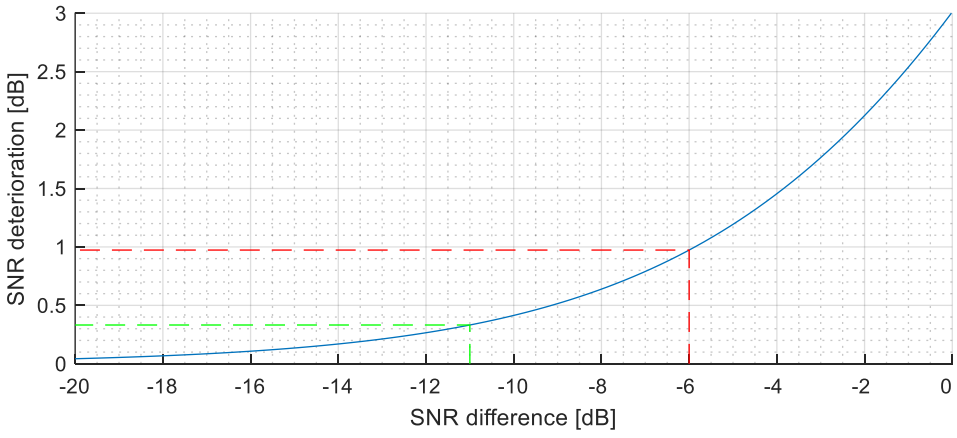

Figure 28 SNR deterioration vs. SNR difference of two SNR contributions

The dotted red lines show an SNR reduction of 1 dB if the difference between the two contributors is 6 dB. The dotted green lines show an SNR impairment of 0.33 dB for a difference of 11 dB (see example above).

Figure 29 depicts approximated as well as calculated estimated SNR contribution from the R&S®SMA100B as a clock source. For each clock rate, the figure shows the SNR calculated from the measured and integrated phase noise as well as the SNR calculated from the wideband phase noise approximation. For the wideband approximation, equation (19) is used to calculate SNR values again. The analog input frequency is equal to the clock rate for these calculations.

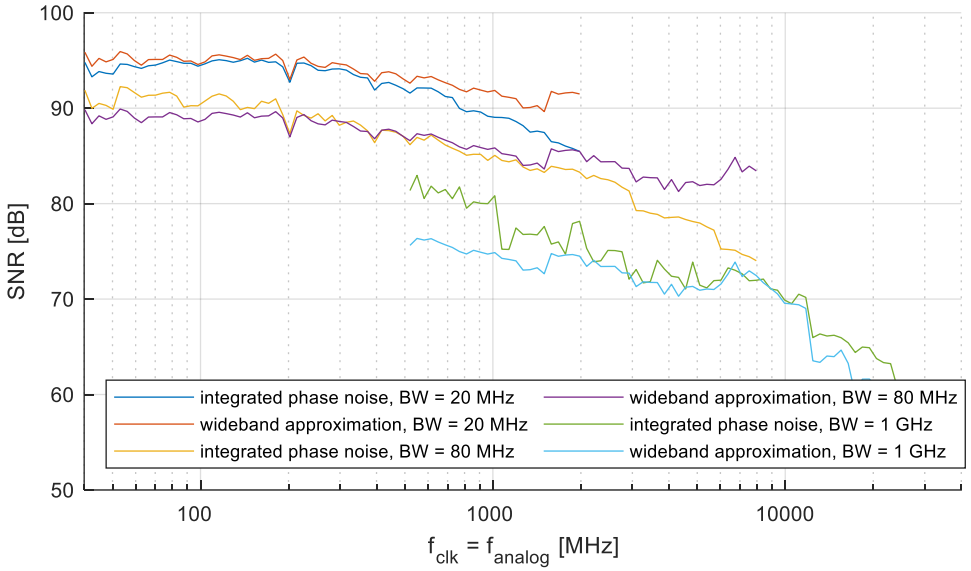

Figure 29 SNR vs. clock rate and clock bandwidth from constant wideband phase noise for an R&S®SMA100B (with B711) (meas.)

The figure shows the SNR contributions from clock jitter calculated from the measured phase noise power spectral density as well as calculated from the wideband phase noise level and confirms the claim from section 3.3, that for large bandwidths the wideband phase noise performance dominates the jitter. For small bandwidths, the phase noise close to the carrier is non-negligible and worsens the actual SNR with respect to the approximation, though. Thus, the viability of using the wideband approximation should be evaluated with care when a small bandwidth of the clock path is expected. With increasing clock bandwidths, the wideband phase noise performance starts to dominate the jitter and the approximation becomes more conservative.

If the SNR for different analog input frequencies is needed, the relation between clock rate and f_{analog} must be considered by adding the correction value given from equation (21) to the SNR values from Figure 29. Calculating the SNR value for a different clock bandwidth while still approximating the phase noise as constant is possible by correcting the SNR value from Figure 29 using the following equation

$$SNR_{BW2} = SNR_{BW1} - 10\log_{10}\left(\frac{BW2}{BW1}\right) \tag{25}$$

Example: If the clock bandwidth reduces from 1 GHz to 500 MHz, the SNR will improve by 3 dB. Inversely, if the clock bandwidth increases from 100 MHz to 200 MHz, the SNR will deteriorate by 3 dB.

4.5 SNR Performance of the R&S®SMA100B as Analog Source

The SNR contribution from the R&S®SMA100B as an analog signal source is usually dominated by the signal generator's wideband noise in the relevant frequency bands. A detailed depiction of the R&S®SMA100B's wideband noise performance was presented in section 4.2.

4.6 Non-Harmonics

4.6.1 SFDR and SNR Due to Non-Harmonics

The SFDR performance of a signal generator is normally dominated by its harmonic distortion since the level of the harmonics is much higher than the level of non-harmonic spurious.

However, by using adequate filtering at the generator's output, the harmonic signal components can be suppressed effectively and only non-harmonic spurious will then contribute to the signal generator's SFDR performance. Those spurs are hard to find as usually their frequencies are unknown and they appear only at discrete frequencies with comparatively low amplitudes. Therefore, we will characterize spurs using the maximum levels specified in the datasheet.

The SFDR contribution for a spur that is present at the analog signal input of an ADC with the specified spur performances of the R&S®SMA100B as well as the R&S®SMA100A is shown in Figure 30 below.

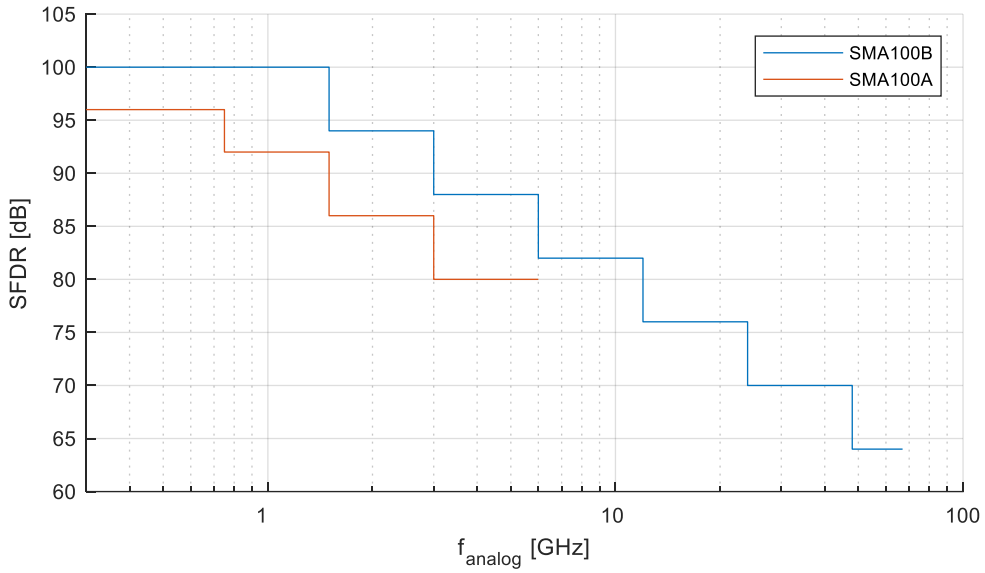

Figure 30 SFDR performance of the R&S®SMA100 due to non-harmonic spurious versus analog signal frequency

Figure 30 is also valid for the clock input if the analog signal frequency is equal to the clock rate. Otherwise, the SFDR must be corrected just like the phase noise using equation (21).

The specification above is also helpful for determining the SNR due to non-harmonics. The SNR does not distinguish between amplitude modulation and phase modulation. Therefore, the noise energy of each spur is directly visible from its level in the frequency spectrum, regardless if the spur is a single non-harmonic or a pair of spurs. This means, the specified worst-case SFDR also provides the designer with a worst-case spur level for each spur. In the case there are multiple spurs or spur-pairs with the same amplitude, the SNR has to be reduced by 3 dB, 4.7 dB, 6 dB, 7 dB and so on respectively for each additional spur.

4.6.2 Jitter Contribution of Non-Harmonics

The following diagram shows the RMS jitter contribution due to a single non-harmonic spur. The typical RMS jitter performance of the R&S®SMA100B, incl. option B711 due to phase noise for 80 MHz bandwidth, is also plotted in Figure 31 in order to estimate the spur level at which the jitter due to the spur is higher than the jitter due to phase noise. The purple line depicts the RMS jitter contribution of a non-harmonic spur equal to the specified performance of the R&S®SMA100B with option B711. The figure also includes the phase noise contributed jitter performance of the R&S®SMA100A for comparison.

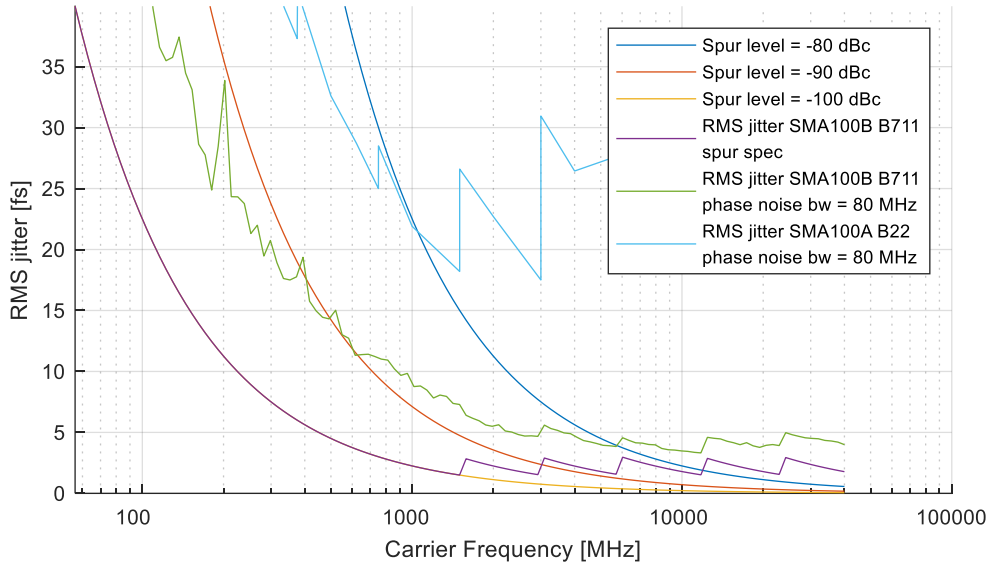

Figure 31 RMS jitter contribution due to non-harmonic spurs and measured phase noise performance of an R&S®SMA100B

Clearly, the jitter performance of the R&S®SMA100B is dominated by its phase noise performance instead of spurious performance over the complete frequency range. The RMS jitter contribution due to phase noise is considerably higher than the maximum possible RMS jitter contribution from non-harmonics based on the spurious specification. Keep in mind though, that for more than one spur, their jitter contributions need to be added as in Equation (15).

4.7 Harmonics

The harmonic distortion for the second harmonic of an R&S®SMA100B (for carrier frequencies > 10 MHz) is depicted in Figure 32 for an output level of +10 dBm. As the R&S®SMA100B produces very low harmonics, the measurement result also includes harmonic contributions and other artifacts from the used R&S®FSW85. The measured intrinsic noise floor of the measuring instrument is shown in the figure as well. This noise floor is measured at two times the set carrier frequency and shown in dBc for comparability. The harmonics with higher orders or higher frequencies are normally far below these values.

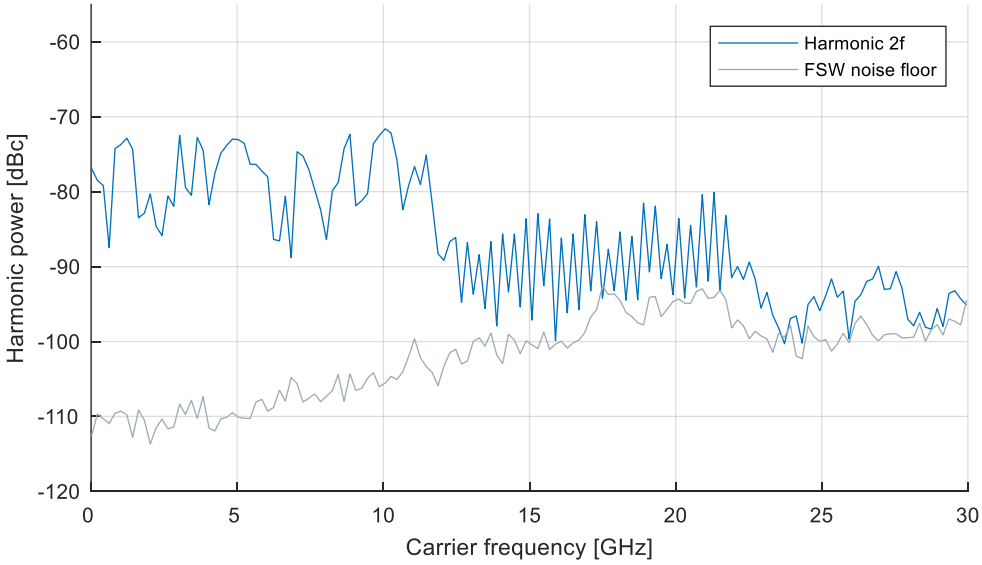

Figure 32 Second harmonics at +10 dBm vs. carrier frequency for an R&S®SMA100B (meas.) for carrier frequencies > 10 MHz

The harmonic distortion of a signal generator varies versus the set output level and frequency and is dominated by the harmonic performance and the signal level at the RF output stage, which is followed by an attenuation stage. Contrary to the R&S®SMA100A, the R&S®SMA100B automatically fine-tunes gain and attenuation in order to achieve a good overall performance at the signal output. There is no necessity for the user to adjust attenuation settings when aiming for low harmonic distortion or a high SNR.

5 Example SNR Calculations for typical ADC Test Setups

This chapter provides some example SNR calculations for the R&S®SMA100B as a clock and analog source using the characteristics shown in the previous chapters.

When sourcing for a signal generator, the following factors must be taken into account:

- The generator's contribution to the wideband noise and close-in noise should be negligible or should have only minimal effect on the SNR measurement procedure of the ADC.
- The generator's non-harmonic distortion products should be far below the distortion products of the ADC.
- Since the demands placed on a signal source may become higher in future challenges, the performance of a purchased generator should optionally already have enough margin to meet these future requirements.

5.1 ADC Test Setup with the R&S®SMA-B29 Clock Synthesizer

In general, signal sources for the analog and clock inputs are needed, as well as means for data analysis. For most ADCs, an evaluation board with a PC interface, e.g. USB, and the required software tools are available. Most ADC evaluation boards include some level shifters or signal transformers in order to convert a sine wave signal at the board input to the required signal for the analog or clock input of the DUT, e.g. a differential signal for analog input.

With the R&S®SMA100B it is also possible to combine analog input signal generator and sample clock generator in one device. Using the B29 option, the test setup is as simple as shown in Figure 33.

Figure 33 Simplified ADC test setup using the R&S®SMA-B29 clock synthesizer as clock source

If required, the clock synthesizer provides a differential output signal, thus eliminating the need for a balun at the ADC clock input.

The clock synthesizer output and the RF output differ from each other in frequency range and properties. As both outputs provide a high-grade signal purity, this setup is the perfect solution for many applications. However, especially applications with both signal and clock frequencies higher than 6 GHz may require using a second R&S®SMA100B.

5.2 ADC Test Setup with two R&S®SMA100B Signal Generators

Figure 34 depicts a test setup with two R&S®SMA100B signal generators.

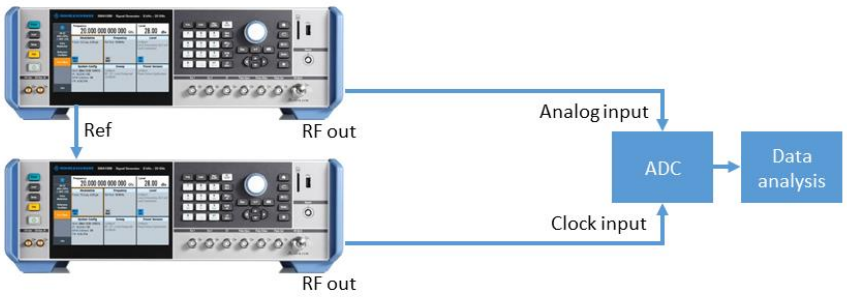

Figure 34 General ADC performance test setup

The RF output of one R&S®SMA100B serves the analog input of the ADC, and the RF output of the other R&S®SMA100B serves the clock input. If necessary, filters can be added to the signal paths to keep SNR contributions from signal impurities even lower. Both signal generators should be synchronized using a common reference signal. Thereby, the phase noise contributions of the used signal generators are reduced further.

5.3 Typical ADC Specifications

The table below lists some typical characteristics of discrete high-speed ADCs.

ADC	Resolution [bits]	Sample rate [MSPS]	SNR [dBFS]	SFDR [dBFS]
Analog Devices AD9213	12	10250	51	65
Texas Instruments ADC14C105	14	105	90	82
Maxim Integrated MAX19588	16	100	79	98
Analog Devices LTC2270	16	20	84	99
Texas Instruments ADC12DJ5200RF	12	10400	56.7	78

5.4 Example SNR Calculation for the R&S®SMA100B

In this example, two R&S®SMA100B generators with B711 are used as a clock source and analog source for an ADC test set, applying a 10 MHz sine signal at the analog input. The ADC under consideration has an SNR of approximately 80 dB. The SNR of the test setup should be far below this value.

The following table lists the frequencies and bandwidths for the clock signal and the analog signal used for the calculations. Note that the given analog and clock bandwidths are a result of bandwidth limitations in the DUT or filters that are inserted between the SMA100B's outputs and the ADC's inputs.

Clock Frequency	Clock Bandwidth	Analog Frequency	Analog Bandwidth
100 MHz	300 MHz	10 MHz	25 MHz

Step 1: Calculation of SNR due to jitter/phase noise of clock source

Using the R&S®SMA100B's wideband noise specification at 100 MHz (-157 dBc/Hz) and equation (19) (see also section 4.4), SNR_{clk} can be approximated as

$$SNR_{clk} =$$

$$-BBNoise_{clk} - 10\log_{10}(BW_{clk})\ \text{dB} + 3\ dB - 20\log_{10}\frac{f_{analog}}{f_{clk}}\ \text{dB} =$$

$$157\ \text{dB} - 10\log_{10}(300\ \text{MHz}/1\ \text{Hz})\ \text{dB} + 3\ \text{dB} - 20\log_{10}\frac{10\ MHz}{100\ MHz}\ \text{dB} =$$

$$157\ \text{dB} - 84.77\ \text{dB} + 3\ \text{dB} + 20\ \text{dB} \approx 95\ \text{dB}$$

This shows that there is still a big margin to the expected performance of the DUT.

Using the measured performance of an R&S®SMA100B instead of its specification indicates that there might be an even bigger margin in reality. Figure 29 shows the measured SNR performance of an R&S®SMA100B used as a clock source for an ADC test set. For a clock rate of 100 MHz, an analog signal frequency of 100 MHz and a clock bandwidth of 80 MHz, an SNR value of roughly 90 dB can be read from the diagram. Then, the lower analog input frequency of 10 MHz must be considered, and the SNR value must be corrected using equation (21). Also, the SNR must be corrected due to the higher clock bandwidth of 300 MHz by using equation (25).

Estimating SNR_{clk} based on measured performance of an R&S®SMA100B yields

$$SNR_{clk} = SNR_{clk,80MHz,BW100MHz} - 20\log_{10}\left(\frac{10\ \text{MHz}}{100\ \text{MHz}}\right)\ \text{dB} - 10\log_{10}\left(\frac{300\ \text{MHz}}{80\ \text{MHz}}\right)\ \text{dB} =$$

$$90\ \text{dB} + 20\ \text{dB} - 5.74\ \text{dB} \approx 104\ \text{dB}$$

and indicates an even bigger margin.

Step 2: Calculation of SNR due to non-harmonics of clock source

It is assumed that the clock signal includes one symmetrical pair of non-harmonic spurs with the maximum specified level at 100 MHz, which is -100 dBc. Evaluating equation (23) yields

$$SNR_{spur,clk} = \ -a_{spur} - 3\ \text{dB} - 20\log\left(\frac{f_{analog}}{f_{clk}}\right)\text{dB} = 100\ \text{dB} - 3\ \text{dB} - 20\log_{10}\left(\frac{10\ MHz}{100\ MHz}\right)\text{dB} = 117\ \text{dB}$$

Step 3: Calculation of SNR due to wideband noise of analog source

Figure 17 shows the measured wideband noise performance of an R&S®SMA100B. For an analog signal frequency of 10 MHz, a value of -163 dBc/Hz can be read from the diagram. Together with the analog bandwidth of 25 MHz, the SNR contribution can be estimated according to equation (20) as

$$SNR_{analog} = -BBNoise - 10\log_{10}(25\ \text{MHz}/1\text{Hz})\ dB = 163\ \text{dB} - 74\ \text{dB} = 89\ \text{dB}$$

Using the R&S®SMA100B's specified value of -157 dBc/Hz at a frequency of 100 MHz, the resulting SNR contribution would be 83 dB.

Step 4: Calculation of SNR due to non-harmonics of analog source

It is assumed that the analog signal includes one symmetrical pair of non-harmonic spurs with the maximum specified level at 10 MHz, which is -100 dBc. According to equation (24), this yields an SNR contribution of 100 dB – 3 dB = 97 dB.

Step 5: Summary

Summing all SNR contributions, the SNR limitation of the test set is

$$SNR_{testset} = -10\log_{10}\left(10^{-\frac{104}{10}} + 10^{-\frac{117}{10}} + 10^{-\frac{89}{10}} + 10^{-\frac{97}{10}}\right) = 88.2\ \text{dB}$$

when considering the measured performance of an R&S®SMA100B, and 82.6 dB when using specified values.

This SNR estimation shows that a test set using two R&S®SMA100B generators as the clock source and the analog signal source has a margin of approximately 8 dB (estimated from measured values) or approximately 2.6 dB (based on specified values), respectively, from the considered ADC. With these margins, there is an SNR deterioration of roughly 0.6 dB (based on measured values) or roughly 2 dB (based on specified values), respectively, as can be seen in Figure 28.

If more precise knowledge of the test set performance is required, the relevant parameters can be measured for the particular instruments that are used. In general, further improvement of the test set performance can be achieved by using filters with lower bandwidths if necessary.

6 Summary

Testing the true performance of ADCs can place high requirements on the input signals. In this application note, background information on the influence of signal quality on the measurement results has been given. It has been shown that the outstanding signal purity of the R&S®SMA100B makes unveiling the true performance of an ADC much easier than it used to be.

7 Literature

[1] F. Maloberti, Data Converters, Springer US, 2007.

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[3] E. Bartolome, V. Mishra, G. Dutta and D. Smith, *Clocking High-Speed Data Converters, Texas Instruments application note,* Texas Instruments, 2005.

[4] American National Standards Institute, *T1.105 Synchronous optical networking.*

[5] B. Brannon, *Sampled Systems and the Effect of Clock Phase Noise and Jitter, Analog Devices application note AN-756,* Analog Devices, 2004.

[6] Analog Devices, Inc., *Data Sheet AD9445, 14-Bit, 125 MSPS ADC,* 2005.

[7] B. Brannon and R. Reeder, *Understanding High Speed ADC Testing and Evaluation, Analog Devices application note AN-835,* Analog Devices, 2006.

8 Ordering Information

Designation	Type	Order No.
RF and Microwave Signal Generator	R&S®SMA100B	1419.8888.02
Frequency Option 8 kHz to xx GHz	R&S®SMAB-B1xx	1420.yyyy.02
Ultra Low Phase Noise	R&S®SMAB-B711	1420.8020.02
Differential Clock Synthesizer, 3 GHz	R&S®SMAB-B29	1420.8088.02
Clock synthesizer frequency extension to 6 GHz	R&S®SMAB-K722	1420.9810.02

9 Appendix

9.1 Performance Data for the R&S®SMA100B with B711

9.1.1 Wideband Noise

As described previously in section 4.2, this appendix shows further noise power spectral density characteristics for different frequency bands to demonstrate variation over the carrier frequency.

For some carrier frequencies and generator configurations, the measured noise power spectral density at very large offsets from the carrier might surpass the wideband noise level specified in the datasheet for an offset of 10 MHz or 40 MHz. In this case, the affected offset frequencies usually cover only a very small portion of the bandwidth and lie far beyond the offsets at which the wideband noise level is specified. The noise power spectral density never surpasses the specified wideband noise level at the specified offset.

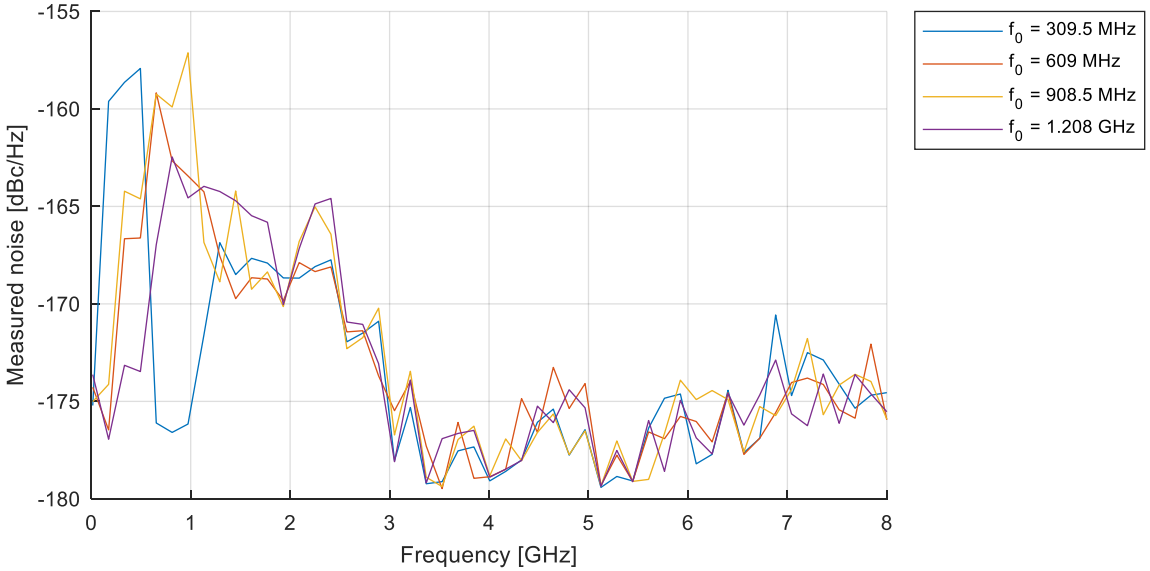

Figure 35 Noise PSD for multiple carrier frequencies with $f \leq 1.5$ GHz

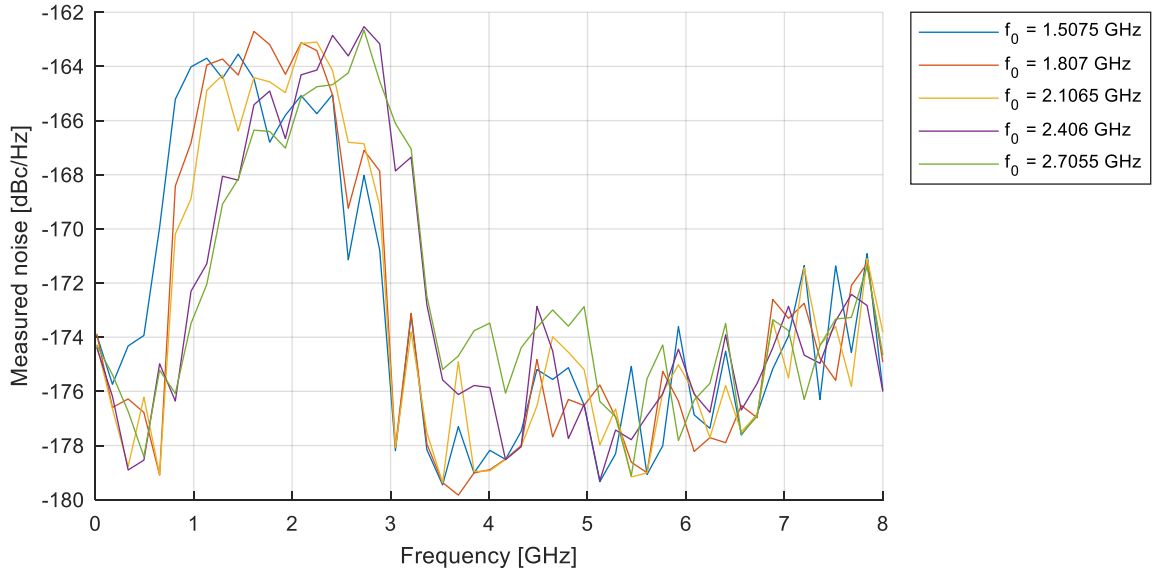

Figure 36 Noise PSD for multiple carrier frequencies with $1.5\ \mathrm{GHz} < f \leq 3\ \mathrm{GHz}$

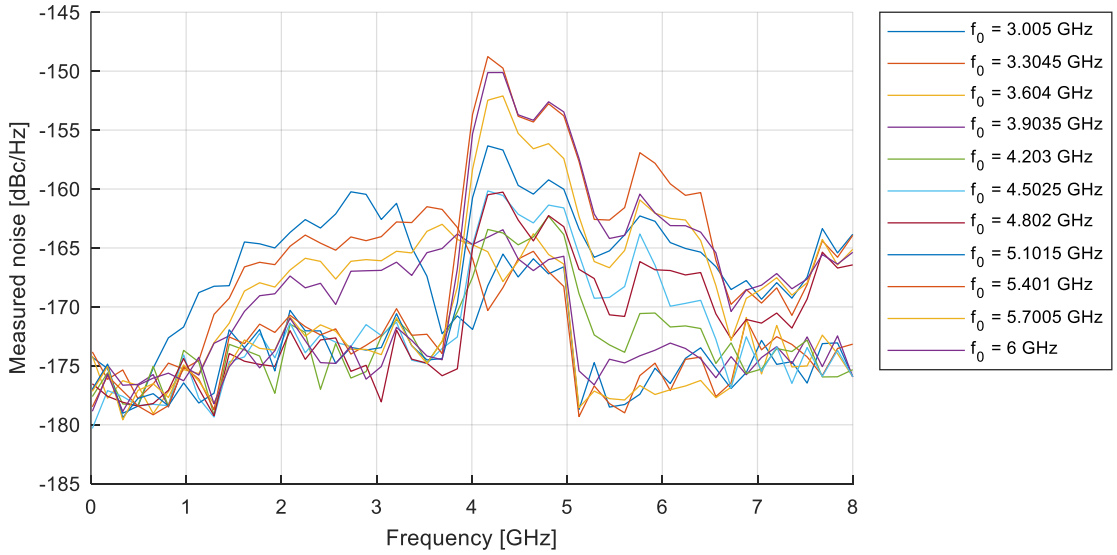

Figure 37 Noise PSD for multiple carrier frequencies with $3\ \mathrm{GHz} < f \leq 6\ \mathrm{GHz}$

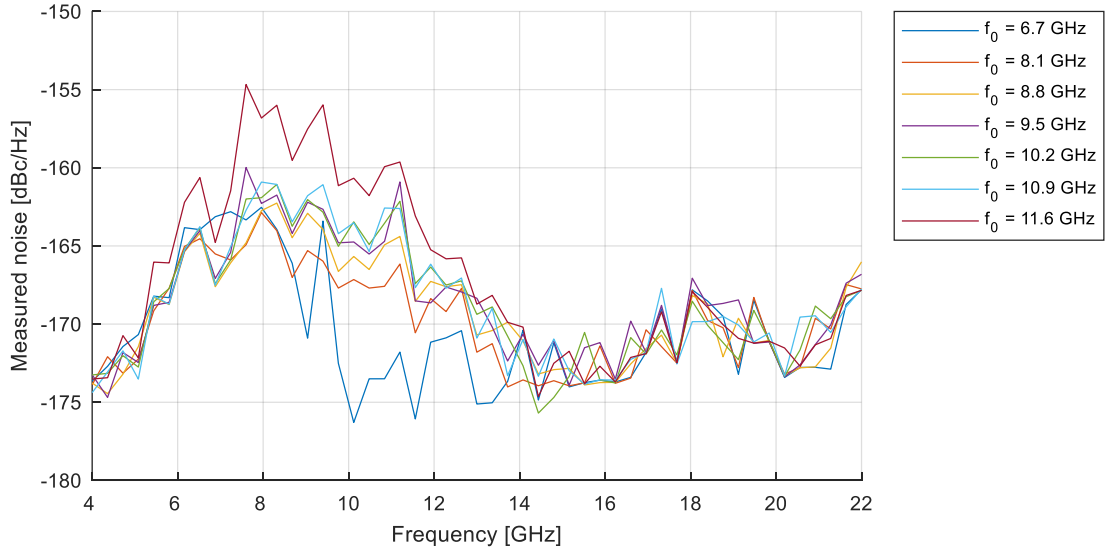

Figure 38 Noise PSD for multiple carrier frequencies with $6\ \mathrm{GHz} < f \leq 12\ \mathrm{GHz}$

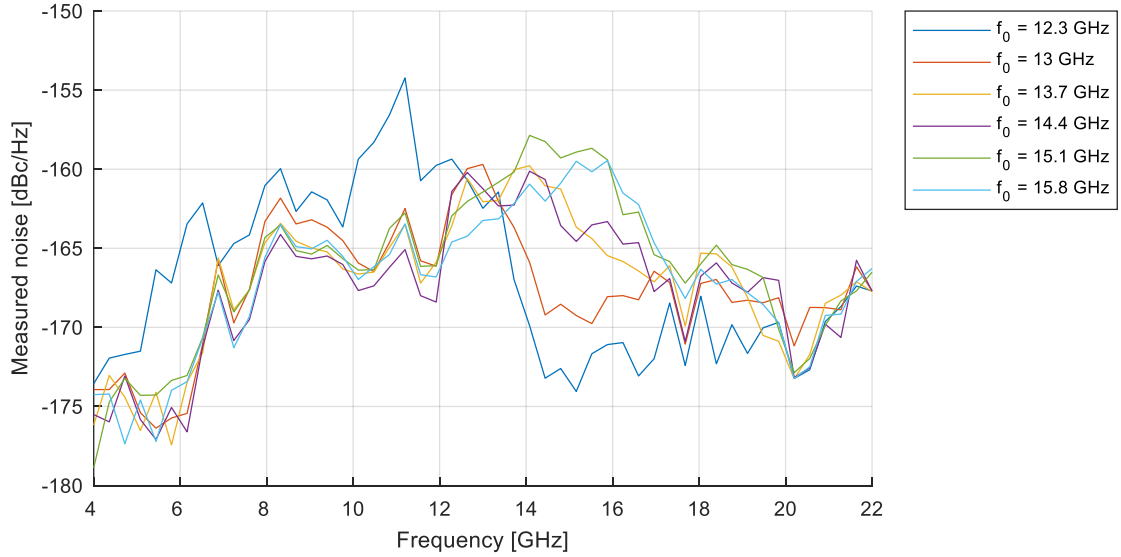

Figure 39 Noise PSD for multiple carrier frequencies with $12\ \mathrm{GHz} < f \leq 16\ \mathrm{GHz}$

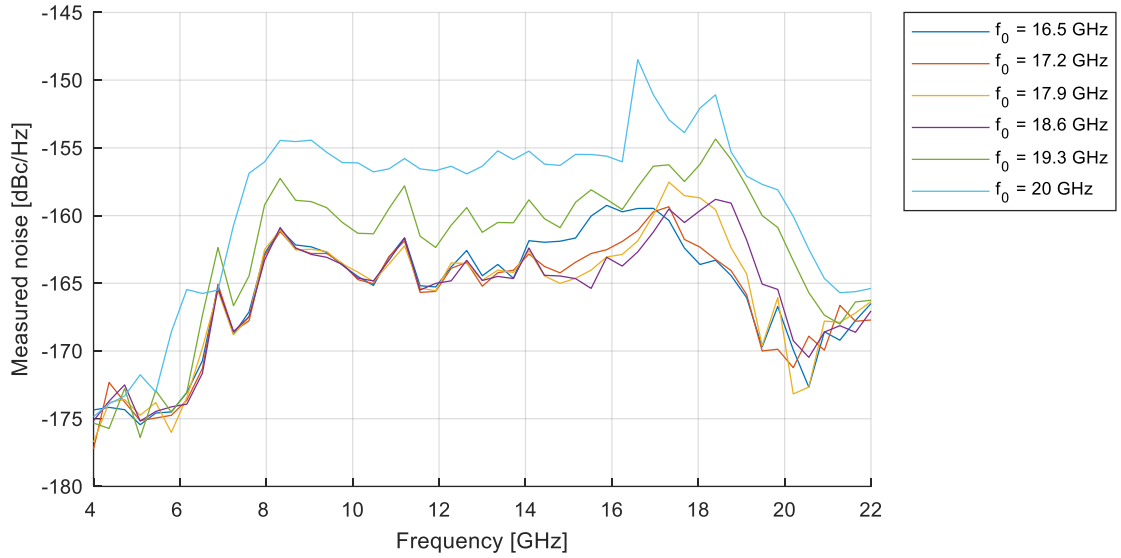

Figure 40 Noise PSD for multiple carrier frequencies with $16\ \mathrm{GHz} < f \leq 20\ \mathrm{GHz}$

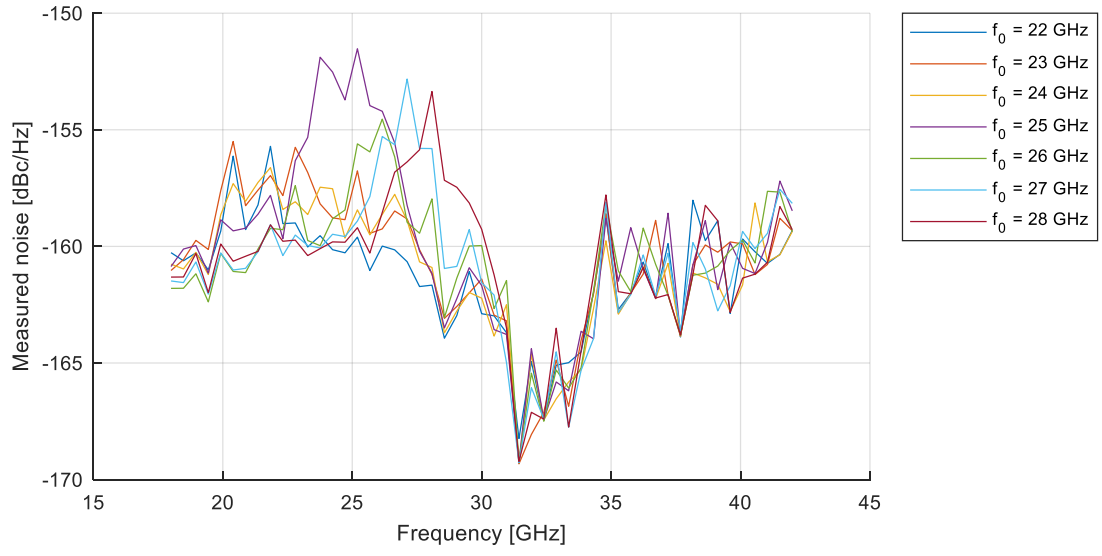

Figure 41 Noise PSD for multiple carrier frequencies with $20\ \mathrm{GHz} < f \leq 28\ \mathrm{GHz}$

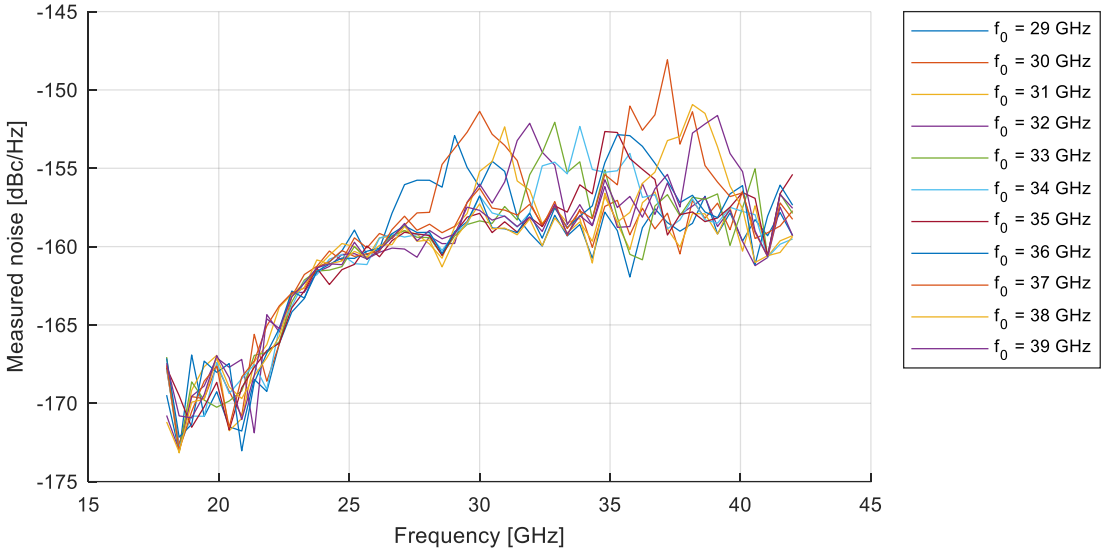

Figure 42 Noise PSD for multiple carrier frequencies with $28\ \mathrm{GHz} < f \leq 40\ \mathrm{GHz}$

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