# How to Run WCDMA BER/ BLER Tests Using R&S Vector Signal Generators Application Note

#### **Products:**

- | R&S<sup>®</sup>SMBV100A | R&S<sup>®</sup>SMU200A
- | R&S<sup>®</sup>SMJ100A

This application note shows how to run 3GPP WCDMA BER and BLER tests according to standard TS 25.141 with the Vector Signal Generators R&S<sup>®</sup>SMBV100A, R&S<sup>®</sup>SMJ100A, or R&S<sup>®</sup>SMU200A.

The description of hardware test setup is followed by detailed instructions on how to configure the R&S<sup>®</sup> generators and how to run a BER or BLER test step by step. Remote control commands for the generators are included, to simplify integrating the BER/BLER tests into your proprietary test suite.

The procedures described in this application note are independent of the type of Device Under Test. Only an external synchronisation signal is required as well as reference frequency input or output.



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### 1 Overview

This application note shows how to run BER and BLER tests according to standard TS 25.141 with the Vector Signal Generators R&S<sup>®</sup>SMBV100A, R&S<sup>®</sup>SMJ100A, or R&S<sup>®</sup>SMU200A on 3GPP WCDMA NodeBs.

A description of the recommended hardware test setup in chapter 2 is followed by detailed instructions on how to configure the R&S<sup>®</sup> generators (chapter 3). Remote control commands are included to simplify integrating the BER/BLER tests into your proprietary test suite. In chapter 4 you find instructions on how to run a BER or BLER test step by step.

Unlike User Equipment, NodeBs calculate the BER and the BLER internally or by means of an external device. The BER and BLER are not evaluated inside the tester; it only provides an uplink reference channel with PRBS data. This method is often called the "single ended BER / BLER test". User Equipment on the other hand provides an internal loop to send back the decoded receive data via the uplink: the calculation is done inside the tester. This method is called the "loopback BER / BLER test".

The single ended NodeB BER / BLER tests described here can be executed with either an R&S<sup>®</sup>SMBV100A, or an R&S<sup>®</sup>SMJ100A, or an R&S<sup>®</sup>SMU200A. To improve the readability, only a "signal generator" is mentioned in the following text. For the reminder of this application note, a reference to this signal generator could equally apply to an SMBV, an SMJ, or an SMU.

#### Benefits of the Rohde & Schwarz solution:

- Real-time test signals for 3GPP up- and downlink
- Additional White Gaussian Noise AWGN provided for receiver tests
- Remote control via IEEE488 and LAN
- Dual independent baseband and RF channels provided by SMU200A
- Dual baseband faders for optimum signal quality inside the SMU200A

The following abbreviations are used in this application note for R&S<sup>®</sup> test equipment:

- The R&S<sup>®</sup>SMBV100A Vector Signal Generator is referred to as SMBV.
- The R&S<sup>®</sup>SMJ100A Vector Signal Generator is referred to as SMJ.
- The R&S<sup>®</sup>SMU200A Vector Signal Generator is referred to as SMU.

# 2 BER / BLER Test Hardware Configuration

#### **Requirements:**

- Test controller (PC) with software to setup the Device Under Test (DUT), to run the test suite, and to generate and store the test protocols.
- Rohde & Schwarz<sup>®</sup> SMBV100A, SMJ100A, or SMU200A generator with the appropriate hardware and software options, see table 8\_1 on page 18.
- Power supply for the DUT.

The DUT shall provide:

- Sync pulse to synchronize up- and downlink. This could be a Start of Frame Number signal (SFN) which indicates when the frame counter wraps from 4095 to 0 or a Transmission Time Interval signal (TTI).
- 10 MHz reference input or output at the DUT. Some NodeBs can also use other frequencies, e.g. 19.2 MHz.



#### Hardware Setup:

Figure 2\_1: Hardware test setup for BER / BLER measurements

The DUT used in Figure 2\_1 that supports this methodology (single ended BER/BLER) is the picoChip WCDMA Femtocell reference design and development platform.

Note: A 19.2 MHz reference clock output could also be provided on this product.

More information for picoChip customers on configuring this reference design for BER/BLER testing is found on the site <u>https://support.picochip.com</u>.

#### Preparations:

- Measure the RF path loss (RF cable including attenuator) for the test frequencies.
- Connect the:
  - Antenna port of the DUT via a 30 dB attenuator to the generator RF output. This improves the impedance matching between generator and DUT increasing level accuracy.

Some base stations provide a DC bias at the RX connector to supply an external amplifier. Make sure that the bias is disabled, or use a DC blocking circuit between the DUT and signal generator.

- 10 MHz Reference input of the DUT to the REF OUT connector of the R&S<sup>®</sup> generator if DUT is set to external reference.
  If the DUT does not have the possibility to receive a reference input, connect the 10 MHz reference port of the DUT to the *REF IN* connector of the R&S<sup>®</sup> generator.
- Sync pulse output of the DUT to the TRIGGER1 input of the SMU and SMJ generators or to the TRIG input of the SMBV.
- Remote control cables between the Controller, the DUT and the R&S<sup>®</sup> generator if the generator shall be remote controlled. Use the IEEE488 or the LAN interface either.

# 3 Generator Configuration

#### Manual Operation:

- 1. Reset the R&S<sup>®</sup> signal generator (press the hardkey *PRESET*).
- 2. Press hardkey *SETUP*; set 10 MHz *Reference Oscillator* to *Internal* or *External Source* as required by your DUT.

Menu 🗖 🖻	🛾 Ref Oscillator 📃 🛛
🗄 Baseband 🔄	Source Internal 🚽
tien AWGN/IMP	,
tiene I/Q Mod	Adjustment
tin RF/A Mod	Adjustment Active
. Graphics	
⊨. Setup	
System —	1
Reference Oscillator	
Internal Adjustments	
Hardware Config	
- Software/Options	
- Start/Stop Gui Update	
Install SW/ Ontion	

Figure 3\_1: Reference oscillator setting.

- 3. Set the test frequency.
- 4. In the signal generator DIAGRAM select RF/A Mod and click config...



The RF level panel opens:

RF Level / EMF / ALC / UCOR					
Level Settings-					
Amplitude	-30.00	dBm 💌			
Limit	30.00	dBm 💌			
Offset	0.00	dB 💌			
Attenuator Setting	15				
Mode Au	uto	-			
Fixed Range (PEP) In: 46.12	-26.12 dBn	n			
User Variation					
Variation Active		Г			
Variation Step	1.00	dB 💌			
Power-On State	Previous Sett	ing 👻			

Figure 3\_3: RF Level Offset input.

6. Enter your RF loss as a negative *Offset* (e.g. -30.7 dB)

7. Press hardkey LEVEL, enter the value required in the testplan, e.g. -98.7 dBm:

Frequency	RF MOD	Р	EP	Level 🦲	DFFSET
1.950 000 000 00 GHz 🗾	OFF OFF	-	98.70	dBy -98.70	dBm 🚽
	ALC-Auto		_	$\sim$	info
RF Level / EMF / ALC / UCOR			<		
Level Settings-		<u> </u>			
Amplitude	-68.00 d	Bm 💌			
Limit	30.00 d	Bm 💌			
Offset	-30.7 d	B	d	RF/A Mod	]
Attenuator Setting	ıs			config	J
Mode	uto	•		□ On	
Fixed Range (PEP) In: -86.02	-66.02 dBm			L	_
User Variation-					
Variation Active			cs		
Variation Step	1.00 df	в			
Power-On / EMF Set	tinas				
Power-On State	Previous Setting		P		

Figure 3\_4: RF Level at the DUT.

#### Glossary of Level Settings:

Level:	power at the DUT (if RF is switched on).
Amplitude:	power at the generator RF port (if RF is switched on).
Offset:	negative value of the insertion loss of the RF path.

Level = Amplitude + Offset

8. Press the *hardkey ESC* to return to the *DIAGRAM*.



9. In the signal generator DIAGRAM select Baseband and click config...

#### The 3GPP FDD main panel opens:

3GPP FDD						
State	Off					
Set To Default	Save/Recall					
Data List Management	Generate Waveform File					
3GPP Version	Release 8					
Chip Rate	3.84 Mcps					
Link Direction	Uplink / Reverse 🗸					
Filter/Clipping/ARB Settings	Downlink / Forward Uplink / Reverse					
Trigger/Marker	Auto					
	Stopped					
Clock	Internal					
Configure Us	er Equipment					
Reset User Equipments	Copy User Equipment					
Additional User Equipment	Test Setups/Models					
Select Use	r Equipment					
	E2 UE3 UE4 On On On On					

11. Set Link Direction to Uplink / Reverse

12. To clear previous settings click *Reset* User Equipments.

Figure 3\_6: 3GPP FDD main panel

13. Click button Trigger / Marker

3GPP FDD: Trigger/Marker/Clock					
Trigger In-					
Mode	Armed Auto				
	Stopped				
	Dropped				
Source	External				
External Delay	8.00 Chips 🔽				
External Inhibit	0 Chips 🗸				
	Marker Mode				
Marker 1 Radio Frame	×				
Marker 2 Radio Frame	×				
	Marker Delay				
	Current Range Without Recalculation				
Marker 1 0 Chips	· ·				
, , ,	0 2000 Chips				
Marker 2 0 Chips					
	0 2000 Chips				
	Fix Marker Delay To Current Range 🗖				
Clock Sattings					
Sync Mode	None				
Clock Source	Internal				
Global Trigger/Clock Settings					

- 14. Select Armed Auto.
- 15. Select *Source External*. This makes the *Delay* and *Inhibit* fields visible.

Figure 3\_7: Trigger settings for BER / BLER tests.

The *External Delay* depends on the type of NodeB. Wide Area NodeBs need a higher delay than Medium Range NodeBs; Medium Range NodeBs need a higher delay than Local Area NodeBs, and so on.

- 16. For optimum value ask the radio vendor.
- 17. Set (Trigger) *Source* back to *Internal*. This halts the generator even if external trigger signals are applied. So the generator doesn't disturb the initialization of the DUT.
- 18. Click Global Trigger/Clock Settings.



19. Modify the default settings if necessary.

Figure 3\_8: The Baseband Trigger is used.

20. Press the hardkey ESC twice to return to the 3GPP FDD main panel.

3GPP FDD			
State	Off		
Set To Default	Save/Recall		
Data List Management	Generate Waveform File		
3GPP Version	Release 8		
Chip Rate	3.84 Mcps		
Link Direction	Uplink / Reverse 💌		
Filter/Clipping/ARB Settings	Root Cosine / Clip Off		
Trigger/Marker	Arm Auto / Ext		
	Stopped		
Clock	Internal		
Configure Us	er Equipment		
Reset User Equipments	Copy User Equipment		
Additional User Equipment	Test Setups/Models		
Select Use	r Equipment		
	E2 On UE3 UE4 I On I On		

Figure 3\_9: 3GPP FDD main panel / Uplink

21. Select and click UE1.

The configuration panel for UE1 opens.

3GPP FDD: User Equipment1	0	0-#1			
	Commo	on Settings		1	
State	On	Mode	DPCCH + DPDCH -	22.	Switch State on.
Scrambling Code (hex)	000 00	Scr Mode	Long Scrambling Code 💌	23.	Enter the Scrambling
Time Delay	0 Chips 🛩 U	se 🗖	UL-DTX		Code.
			Code Domain		
	DPCCH	I Settings		1	
	Pilot 6	TFCI 2	TPC 2		
Show Detail	s >>>	Power	-2.69 dB 💌	24.	Set DPCCH Power to
	DPDCH	I Settings		1	-2.69 dB
	D	Jata 40			
State	🔽 On	Channel Power	0.00 dB 💌		
Show Detail	\$ >>>			25.	Click Show Details.
	HS-DPC	CH Settings		1	
HARQ-ACK (Slo	its)	CQI (	Slots)		

Figure 3\_10: Panel of UE1



<sup>26.</sup> Click Global Enhanced Channels.

3GPP FDD: User Mobile Equipment1/Enhanced Channels				
Enhanced Channels		On		
Channel Coding				
State			🔽 On	27. Click Channel Coding
Coding Type	RMC	(12.2 kb	ps) 🔻	State On.
Show Details >>>				
Bit Error Insertion				
State			□ On	
Bit Error Rate		0.00	1 000 0	
Insert Errors On	Physi	cal Layer	-	
Block Error Insertion-				
State			□ On	

Figure 3\_12: UE1 to generate a real-time RMC 12.2

28. Press the hardkey ESC twice to return to the 3GPP FDD main panel.

3GPP FDD		
State	Off	29. Click State on.
Set To Default	Save/Recall	
Data List Management	Generate Waveform File	
3GPP Version	Release 8	
Chip Rate	3.84 Mcps	
Link Direction	Uplink / Reverse	
Filter/Clipping/ARB Settings	Root Cosine / Clip Off	
Trigger/Marker	Arm Auto / Ext	
	Stopped	

Figure 3\_13: 3GPP FDD main panel

30. Press hardkey RF on.

Figure 3\_11: Panel of UE1 / details

Without a trigger signal, the generator remains stopped. There is no RF output.

- 31. Click button Trigger / Marker...
- 32. Set (Trigger) Source to External.

Now the generator starts running after the trigger event, delayed by the *External Delay*, see fig. 3\_7.

Once running the *ARM* button appears in the 3GPP and the trigger panel:

Filter/Clipping/ARB Settings	Root Cosine / Clip Off		
Trigger/Marker	Arm Auto / Ext		
Arm	Running		
Clock	Internal		
Configure Us	er Equipment		
Reset User Equipments	Copy User Equipment		
Additional User Equipment	Test Setups/Models		

Figure 3\_14: ARM button in the 3GPP FDD main panel

Click ARM to stop the generator (until the next trigger event).

#### Remote Control / SCPI Commands (example values are shaded):

#### Basic settings:

*RST	//	reset
ROSC:SOUR INT	//	10 MHz ref. int
SOUR:FREQ:CW 1950 MHz	//	test frequency
SOUR:POW:OFFS -30.7 dB	//	level offset
SOUR:POW:LEV:IMM:AMPL -98.7 dBm	//	level
Generate uplink RMC 12.2:		
SOUR:BB:W3GP:PRES	//	reset 3G settings
SOUR:BB:W3GP:LINK UP	//	uplink
SOUR:BB:W3GP:SEQ AAUT	//	trig. armed auto
SOUR:BB:W3GP:TRIG:SOUR INT	//	trig. internal
SOUR:BB:W3GP:TRIG:EXT:DEL 2	//	2 chips delay
SOUR:BB:W3GP:MST1:ENH:DPDC:CCOD:STAT ON	//	enhanced on
SOUR:BB:W3GP:MST:ENH:DPDC:CCOD:TYPE M12K2	//	RMC 12.2
SOUR:BB:W3GP:MST1:ENH:DPDC:TCH1:DATA PN9	//	data PN9
SOUR:BB:W3GP:MST1:ENH:DPDC:TCH1:INT1 ON	//	interleaver 1 on
SOUR:BB:W3GP:MST1:ENH:DPDC:INT2 ON	//	interleaver 2 on
SOUR:BB:W3GP:MST:DPCC:SFOR 0	//	slot format O
SOUR:BB:W3GP:MST:DPCC:POW -2.69	//	DPCCH/DPDCH
SOUR:BB:W3GP:MST1:SCOD #H1A	//	scrambl. code 1A
SOUR:BB:W3GP:MST1:STAT ON	//	UE on
SOUR:BB:W3GP:STAT ON	//	3GPP on
OUTP:STAT ON	//	RF on

#### To start the uplink signal at the next trigger event set trigger to external:

SOUR:BB:W3GP:TRIG:SOUR EXT

### 4 Test Steps

The order of the test steps may vary for different NodeBs, in particular at which point in time the generator and the measurement have to be started (steps 7 and 8 below). Ask your radio vendor for the correct order.

1. Connect the DUT, power supply, controller PC and generator as shown in fig. 2\_1 on page 5.

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- 2. Power up the signal generator.
- 3. If the DUT is set to internal 10 MHz reference, configure the signal generator to external reference (and vice versa).
- Configure the signal generator as described in section 3 *Generator Configuration*, steps 1 to 31. The trigger *Source* should still be set to *Internal*. At the first time it could be helpful to use a fairly high generator power level (-70 dBm at the DUT RF port).

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- 5. Power up the DUT.
- 6. Configure the DUT to generate sync pulses.
- 7. Set the generator trigger *Source* to *External*. This starts the uplink signal after the next sync pulse. Check whether the signal generator is running.
- 8. Configure the uplink channel on the DUT and start the test.

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If the DUT does not receive the uplink signal correctly, click *Arm* on the generator to resync up- and downlink.

If this does not help, abort the test program, stop the generator (set it to internal trigger), reset the DUT and restart from step 6.

Consider that the trigger delay set in section 3 step 16 may have been set incorrectly.

### 5 Conclusion

BER and BLER receiver tests are required in R&D, for conformance testing and in production. For all receiver sensitivity and performance measurements, the R&S<sup>®</sup> generators provide the test signals as stipulated by the standard TS 25.141. The insertion of bit errors, applying signal impairments, or Additional White Gaussian Noise requires only a few keystrokes.

The R&S $^{\circ}$  generators SMU, SMJ, and SMBV are remote compatible, and can be controlled via LAN or IEEE.

For transmitter tests to TS25.141 as well as for classical spectrum measurements in R&D and production Rohde & Schwarz<sup>®</sup> recommends the R&S<sup>®</sup>FSQ, R&S<sup>®</sup>FSL, and R&S<sup>®</sup>FSV Signal Analyzers.

### 6 Literature

- [1] 3GPP TS25.141; Base Station (BS) conformance testing (FDD) V 8.4.0, 2008-09
- [2] 3GPP TS25.104; Base Station (BS) radio transmission and reception (FDD) V 8.4.0, 2008-09
- [3] 3GPP TR25.820; 3G Home NodeB Study Item Technical Report V 8.0.2, 2008-09
- [4] Tests on 3GPP WCDMA FDD NodeBs in Accordance with Standard TS25.141, Application Note 1MA67, Rohde&Schwarz<sup>®</sup>, 2005
- [5] picoChip support site https://support.picochip.com/

## 7 Additional Information

Please contact <u>tm-applications@rohde-schwarz.com</u> for comments and further suggestions.

For additional information on picoChip, mail to info@picochip.com.

# 8 Ordering Information

SMBV100A VECTOR SIGNAL GENERATO	R
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Туре	Designation	Order No
SMBV100A	Vector Signal Generator	1407.6004.02
SMBV-B103 or	9 kHz to 3.2 GHz	1407.9603.02
SMBV-B106	9 kHz to 6 GHz	1407.9703.02
SMBV-B10	Baseband Generator with Digital Modulation (realtime) and ARB (32 MSample), 120 MHz RF Bandwidth	1407.8607.02
SMBV-K42	Digital Standard 3GPP FDD	1415.8048.02

SMJ100A VECTOR SIGNAL GENERATOR				
	-			
Туре	Designation	Order No		
SMJ100A	Vector Signal Generator	1403.4507.02		
SMJ-B103 or SMJ-B106	Frequ. range 100 kHz - 3 GHz Frequ. range 100 kHz - 6 GHz	1403.8502.02 1403.8702.02		
SMJ-B9 or SMJ-B10 or SMJ-B11	Basebandgenerator with dig. modulation (real time) and ARB 128 / 64 / 16 MSamples	1404.1501.02 1403.8902.02 1403.9009.02		
SMJ-B13	Baseband main module	1403.9109.02		
SMJ-K42	Digital Standard 3GPP FDD	1404.0405.02		

SMBV100A VECTOR SIGNAL GENERATOR				
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Туре	Designation	Order No		
SMU200A	Vector Signal Generator	1141.2005.02		
SMU-B102 or	Frequ. range 100 kHz - 2.2 GHz	1141.8503.02		
SMU-B103 or	Frequ. range 100 kHz - 3 GHz	1141.8603.02		
SMU-B104 or	Frequ. range 100 kHz - 4 GHz	1141.8703.02		
SMU-B106	Frequ. range 100 kHz - 6 GHz	1141.8803.02		
SMU-B9 or	Basebandgenerator with dig.	1161.0766.02		
SMU-B10 or	modulation (real time) and ARB	1141.7007.02		
SMU-B11	128 / 64 / 16 MSamples	1159.8411.02		
SMU-B13	Baseband main module	1141.8003.02		
SMU-K42	Digital standard 3GPP FDD	1160.7909.02		

Table 8\_1: Instruments and instrument options for BER / BLER tests

#### About Rohde & Schwarz

Rohde & Schwarz is an independent group of companies specializing in electronics. It is a leading supplier of solutions in the fields of test and measurement, broadcasting, radiomonitoring and radiolocation, as well as secure communications. Established 75 years ago, Rohde & Schwarz has a global presence and a dedicated service network in over 70 countries. Company headquarters are in Munich, Germany.

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Certified Quality System ISO 9001 DQS REG. NO 1954 QM

Certified Environmental System ISO 14001 DQS REG. NO 1954 UM

This application note and the supplied programs may only be used subject to the conditions of use set forth in the download area of the Rohde & Schwarz website.

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