## Starting Successfully with the R&S<sup>®</sup> EX-IQ-Box Application Note

### Products:

- | R&S<sup>®</sup>EX-IQ-Box | R&S<sup>®</sup>FSV
- | R&S<sup>®</sup>CMW500 | R&S<sup>®</sup>FSQ
- | R&S<sup>®</sup>AMU100A | R&S<sup>®</sup>FSG
- | R&S<sup>®</sup>SMU200A | R&S<sup>®</sup>FMU36
- | R&S<sup>®</sup>SMJ100A

The R&S EX-IQ-Box serves as a digital baseband interface between a device under test (DUT) and Rohde & Schwarz generators, analyzers and radio communication testers. The *DiglConf* software supplied with the device controls up to four R&S EX-IQ-Boxes in a test setup and can thus output IQ data for feeding into a DUT while simultaneously receiving IQ output from a DUT.

To work together smoothly, the DUT, the R&S EX-IQ-Box and the R&S test instruments have to be configured properly. The purpose of Application Note 1MA168 is to introduce the right "initial steps" required to get started successfully.



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### 1 Overview

The R&S EX-IQ-Box serves as a digital baseband interface between a device under test (DUT) and Rohde & Schwarz generators, analyzers and radio communication testers. The *DiglConf* software supplied with the device controls up to four R&S EX-IQ-Boxes in a test setup and can thus output IQ data for feeding into a DUT while simultaneously receiving IQ output from a DUT.



Figure 1: The R&S EX-IQ-Box as an interface between R&S-formatted and user-formatted IQ data

R&S instruments use an R&S-specific interface to exchange digital IQ data amongst themselves. The main purpose of the R&S EX-IQ-Box is to convert the R&S format used for this into a DUT's individual user format, or (in the opposite direction) to convert the DUT's user format into the R&S format. This takes place inside the R&S EX-IQ-Box with the aid of programmable logic arrays (FPGAs).

The modes of operation for the interface to the DUT offer:

- Parallel or serial data formats.
- Various word sizes (number of bits per word).
- Different bit orders (LSB or MSB first).
- Interleaving or not interleaving of I and Q values.
- Single or double data rate.
- Internal or external clock.
- LTTL or CMOS logic with various voltage level.
- Single-ended or differential inputs and outputs.

This high flexibility enables the R&S EX-IQ-Box to meet nearly all kinds of user requirements. The "breakout boards" supplied with the box make it easy to adapt to the DUT at the *User Interface*.

To work together smoothly, the DUT, the R&S EX-IQ-Box and the R&S test instruments have to be configured properly. The purpose of Application Note 1MA168 is to introduce you to the right "initial steps" required to get started successfully. This Application Note cannot replace the instrument manuals and is not meant to do so; it should be understood as a summary of the most important steps in a single document.



1MA168 covers the following topics:

Figure 2: Topics covered in application note 1MA168

The *R&S EX-IQ-Box Operation* chapter (yellow) explains the *R&S EX-IQ-Box's* basic functions, its use as a transmitter or a receiver. It then introduces the *DiglConf* program that is used to configure the box. A description of the interface signals rounds off this overview.

The topics with a green background deal with the hardware and instrument setups for the different modes: the transmitter mode (which stimulates the DUT), the receiver mode (records DUT data) and mixed mode (stimulates the DUT and records the DUT data).

The topics with a red background deal with the physical aspects regarding transmission of data signals. This covers:

- Testing the user interface port in the *DiglConf* test mode.
- Setup and hold times on the user interface with an internal and an external clock.
- Verification of the actual signal and timing conditions.
- The breakout board types.

Although the content differs significantly, all of these subjects are equally important.

The *Transmitter*, *Receiver* and *Mixed* modes are each handled separately for the R&S generator, analyzer and radio communication tester. By this you can concentrate fully on your use case. Each individual application is described completely: if you are working in *Transmitter Mode*, you don't need any information from the *Receiver Mode* chapter; if you are working with the analyzer, you do not need any information from the generator sections.

The 1MA168 Application Note is based on the K04 variant of the R&S EX-IQ-Box and deals exclusively with the R&S EX-IQ-Box's user-defined mode.

The handling of the analyzers R&S FSQ, R&S FSG, and F&S FMU36 is very simular. So the R&S FSG and the F&S FMU36 are no longer mentionned in this document. Refer to the description of the R&S FSQ.

Screen shots from the generators are mostly taken from the R&S AMU. For R&S SMJ and R&S SMU they are almost the same.

The following abbreviations are used throughout this manual:

R&S<sup>®</sup>AMU200A as R&S AMU R&S<sup>®</sup>SMU200A as R&S SMU R&S<sup>®</sup>SMJ100A as R&S SMJ R&S<sup>®</sup>FSQ as R&S FSQ R&S<sup>®</sup>FSV as R&S FSV R&S<sup>®</sup>CMW500 as R&S CMW

### 2 R&S EX-IQ-Box Operation

### **Transmitter and Receiver Mode**

The R&S EX-IQ-Box serves as a digital IQ interface between R&S instruments and a DUT. It is operated via an Dig. IQ Data cable that is approximately 2 m long. So it is possible to put the EX-IQ-Box very close to the DUT, and use advantageously short cables between DUT and the User Interface.

The R&S EX-IQ-Box is configured using *DiglConf*, a PC program that controls the box via its USB port. This is where the operating mode is selected:



Figure 3: Basic operation of the R&S EX-IQ-Box

If the DUT is to be stimulated, the R&S instruments serve as IQ sources; the R&S EX-IQ-Box works in **Transmitter Mode**. The IQ data usually comes from a generator or from the R&S CMW radio communication tester. However, several R&S analyzers also have (optional) IQ outputs, through which the down-converted RF signals are supplied as IQ data streams in real time.

For analysis of the data sent from the DUT, the R&S instruments serve as IQ sinks; the R&S EX-IQ-Box works in **Receiver Mode**. Usually, the IQ data is evaluated by an analyzer with specialized personalities – vector signal analysis (VSA), WCDMA, LTE etc. – or with the R&S CMW radio communication tester. Many R&S generators can also (optionally) be equipped with IQ inputs to add impairments, fading or AWGN in real time. These post-processed IQ signals can then be up-converted into the RF band or, be outputted digitally and, for instance, looped back into the radio communication tester.

The following applies in both transmitter and receiver mode:

The R&S-specific IQ interface between the R&S instrument and the R&S EX-IQ-Box (see Figure 3 on page 6) is used for more than just transferring the IQ data and clock. When the instruments are connected and when specific settings are changed, a complex protocol runs, hidden to the user. This protocol clarifies:

- Which devices are connected.
- Whether the cable connection works reliably (PRBS test).
- Which sample rate is programmed in the R&S EX-IQ-Box.

The data transfer between the R&S instrument and the R&S EX-IQ-Box works fully automatically; in particular the following details are hidden to the user:

Inside the R&S EX-IQ-Box a dual port FIFO manages the data flow. One port serves the R&S-specific IQ interface, the other one the user interface. The ports are read out or written to independently from each other, thus synchronizing two data streams with different timing:

- Data traffic between the user interface and the DUT is always accomplished synchronously with the clock signal of the user interface.
- Data traffic on the R&S-specific IQ interface, on the other hand, depends on the connected instrument. Data may flow regulary, or in a bursted mode at maximum speed.

In this way, the R&S EX-IQ-Box's data throughput is determined by the clock rate at the user interface.

This has no particular significance for real time applications. As a user, you can always concentrate fully on the interface between the R&S EX-IQ-Box and the DUT.

Nonetheless, this creates additional interesting usage scenarios for the R&S analyzers and radio communication testers:

### • Gated transfer

In addition to the clock, there is a valid pin (Signal-Name: UI\_Valid) on the R&S EX-IQ-Box's user interface. In Receiver Mode, you can apply a gate signal here, which either enables or disables the data flow. This is needed, for example, if the recording has to begin precisely at a certain point in time, e.g. at the start of a mobile radio frame.

### • Slow IQ mode (non-real time operation)

As a mobile tester, the R&S CMW generates downlink signals and analyzes uplink signals. The R&S CMW can do this in real time. In this case the *sample rate* is the mobile radio standard's system clock, multiplied by an oversampling factor. (A WCDMA signal using 3.84 MHz system clock with four-fold oversampling, for example, has a *sample rate* of 15.36 Msps.)

However, the R&S CMW can also output or input the same data more slowly via the R&S EX-IQ-Box, for example at 1 MHz.

To do this, you only need to reduce the clock frequency at the user interface to 1 MHz in *DiglConf.* In particular the configuration of the R&S CMW requires no changes at all.

Gated recording and slow IQ will be covered again later.

The R&S *DiglConf* software controls up to four R&S EX-IQ-Boxes in a test setup. Each of these boxes can work either as a transmitter or as a receiver, independently.

With the R&S AMU or R&S SMU two-channel generators and two R&S EX-IQ-Boxes, you can establish two independent TX paths, for instance for MIMO applications.

Figure 4 shows how you can use two R&S EX-IQ-Boxes to simultaneously stimulate a DUT at its input and analyze its output. This is a typical configuration for testing and measuring mobile radio chips. The IQ data source is, in this case, the R&S SMU vector signal generator; R&S EX-IQ-Box 1 serves as a transmitter. R&S EX-IQ-Box 2 serves as a receiver; the IQ data sink is an R&S FSQ signal analyzer.



Figure 4: DUT between an IQ transmitter and IQ receiver

Users of the R&S CMW test DUTs with a similar setup (see Figure 5 on page 9).

Here, the R&S CMW simulates an IQ base station. In this case, it sends a downlink signal to the DUT via R&S EX-IQ-Box 1. R&S EX-IQ-Box 2 receives the DUT uplink signal's IQ values and returns them to the R&S CMW for analysis. You will find a more detailed description of this application in Chapter 7, *Mixed Mode: How to Stimulate and Analyze DUT Data*.



Figure 5: DUT between the R&S CMW's IQ input and output

*DiglConf* uses a separate set of parameters for each R&S EX-IQ-Box. The DUT may use different data formats or clocks at the input and the output.

The figures shown up until now have only shown the basic data flows. Additional signals are also present in the test setup: an internal or external clock, possibly a marker and possibly a data-valid signal. Moreover, the components have to be synchronized with one another using a frequency reference. You will find details on this in the following chapters of this Application Note.

Prior to starting the measurement task itself, the following steps are always necessary:

- 1. Setup the Hardware: Connect the test instruments, the R&S EX-IQ-Box and the DUT.
- 2. Setup the R&S EX-IQ-Box: Configure the R&S EX-IQ-Box using the *DiglConf* program.
- 3. Setup the R&S instruments (generator, analyzer, radio communication tester).
- 4. Setup the DUT.

The DUT setup is the user's responsibility. (This step can be performed earlier in the sequence.)

The other steps will be described in the chapters to come. This Application Note will cover the setup of the R&S EX-IQ-Box first, because the same procedure is used for transmitter mode and receiver mode.

### 3 Using *DiglConf* to Set up the R&S EX-IQ-Box

### **First steps**

Configuration of the R&S EX-IQ-Box K04 is performed via the *DiglConf program*; the R&S EX-IQ-Box is programmed via its USB port.

- Install the DiglConf software on your PC. Be sure to observe the notes in the R&S EX-IQ-Box Manual, especially with regard to the Windows login.
- ► Start *DiglConf*.

*DiglConf* manages up to four R&S EX-IQ-Boxes. The top level in the program's GUI shows as many EX-IQ blocks as are indicated for the *Number of Ex-IQ-Boxes* (see Figure 6).



Figure 6: Top level of the DiglConf GUI, controlling up to four R&S EX-IQ-Boxes

There is an independent set of parameters behind each EX-IQ-Box block. This parameter set is automatically stored when the program is closed and then automatically loaded the next time the program starts.

For this reason, the following explanations can be limited to a setup with only one R&S EX-IQ-Box.

Each R&S EX-IQ-Box has its own power supply. However, the box does not switch on until the USB connection is established with the control PC.

Start *DiglConf* and insert the USB cable (or do this in the opposite order).

It takes a few seconds until an R&S EX-IQ-Box is recognized as a USB device. Then a brief message appears on the *DiglConf* top-level screen, see Figure 7:

-lie Tools Hi	sib
🖆 🚅 日	Number of Ex-IQ-Boxes: 1
EX-IQ-BOX	connected on USB

Figure 7: DiglConf indicates a connected R&S EX-IQ-Box

At this point, *DiglConf* has already read such information as the serial numbers of the connected R&S EX-IQ-Boxes. This information now appears in the pulldown lists for each EX-IQ-Box block. In Figure 8, only one R&S EX-IQ-Box is involved:

	EX-IQ-BOX 1	
	config	
	Undefined 💌	TUD 🖯
IG IQ IN/OUT	Undefined	
	101274	·

Figure 8: Serial No. of a connected R&S EX-IQ-Box

 Using the serial number, select the R&S EX-IQ-Box that you now want to configure.

When this is done, *DiglConf* shows which measurement instrument is already connected with the selected Box and ready for operation (see Figure 9). This information and the instrument's serial number were automatically retrieved via the digital IQ interface:



Figure 9: Instruments and data flow in the DiglConf GUI

Now you can configure the selected R&S EX-IQ-Box.

### Configuring the R&S EX-IQ-Box

Click on *config* in the module block of the R&S EX-IQ-Box that you want to configure. Select "User Defined", see Figure 10:

Instrument ] 🔍	——— Interface Type ———	
MU200A (100228)	User Defined	
	CPRI	DUT
	Transient Recorder 1	
	Transient Recorder 2	

Figure 10: Basic operation mode: User Defined

This takes you to the user defined main panel. Instead of the normal main panel content, Figure 11 shows the configurable parameters for the four tabs *Protocol*, *Data*, *Clock* and *Test*.

🧱 EX-IQ-BOX 1 (10127	4): User Defined		<u>s</u> _ • ×
State	On Logic Type	3.3V CMOS 🚽	Set To Default
	Direction	Transmitter 🚽	Save/Recall
/Protocol VData VCI	ock VTest \		
Format	Signal Type		
Data Rate	Word Size	Clock Rate	Test On
Interleaving	Bit Order	Clock Source	Test Signal
	Numeric Format	Clock Phase	
		Clock Skew	
		Sample / Clocl	k Ratio
		Ext. Reference	e Frequency
R&S 16 EX-IQ-BOX 16	Clock Data )(		
	« Data <u>k</u>	Λ	λ

Figure 11: Setting the parameters of the main User Defined panel

All of the configurations for the R&S EX-IQ-Box are set in the main panel.

► To get familiar with all the parameter settings, go through all of them in order.

For most parameters, the program shows a list of options to choose from. With the *Data* and *Clock* tabs, the main panel shows a wiring diagram. Beneath this, you will always find the timing for the clock, data and, where applicable, the marker or strobe. As a result, *DiglConf* is very easy to use. Before you turn your attention to the parameters for the tabs:

- Select your *Logic Type*.
- Select whether the box is to be operated as a **Transmitter** or **Receiver**.

For the most part, the parameters found under the tabs are self-explanatory. For this reason, the following explanations only cover the special aspects. For comprehensive information, read the R&S EX-IQ-BOX Operating Manual [1].

### Protocol tab (Figure 12)

Format: Data can be output or read in as a Parallel or a serial bit stream.

*Data Rate: SDR* and *DDR* are available for selection. *SDR* stands for single data rate, which means that one data transfer takes place per clock cycle. *DDR* stands for double data rate: Here, data is transferred at each edge of the clock signal.

*Interleaving*: IQ data can be available via separate ports, or it can be multiplexed using the same ports.

🧱 EX-IQ-BOX 1 (101274): User De	fined	
State	Logic Type 3.3V CMOS	Set To Default
	Direction Transmitter	Save/Recall
/Protocol VData VClock VTest	7	
l f	Protocol	1
Format		Parallel
Data Rate		SDR 🗾
Interleaving		Not Interleaved 💌
Data Settings	1	6 Bit / 2's Complement / IQ
Clock Settings		Internal (BNC REF IN) / 0 deg
Clock Rate / Sample Rate	50.000 000 000	MHz / 50.000 000 000 MHz
Clock		
R&S 16 I Data )	χ	χ
EX-IQ-BOX 16 → Q Data )	χ	χ

Figure 12: Setting parameters for the Protocol tab

Below the *Protocol* entry window, there is a display of the data and clock settings from the other tabs.

These sections will be described in greater detail below.

### Data tab (Figure 13)

The R&S EX-IQ-Box works with a word size of up to 18 bits for I and Q. Correspondingly, the user interface for the R&S EX-IQ-Box has 18 data ports for I and Q. Parallel data with a smaller word size can either be aligned at Position 0 or at Position 17 (*LSB* or *MSB Word Alignment*). This applies, for example, to the R&S generators, which make do with a 16-bit word size.

Within the data words, the bits can be arranged in ascending or descending order (*LSB* or *MSB Bit Order*).

				100			122				5 N.					and a second
			On		Lo	gic Ty	pe 3.	3V C	MOS	•			Se	t To C	)efault	É
					Dir	ection	T	ransm	itter	-			Sa	ve/Re	call	8
	Data	VCI	ock	( Tes			24									
Туре	D.												T I	Q		-
Size													Γ		16	Bit 💌
Aligni	ment												Γ	SB	2	•
ler													Γ	.SB		
						ser Int	erfac	e Bits	Align	ment						
1 ×	2 ×	3 ×	4 ×	5 X	6 ×	7 ×	8 ×	9 ×	10 ×	11 ×	12 ×	13 ×	14 ×	15 M	16 	17 -
ic Fo	rmat												2	's Co	mpler	nent 💌
_							_									
		$\rightarrow$ (	lock	1												
¢	16	<b>_</b> I	Data	X						X						
X.	16		Data	.v—												
	Type Size Aligni er	Type Size Vignment er 1 2 x x ic Format	Type Size Vignment er 1 2 3 * * * ic Format	On Type Nize Vignment er 1 2 3 4 × × × × ic Format ↓ 15 Clock ↓ 16 Data	On Type Size Vignment er $1 \ 2 \ 3 \ 4 \ 5$ $\times \ \times \ \times \ \times \ \times$ ic Format Clock J 16 I Data J DATA	$\begin{array}{c c} \hline On & Lo. \\ \hline Dir \\ Dir \\ \hline Dir \\ \hline Dir \\ \hline Dir \\ \hline Dir \\ Dir \\ \hline Dir \\ \hline Dir \\ \hline Dir \\ Dir \\ \hline Dir \\ \hline Dir \\ Dir \\ \hline Dir \\ Dir \\ \hline Dir \\ $	On Logic Ty Direction Type Size Vignment 1 2 3 4 5 6 7 x x x x x x x ic Format Clock 16 Data Y	On Logic Type 3 Direction T Direction T Type Size Vignment er 1 2 3 4 5 6 7 8 $\times$ $\times$ $\times$ $\times$ $\times$ $\times$ $\times$ ic Format Clock 16 Data X	On Logic Type 3.3V Cl Direction Transm $\Gamma \sqrt{Data} \sqrt{Clock} \sqrt{Test}$ Type Size Vignment er User Interface Bits 1 2 3 4 5 6 7 8 9 * * * * * * * * * * * ic Format Clock 16   Data )	On Logic Type 3.3V CMOS Direction Transmitter Type Nize Vignment 1 2 3 4 5 6 7 8 9 10 x x x x x x x x x ic Format Clock Clock Core Logic Core	On Logic Type 3.3∨ CMOS Direction Transmitter Type Nize Vignment er 1 2 3 4 5 6 7 8 9 10 11 × × × × × × × × × × × × × × × × × × ×	On Logic Type 3.3∨ CMOS ✓ Direction Transmitter ✓ Type Nize Vignment 1 2 3 4 5 6 7 8 9 10 11 12 × × × × × × × × × × × × × × × × × × ×	On Logic Type $3.3 \vee CMOS$ Direction Transmitter Type Nize Vignment 1  2  3  4  5  6  7  8  9  10  11  12  13 $\times  \times  \times  \times  \times  \times  \times  \times  \times  \times $	On     Logic Type     3.3V CMOS     ✓     Se       Direction     Transmitter     ✓     Sa       Type     I     I     I       Type     I     I     I       Size     I     I     I       Vignment     I     I     I       1     2     3     4     6       Viser Interface Bits Alignment     I     I       1     2     3     4     5       Viser Interface Bits Alignment     I     I       1     2     3     4     5       0     0     11     12     13       14     X     X     X     X       16     1 Data X     X     X	On     Logic Type     3.3V CMOS     Set To E       Direction     Transmitter     Save/Re       Type     IQ       Size     IQ       Nize     IQ       Vignment     LSB       1     2     3     4     5     7     8     9     10     11     12     13     14     15       *     ×<	On     Logic Type     3.3V CMOS     Set To Default       Direction     Transmitter      Save/Recall       Type     IQ       Size     16       Vignment     LSB       1     2     3     4     5     7     8     10     11     12     13     14     16     16       1     2     3     4     5     7     8     9     10     11     12     13     14     16     16       1     2     3     4     5     7     8     9     10     11     12     13     14     16     16       ic Format     2's Compler     I     2's Compler     I     16     10     11     12     13     14     15     16       ic Format     2's Compler     I

Figure 13: Setting parameters for the Data tab

Clock tab (Figure 15 on page 15)

The word *Clock* refers to the internal or the external clock signal at the user interface. (It should not be mixed up with the *Reference Frequency* which can also be set to external or internal).

Internal Clock: the R&S EX-IQ-Box supplies a clock signal to the DUT. External Clock: the DUT supplies a clock signal to the R&S EX-IQ-Box.

The Clock (Clock Rate) is defined by the data rate the DUT requires. The range of Clock Rate values depends on which breakout board is used and whether Internal or External is selected as the Clock Source:

Clock rate range		
	Single-ended breakout board	Differential breakout board
Internal clock	1 kHz - 100 MHz	1 kHz - 400 MHz
External clock	25 kHz - 100 MHz	25 kHz - 400 MHz

Figure 14: Clock rates for the R&S EX-IQ-Box

If the *Clock Source* is set to *Internal*, the R&S EX-IQ-Box requires an external reference frequency input signal at the BNC *REF IN* connector.

This External Reference Frequency can be 5 MHz, 10 MHz or 13 MHz.

State	On	Logic Type 3.	3V CMOS	•	Set To	Default
		Direction Tr	ansmitter	•	Save/F	Recall
Protocol V Data	/Clock VTe	st				
(	Clock Settings		1 [	External	Reference Frequ	Jency
Clock Rate	50.000 0	00 000 MHz 💌	Source		REF IN	<u>.</u>
Clock Source	Internal (B	NC REF IN) 💌	Frequenc	;y	10 MHz	-
Clock Phase	0 deg					
Clock Skew		0.00 ns 💌				
Sample/Clock Ra	te Ratio	1 -				
R&S Instrument Ref.Out		ita F EX-I R	R&S Q-BOX ef.In	(	Data	DUT
R&S 16	Freq. I → Clock ⇒ I Data )(	Ref.				ſ
X-IQ-BOX 16	⇒ Q Data <u>)</u>			_X		X

Figure 15: Setting parameters for the Clock tab

If the *Clock Source* is set to *External*, a reference frequency input is not required. In this case, the R&S EX-IQ-Box derives its internal reference from the external clock supplied by the DUT. This external clock must be a continuous signal.

Always enter the Clock Rate, even if you are working with an External Clock. The R&S EX-IQ-Box's PLL needs this value in order to determine its capture range.

A reference signal fed into the R&S EX-IQ-Box's *REF IN* connector, is ignored if an external clock is used.

The *Clock Phase* and *Clock Skew* both have an effect as a data delay. In this way, you can fine tune setup and hold times at the user interface if necessary. The current timing is shown on the bottom of the main panel.

### Sample / Clock ratio

The *Clock Rate* determines the data transfer between the DUT and the R&S EX-IQ-Box. The *Clock Rate* is defined by the DUT requirements and is entered by you in the *DiglConf* program.

*DiglConf* uses this entry to derive a *Sample Rate* for the data transfer between the R&S EX-IQ-Box and the R&S measurement instrument. This *Sample Rate* is indicated in the *Protocol* tab (see Figure 16).

Protocol VData VClock VTest		
	Protocol	
Format		Parallel 🗾
Data Rate		SDR 👤
Interleaving		I/Q Interleaved 💌
Data Settings	18 Bit / 2	's Complement / IQ
Clock Settings	Internal (B	NC REF IN) / 0 deg
Clock Rate / Sample Rate	100.000 000 000 MHz / 5	50.000 000 000 MHz

Figure 16: Indication of calculated Sample Rate

- If you are working with the *parallel* data format, each active clock edge at the user interface requires a data transfer on the cable between the R&S EX-IQ-Box and the connected R&S instrument. Without Interleaving the clock and the (effective) sample rate are the same.
- When using the *serial* data format at the user interface, the sample rate is reduced by a factor 1/ word size.
- Double data rate (DDR) doubles the sample rate.
- Interleaving cuts the sample rate in half (see Figure 16).

The connected R&S device has to deliver this sample rate or to process it.

As an exceptional case, you can set the *Sample / Clock Rate Ratio* to less than one in the clock settings (Figure 15 on page 15). Here, you can choose from the ratios of 4/5, 2/5, 1/5, 1/10 or 1/20. In these cases, you have "more clocks than valid data." In the TX mode, die R&S EX-IQ-Box then fills in dummy data. For each clock period, the *Data Valid* connection at the user interface indicates whether valid or dummy data is being supplied. When the data is valid, *Data Valid* is high; for dummy data, it is low.

### Test tab

In transmitter mode, you can output test patterns and input them in receiver mode. In test mode, you can measure and optimize the settings for setup times and hold times. A separate chapter, *Testing the User Interface,* on page 51, will cover this interface test.

### Starting the R&S EX-IQ-Box

► Click State On in the main panel (see Figure 17).

EX-IQ-BOX 1 (1012	74): Usei	Defined			
State	On	Logic Type	3.3V CMOS	•	Set To Default
		Direction	Transmitter	•	Save/Recall
Protocol V Data V C	lock VT	est \			
			Protocol		
Format					Parallel 🗾
Data Rate					SDR / DDR

Figure 17: Starting the R&S EX-IQ-Box

A dialog window asks if you want to accept the level of the set logic type.

► Click OK.

**Note**: In the *State Off* mode, the data connections at the user interface have high-impedance characteristics. They become active when the system switches to *State On*.

### **Transient recorders**

The transient recorders monitor the R&S EX-IQ-Box's DIG IN/OUT 1 and 2 interfaces. Use the transient recorders to observe the incoming and outgoing data flowing between an R&S instrument and the R&S EX-IQ-Box.

- First, start your application. Then go to the main menu in *DiglConf*.
- Click config in the module block for the desired R&S EX-IQ-Box. Select Transient Recorder 1 or 2 (see Figure 18):

CMW 500 (100397)	User Defined	
	Misc	DUT
	Transient Recorder 1	
	Transient Recorder 2	

Figure 18: Selecting a transient recorder

This takes you to the transient recorder panel (Figure 19).



Figure 19: Active transient recorder panel

- Select DIG IQ IN 1 data source in transmitter mode.
- ► Select DIG IQ OUT 2 data source in receiver mode.

You have four types of displays to choose from (see Figure 20):

Dis Smart Graphic	olay Settings I
Display Type	1/Q 🗾
	I/Q
Acqu	Vector
Aquisition Length	CCDF
Decimation Factor	Power Spectrum

Figure 20: Types of signal representation with the transient recorders

Please note that signal representation only appears in the display windows when the transient recorder is turned on <u>and</u> data is flowing between the Rohde&Schwarz instrument and the R&S EX-IQ-Box.

The transient recorder enables you to quickly gain an overview of the interface signals:

- In TX mode, you can perform a rough check to see if you have configured your IQ source correctly.
- When you are in RX mode and are inputting signals with a known signal spectrum, use the transient recorder to check if the spectrum is also correct at the interface between the Rohde&Schwarz instrument and the R&S EX-IQ-Box. If the spectrums match, the connection between the DUT and the R&S EX-IQ-Box is OK and the *Alignment* has been set properly in *DiglConf*.

The *Smart Graphic* check box (see Figure 19) determines whether or not the graphics display should also be displayed in *DiglConf*'s main menu.

► Familiarize yourself with the display options.

### 4 Signals at the User Interface

The interface to the DUT, the user interface, consists of a multi-pin connector at the R&S EX-IQ-Box front. It is made for connecting either the single-ended or the differential breakout board supplied with the R&S EX-IQ-Box. Here, the user interface's contacts are distributed across two connectors; additional pins provide Vcc and ground potential.

With the single-ended breakout board, there is one active pin for each logical connection (and a ground wire); with the differential breakout board, there are two (and two ground wires).

The figures in earlier sections of this document only showed the basic connections between the components involved in the flow of data. In practice, the following signals are of importance:

I / Q data	(User Interface)
Clock input	(User Interface)
Clock output	(User Interface)
Marker, strobe	(User Interface)
Data valid	(User Interface)
Frequency reference	(REF IN BNC connector)
	I / Q data Clock input Clock output Marker, strobe Data valid Frequency reference

The data and clock signals are always required; the need for the other signals depends on the specific application.

This chapter deals with the meaning of the signals. The question of which pins these signals are available on for the individual breakout boards are answered in the chapter entitled *The Breakout Boards*, page 61. There, you will also find data on fan-out and on setup times and hold times.

The following section cites the signal names that are used with the single-end board, such as UI\_I\_P0 for user interface / I Data / Data Pin 0 etc. For the differential breakout board, there is a pin pair – such as UI\_I\_P0 and UI\_I\_N0 – for each logical connection.

### I / Q Data: UI\_I\_P0 ... 17, UI\_Q\_P0 ... 17 (output or input)

The R&S EX-IQ-Box works with a word size of up to 18 bits for I and Q; there are 18 data ports in each case. Parallel data with a smaller word size can be aligned at either P0 or P17. In transmitter mode, the data ports are outputs; in receiver mode, they are inputs. The number of active ports is lower when your application requires a smaller word size, when you use interleaving, or when you work with serial data streams (see Table 4\_1).

Data format	UI_I_P0	 UI_I	_P17	UI_Q_P0	 UI_Q_P17
Parallel, no interleaving					
Parallel, with interleaving					
Serial, no interleaving					
Serial, with interleaving					

Table 4\_1: Data ports used for the different output formats

### Clock output: D\_CLK\_UOUT (output)

Outputs the data clock. If the R&S EX-IQ-Box is set to internal clock, this will be the internal clock. If set to external clock, the external clock will be offered here in a buffered state.

(To generate an internal clock, the R&S EX-IQ-Box requires a reference signal at the REF IN BNC connector.)

### Clock input: D\_CLK\_UIN (input)

Input for the external clock from the DUT. If the R&S EX-IQ-Box is set to internal clock, any signal applied here is ignored.

Clock frequency range		
	Single-ended breakout board	Differential breakout board
Internal clock	1 kHz - 100 MHz	1 kHz - 400 MHz
External clock	25 kHz - 100 MHz	20 kHz - 400 MHz

 Table 4\_2: Clock frequency ranges for the specific clock modes and types of breakout board

Note: External or internal clock can be used in transmitter or receiver mode either.

### Marker, strobe: UI\_GP5 (output or input)

This signal is relevant for serial data and interleaving. In transmitter mode, this port serves as an output, in receiver mode as an input.

### Parallel data:

When I/Q or Q/I interleaving is used, this port indicates the I data.

	$\xrightarrow{16}$ Data V				ſ
R&S EX-IQ-BOX		<b>1</b> ,0)	^	U.	A
UI_GP5			1		



Serial data:

The bit position and the signal polarity are configurable. When interleaving is not used, the selected bit position is displayed. With I/Q interleaving, this port is active from  $I_{Bit-Position}$  to (and including)  $Q_{Bit-Position}$ , with Q/I-interleaving from  $Q_{Bit-Position}$  to (and including)  $I_{Bit-Position}$  (see Figure 22).

	──→ Clock ∫				ſ
R&S	IQOIQ16 Data X	Q3	χ	13	χ
LA-IQ-BUX	s Strobo				

Figure 22: Marker timing for Q/I interleaved serial data, bit position = 3

### Data Valid: UI\_VALID

### (output or input)

### Transmitter mode:

If the sample / clock ratio is set in *DiglConf* to a value lower than 1, the clock rate at the user interface is higher than samples can be supplied by the R&S instruments. In this case, the R&S EX-IQ-Box inserts dummy data. UI\_VALID = high marks the valid data and UI\_VALID = low marks the dummy data.

### Receiver mode:

In this case, you can realize a gate window. The R&S EX-IQ-Box only reads in data when UI\_Valid has a high level. If the port is not connected, an internal pull-up resistor keeps UI\_Valid on "high."

### Frequency reference: REF IN (input, 50 ohm)

If the R&S EX-IQ-Box is set to internal clock, the R&S instrument (generator, analyzer etc.) must supply a reference frequency to *REF IN* connector of the Box.

If the R&S EX-IQ-Box is set to external clock, synchronization of the Box and the R&S instrument is derived from this clock by a PLL circuit. For this reason, the external clock must be applied as a continuous signal.

The R&S EX-IQ-Box ignores signals at the *REF IN* connector when the R&S EX-IQ-Box is configured for external clock.

Beyond this, in general, the referencies of R&S instrument and the DUT also have to be coupled. You will find connection recommendations in later sections of this document that cover the hardware setups.

# 5 Transmitter Mode: How to Stimulate a DUT

Data transmission between the DUT and R&S instruments always requires the following steps, which remain the same:

- 1. Setup the hardware: Connect the measurement instruments, the R&S EX-IQ-Box and the DUT.
- Setup the R&S EX-IQ-Box: Configure the R&S EX-IQ-Box with the *DiglConf* program.
- 3. Setup the instruments (generator, analyzer, communication tester).
- 4. Setup the DUT (this step can be performed earlier in the sequence).

Setting up the R&S EX-IQ-Box was covered in a previous chapter; setting up the DUT is completely the user's responsibility. . In this section, we will explain how to set up the hardware and how to set up the measurement instrument as transmitters (IQ sources).

### 5.1 Hardware Setup, Instruments and Signals

Figure 23 shows a recommended hardware setup for the R&S EX-IQ-Box's transmitter mode. (The computer with the *DiglConf* control software is no longer included in the following drawings.)



Figure 23: Instruments and signals in transmitter mode

In transmitter mode, the R&S instruments serve as IQ sources. Typical sources are the R&S SMU, R&S SMJ and R&S AMU standalone generators or the R&S CMW radio communication tester. However, the R&S FSV and R&S FSQ analyzers could also be used for this: They can output down-converted RF signals as real time IQ data streams.

### Dig. IQ from the R&S instrument to the R&S EX-IQ-Box

Connect your IQ source with the R&S EX-IQ-Box's DIG IN/OUT 1 connector. Only use the cable supplied with the R&S EX-IQ-Box.

### Reference frequency

The reference connections of Figure 23 are recommended because this setup works in transmitter mode as well as in receiver mode, using internal clock as well as external clock.

A 10 MHz reference frequency is recommended; this value is most commonly used.

If the R&S EX-IQ-Box is set to external clock you may do without the reference cable from the R&S instrument to the R&S EX-IQ-Box. If set to external clock, signals at the *REF IN* connector are ignored.

If the signal source is a radiocommunication tester which is configured to slow IQ mode you may even do without the reference cable from the DUT to the R&S instrument.

**Notes:** Never connect one reference output with more than one reference input. Do not use T-connectors. Reference inputs have an impedance of 50 ohms. Connecting several devices in parallel might lower the level to such an extent that the reference signal can no longer be detected.

Furthermore, star or daisy-chain structures in the reference path lead to reflections on the cables, which can prevent synchronous work.

The wiring recommendations in this application note avoid such problems.

If you have to split up the reference signal, use power splitters. Check to make sure that the level reduction that this causes does not render the signal insufficient for level control. (A resistive splitter has a 6 dB attenuation).

### Breakout board to the DUT:

Connect the breakout board and DUT with short cables. Avoid cable lengths longer than 30 cm. Since the box is operated in a detached setup away from the R&S instruments via a 2 meter long IQ cable, the box can be positioned close to the DUT.

The cable with the Marker / Strobe signal in Figure 23 on page 23 is only needed if you are working with serial data or with interleaving.

The cable with the UI\_Valid signal in Figure 23 on page 23 is only needed if you are working with parallel data and you have explicitly set the Sample / Clock Ratio in *DiglConf* to a value less than 1.

- Connect each ground point for connectors X2 and X3 at the breakout board directly to ground at the DUT, too. This creates a situation with the same impedances for all data channels, and prevents crosstalk.
- Put the interface into operation in the R&S EX-IQ-Box's test mode. Observe the waveforms of the data and clock signals directly on the DUT with a two-channel oscilloscope. If necessary, optimize the timing by fine-tuning the *Clock Phase* or the *Clock Skew* in the *DiglConf program*.
- ▶ If necessary, terminate the clock cable with resistors.

You will find notes on these points in the *Setup and Hold Times* and *Actual Signal Shapes* chapters on pages 54 and 59.

### 5.2 Generator Setup

The R&S SMU, R&S SMJ and R&S AMU generators are typical IQ sources. Using these R&S generators, you can generate IQ data in real time or run cyclical sequences from an arbitrary waveform generator's memory.

(The following screen shots are from an R&S AMU; there are minor differences in the graphical user interfaces for the R&S SMU and R&S SMJ.)

To use the digital IQ interfaces, you need the R&S SMU-B17 / B18, SMJ-B17 / B18 or AMU-B17 / B18 option.

### Preparations on the R&S EX-IQ-Box:

- Connect the generator, R&S EX-IQ-Box and DUT as shown in Figure 23 on page 23.
- ► Configure your R&S EX-IQ-Box with *DiglConf*.
- Set the *Direction* to *Transmitter*.
- The generator's Word Size is 16 bits. Position the generator word in the R&S EX-IQ-Box's 18-bit space at the place where your data cables are connected (Word Alignment).
- Enter the Clock Rate, even when you are working with an External Clock. The R&S EX-IQ-Box's PLL requires this value to set its capture range.
- Switch State to On.

### Generator configuration:

- Configure your generator so that it generates the desired baseband signal (for example, an LTE downlink).
- On the generator, select the I/Q Out... block, and then click config (see Figure 24).



Figure 24: Digital I/Q output settings in the AMU diagram

- Click Digital I/Q Output Settings. The panel of the same name appears (Figure 25 on page 26).
- Set the Sample Rate Source to Digital I/Q Out.
- Switch the State to On.

Generator output begins (as with output at the user interface).

State	On	
San	nple Rate	_
Source	Digital I/Q Out	-
Value	100.000 000 000	MHz 💌
Sign	al Output	
Set Level Via	PEP	•
PEP	0.00	dBFS 💌
Level	-11.35	dBFS -
Crest Factor (S)	11.35	dB 💌
Crest Factor ((S+N)/S)	11.35	dB 💌
User	Variation	
Variation Active		□ On
Variation Step	1.00	dB 💌
Signal	Monitoring	
No Overflow	٢	
Overflow Hold	Re	eset
Power	On Settings	
Power-On State	I/Q Out Off	•
Conne	cted Device	
ExBox2 (101274) IO IN		

Figure 25: Configuration of the digital I/Q output

Using the IQ interface's protocol, the generator has automatically taken on the sample rate that is derived from the R&S EX-IQ-Box's settings for the *User Interface* (clock, data format etc.). This is the case for both the internal and external clock. It is not possible to edit the *Sample Value*.

► If necessary, change the output power.

### 0 dBFS means full-scale I/Q.

(The generator works with a word size of 16 bits for both I and Q.)

In the bottom field in Figure 25 you can see that the generator with the IQ IN input for the R&S EX-IQ-Box (with the serial number 101274) is connected. This information, too, was automatically supplied via the IQ interface's protocol.

**Notes:** Keep in mind that signal generation has to be activated in the baseband. Otherwise, it is not possible to properly display or set the output power.

The generator's IQ data is generated in real time. It is not possible to stop the data output or run it at a lower clock rate. The automatically set sample rate is the rate at which the generator outputs the IQ pairs.

The *State On/Off* switch in the *DiglConf* program neither starts nor stops the generator's data sequence; it only switches the R&S EX-IQ-Box's output stages to active or to inactive.

### 5.3 Analyzer Setup

The R&S FSV and R&S FSQ analyzers make their IF signal available as a continuous IQ data stream in real time (streaming). To do this, you need the R&S FSV-B17 or R&S FSQ-B17 option.

Unlike oscilloscopes, analyzers input data continuously until a trigger signal stops this process. To endlessly stream IQ data, set the analyzer trigger source to external, without applying a trigger signal.

► First configure your analyzer to achieve ideal signal reception (frequency, span, RBW, reference level, etc.).

The block diagram in Figure 26 shows how the IQ data is derived from the analog IF signal. (The block diagram for the R&S FSQ is almost the same.)



Figure 26: Data acquisition hardware in the R&S FSV

The analyzer's analog IF signal is first digitalized at 128 MHz. After it is broken down into its I- and Q-components, a resampling unit with anti-aliasing and decimation filters uses the results to generate IQ pairs with sample rates that can be set in the range from 100 Hz to 45 MHz (or up to 128 MHz with the FSV-B70 option). These pairs are either stored in the I+Q memory and then processed further, or they are made available at the digital IQ interface.

With the R&S FSQ, the analog IF is digitalized at 81.6 MHz. The sample rate for the IQ pairs at the digital output can be set at a value between 400 Hz and 81.6 MHz.

In both analyzers, automatic downsampling filters prevent aliasing products.

 Connect the analyzer, R&S EX-IQ-Box and DUT together as shown in Figure 23 on page 23.

### Preparation of the R&S EX-IQ-Box:

- Configure your R&S EX-IQ-Box with *DiglConf*.
- ▶ In particular, set the *Direction* to *Transmitter*.
- The analyzers' Word Size is 20 bits. In the R&S EX-IQ-Box, the 18 most significant bits are passed on. If you use a smaller word size, place the word in the R&S EX-IQ-Box's 18-bit space where your data cables are connected (Word Alignment).
- Enter the Clock Rate, even when you are working with an External Clock. The R&S EX-IQ-Box's PLL requires this value in order to establish its capture range.
- Switch State to On.

### **R&S FSV analyzer configuration:**

Continuous output of the IF signal (streaming) is only possible if the RF input is the signal source.

- Press the MODE hardkey, then the IQ ANALYZER softkey, then the SIGNAL SOURCE softkey.
- ▶ Now select *RF Radio Frequency*, see Figure 27.

	🛞 ROI	HDE&	SCHW/	ARZ					FSV •	SIGNAL	ANALYZ	ER	
S	<u> </u>	l Sourc	9									×	IQ Analyzer
F Y	Input I	Path —	Setti	ngs ——									Signal Source RF
	RF R Frequ	adio ency	00	setting	ava	ailah	le						EXIQ
×	IQ Di Base	gital band		secury		inab	ie n	•					Level
											ſ	Close	Data Acquisition
-{	0 dBm					Į.							Display Config
						1.							

Figure 27: Select the R&S FSV's signal input

(If you select the *IQ Digital Baseband* as Input Path the digital IQ output will be deactivated.)

▶ Press the Data Acquisition softkey.

The following window opens:

FSV • S	GIGNAL ANALYZER	
Data Acquisitio	n	IQ Analyzer
Sample Rate:	100.0 MHz	Signal Source
Filter BW:	40 MHz	RF
Meas Time:	20.0 ms	EXIQ
Record Length:	2000000	Level
	Close	Data
الالمربغ بالبالعين المتخليل الجمر والمربية فجاره	فالتربية المنطقية والمقاطعة والمتعارية المطلحان الطريقا	Acquisition

Figure 28: Output Sample Rate for streaming

Enter the desired Sample Rate.

This programs the digital down converter's arbitrary sample rate shown in Figure 26 on page 28.

• Get the required value from the *DiglConf* program's Protocol tab, see Figure 29.

/	Protocol V Data V Clock V Test	
		Protocol
	Format	Parallel
	Data Rate	SDR
	Interleaving	Not Interleaved 💌
	Data Settings	16 Bit / 2's Complement / IQ
	Clock Settings	Internal (BNC REF IN) / 0 deg
	Clock Rate / Sample Rate	100.000 000 000 MHz 100.000 000 MHz

Figure 29: Where to get the Sample Rate value

As IQ sources, the analyzers work in real time; it is not possible to delay or stop the output. If you enter a different sample rate, this will lead to a data overrun or underrun.

Please note that the resampling unit automatically adjusts the downsampling filter's bandwidth to prevent aliasing products. It is not possible to edit the *Filter BW* in Figure 28.

The *Meas Time* and *Record Length* parameters (also in Figure 28) are not relevant for streaming.

Then activate the output:

- Press the DIGITAL OUTPUT softkey.
- Activate the Enable Digital Output Stream check box:

Digital Output	Acquisition
Enable Digital Output Stream	Display Config
Sample Rate: 100 MHz	
Close	
	Digital Output

Figure 30: Starting the streaming

This automatically switches the trigger to external. Ensure that no trigger signal is being applied.

Streaming begins without any notice being shown on the analyzer display. On the contrary: as soon as the trigger is switched to external, the screen content "freezes." This is OK; without a trigger, there is no display updating.

### **R&S FSQ analyzer configuration:**

Just as with the R&S FSV, the R&S FSQ, too, can make its intermediate frequency signals available as a digital IQ data stream.

- Configure your analyzer (frequency, span, RBW, reference level, etc.) in such a way that you achieve ideal reception of your signal.
- Press the MEAS hardkey; then chose NEXT to move into the side menu and press the IQ MODE softkey (see Figure 31).
- ► Switch *IQ MODE* to *ON*, and then press *IQ SETTINGS*. A window of the same name opens (blue in Figure 31).

Here, *IF FILTER BW* is the RBW that has been set. Note that the resampling unit might have automatically reduced the actual bandwidth to prevent aliasing products.

► Enter the desired SAMPLE RATE.

As an IQ source, the R&S FSQ (like the R&S FSV) works in real time. You will find the number value that you need for the *SAMPLE RATE* in the *DiglCinf* program on the *Protocol* tab (see Figure 29 on page 30).

The values for *PRETRIGGER SAMPLES*, *NUMBER OF SAMPLES* and *DATA FORMAT* are not relevant for streaming.



Figure 31: Analyzer configuration for IQ streaming

► Start the data output by pressing the *DIG IQ OUT STREAM* softkey.

This automatically switches the trigger to external. Make certain that no trigger signal is being applied.

Streaming begins without any notice being displayed on the analyzer screen. On the contrary: as soon as the trigger is switched to external, the screen content "freezes." That is OK; without a trigger, there is no display updating.

▶ If necessary, stop the output by pressing DIG IQ OUT STREAM again.

### 5.4 Radio Communication Tester Setup

This section will discuss the R&S CMW radio communication tester configured as a protocol tester. For such tasks, the instrument works through test cases stored on the harddisk.

To use the digital IQ interfaces, the tester requires the R&S CMW-B510A option. With this option, the device has two digital IQ outputs and inputs available.

On the instrument you find test cases for one and for two (IQ) channels; a singlechannel application has been selected as an example for the discussion in this section. The procedure is essentially the same for two-channel cases.

#### Real time operation / Slow IQ mode (non-real time operation)

As a mobile tester, the R&S CMW generates downlink signals and analyzes uplink signals. In general, the *sample rate* relevant for the generation of the modulation data is the mobile radio standard's system clock, multiplied by an oversampling factor. For a WCDMA signal (3.84 MHz system clock) with fourfold oversampling, for example, this leads to a *Sample Rate* of 15.36 Msps.

The R&S CMW can supply this data in real time. However, the R&S CMW can also output or input <u>the same data</u> via the R&S EX-IQ-Box more slowly, for instance at 1 MHz. This mode is called *Slow IQ*.

In this mode, you can also perform measurements on breadboard models that do not yet operate in real time.

To do this, you <u>only</u> need to reduce in *DiglConf* the *Clock* frequency of the *User Interface* to 1 MHz. The FIFO mechanism within the R&S EX-IQ-Box then automatically reduces the transfer quantity between the box and the R&S CMW.

In particular, this requires no changes in the configuration for the R&S CMW. The sample rate you enter on the R&S CMW remains the same (e.g. 15.36 Msps).

#### Hardware setup:

Connect the R&S CMW, R&S EX-IQ-Box and DUT as shown in Figure 23 on page 23. Connect the R&S CMW's DIG IQ OUT 2 with the R&S EX-IQ-Box's DIG IQ IN/OUT 1.

Only use the cable supplied with the R&S EX-IQ-Box.

When you are working in Slow IQ Mode <u>and</u> you are using an external clock, you can do without the reference frequency coupling of the DUT and the R&S instrument. (The FIFO mechanism in the R&S EX-IQ-Box ensures that no data underrun occurs.) In this case, set the radio communication tester to *REF INT*.

### Preparations on the R&S EX-IQ-Box:

- ► Configure your R&S EX-IQ-Box using *DiglConf*.
- ▶ In particular, set the *Direction* to *Transmitter*.
- Set the required Clock Rate. In real time operation, this corresponds to the R&S CMW sample rate. In Slow IQ Mode, it is lower.
- Enter the Clock Rate, even if you are working with an External Clock. The R&S EX-IQ-Box's PLL requires this value in order to be able to establish its capture range.
- ► The R&S CMW's *Word Size* is 16 bits. Place the data word in the R&S EX-IQ-Box's 18-bit space where your data cables are connected (*Word Alignment*).
- Switch the *State* to *On*.

### Configuring the R&S CMW:

Start the Project Explorer on the R&S CMW (see Figure 32).



Figure 32: Test cases in the Project Explorer

Select a test case here.

Now configure the system parameters and the signal paths.

To do this, click in the toolbar on the device icon in order to open the Configuration Dialog:



Figure 33: The path to configuration

This takes you to the System Configuration menu:

UE Connected To	Configuration	on Files						
DIGITAL IQ	test							
			Configuration	is applicable for	all test (	cases		
Connector Settings	Signal Routing Se	lected Te	st Cases 🛛 General Se	attings				
IQ Board 1								
THE TO IN / OUT 1.			LDIG IQ OUT 2-			LAUX A		
Direction	OFF		Direction	OUT		Direction	OFF	~
RAT(s)	LTE		RAT(s)	LTE		Function	None	¥.
Monitor Source	NONE	×.	Monitor Source	NONE	140	Glock Freq. [MHz]	100.0	
Sample Rate	15.36 Msps	×	Sample Rate	15.36 Msps	~	,		
Start Source	Auto Internal	¥	Start Source	Auto Internal	×	FAUX B		
Enable Source	Auto Internal	*	Enable Source	Digital IQ Out	~	Direction	OFF	~
Additional Filter	None	×.	Additional Filter	None	140	Function	None	×.
Connected Device			Connected Device			Clock Freq. [MHz]	100.0	
EIGIQIN/OUT3-			-DISTQ OUT +			Direction Sottings		
Direction	OFF		Direction	OFF		Downlink Only		
RAT(s)			RAT(s)					
Monitor Source	NONE	×	Monitor Source	NONE	2			
Sample Rate	100.0 Msps	×.	Sample Rate	100.0 Msps	140			
Start Source	Auto Internal	×	Start Source	Auto Internal	.92			
Enable Source	Auto Internal	×	Enable Source	Auto Internal	*			
Additional Filter	None	v	Additional Filter	None	~			
Connected Device			Connected Device					

Figure 34: Setting for downlink only

- Set (in the top left) UE Connected To to DIGITAL IQ.
- Activate the checkbox Downlink Only.
- Enter your Sample Rate. This rate is determined by the mobile radio standard. In general, the Sample Rate is the standard's system clock, multiplied by an oversampling factor.
- Set Enable Source to Digital IQ-Out.

You have now defined the calculation of the output data and selected the IQ output.

▶ Now click on the Signal Routing tab.

Connector Settings Signal R	outing Selected Test Case	es General Settings						
	OUT		IN					
1 SUW [WCDMA,LTE]								
IQBoard 1	DIG IQ 2	DIG IQ 4	DIG IQ 1	DIG IQ 3				
IL_001 Cell Setup	LTE		LTE					

Figure 35: Input / Output routing

Make sure that your test case uses the DIG IQ OUT 2 port.

Click the General Settings tab:

Connector Settings Signal Routing	Selected Test Cases	General Settings			
Reference Frequency			External Trigger		
Frequency Source	External	~	TRIG A	OFF	~
Ext. Ref. Frequency [MHz]	10.0		TRIG B	OFF	~

Figure 36: Synchronization of the R&S CMW and DUT

If you work in Slow IQ mode, you may set the *Frequency Source* to *Internal*. Otherwise:

► Set the Frequency Source to External.

**Note:** The CMW Radiocommunication Tester accepts input reference frequencies from 1 MHz (squarewave) or 10 MHz (sine) to 80 MHz. The resolution is 1 Hz.

- ► Close the System Configuration menu.
- Save the System Configuration.

When you start a test case, the *System Configuration* loads from the hard disk. If you have forgotten to save your configuration, the last stored configuration overwrites your current settings.

Start the test case via the Run test project icon in the toolbar:

San	nple	_Scr	n.tpd	[C:	Rohde	-Schv	warz	Sce	nari	os\1	5.11	APPL	MLA
Ū	~	Y	<del>8</del> 8	8			Þ	41	10-	0	86	86	1
							R	un te	est pr	ojec	t]		

Figure 37: Running the test

Some test cases expect a hardware trigger at the digital IQ interface's AUX A or AUX B jack.

In such a case, activate the start via a signal applied here.

Data output begins.

### 6 Receiver Mode: How to Analyze DUT Data

In receiver mode, the same steps as in transceiver mode are used to prepare a data transmission between the DUT and R&S instruments:

- 1. Setup the Hardware: Connect the instruments, the R&S EX-IQ-Box and the DUT
- Setup the R&S EX-IQ-Box: Configure the R&S EX-IQ-Box with the DiglConf program
- 3. Setup the instruments (generator, analyzer, communication tester)
- 4. Setup the DUT (this step can be performed earlier in the sequence).

Setting up the R&S EX-IQ-Box was covered in Chapter 3; setting up the DUT is completely the user's responsibility. In this section, we will explain how to set up the hardware and how to set up the measurement instrument as a receiver (IQ sink).

### 6.1 Hardware Setup, Instruments and Signals

Figure 38 shows a recommended hardware setup for the R&S EX-IQ-Box's receiver mode. (The computer with the *DiglConf* control software is not included in these illustrations.)



Figure 38: Instruments and signals in receiver mode

For analysis of the data sent from the DUT, the R&S EX-IQ-Box works in receiver mode; the R&S instruments serve as IQ sinks. The IQ data will usually be analyzed by an R&S analyzer or by an R&S CMW communication tester. Many R&S generators can also (optionally) be equipped with IQ inputs to add impairments, fading or AWGN in real time. These post-processed IQ signals can then be up-converted into the RF band or, be outputted digitally and, for instance, looped back into the radio communication tester.

Dig. IQ from R&S instrument to the R&S EX-IQ-Box:

Connect your IQ sink with the R&S EX-IQ-Box's DIG IN/OUT 2 connector. Only use the cable supplied with the R&S EX-IQ-Box.

### Reference frequency

The reference connections of Figure 23 are recommended because this setup works in transmitter mode as well as in receiver mode, using internal clock as well as external clock.

A 10 MHz reference frequency is recommended; this value is most commonly used.

If the R&S EX-IQ-Box is set to external clock you may do without the reference cable from the R&S instrument to the R&S EX-IQ-Box. If set to external clock, signals at the *REF IN* connector are ignored.

If the signal source is a radiocommunication tester which is configured to slow IQ mode you may even do without the reference cable from the DUT to the R&S instrument.

• Observe the notes on reference wiring in Chapter 5.1 on page 23.

### Breakout board to the DUT:

Connect the breakout board and DUT with short cables. Avoid cable lengths longer than 30 cm. Since the box is operated in a detached setup away from the R&S instruments via a 2 meter long IQ cable, the box can be positioned close to the DUT.

The cable with the Marker / Strobe signal in Figure 23 on page 23 is only needed if you are working with serial data or with interleaving.

UI\_Valid on the R&S EX-IQ-Box's user interface serves as a gate signal. The R&S EX-IQ-Box only reads in data only when UI\_Valid has a high level. If the port is not connected, an internal pull-up resistor keeps UI\_Valid on "high."

Connect each ground point for connectors X2 and X3 at the breakout board directly to ground at the DUT, too. This creates a situation with the same impedances for all data channels, and prevents crosstalk.

- Put the interface into operation in the R&S EX-IQ-Box's test mode. Observe the waveforms of the data and clock signals directly on the breakout board with a two-channel oscilloscope. If necessary, optimize the timing by fine-tuning the Clock Phase or the Clock Skew in the DiglConf program.
- ▶ If necessary, terminate the clock cable with resistors.

You will find notes on these points in the *Setup and Hold Times* and *Actual Signal Shapes* chapters on pages 54 and 59.

### 6.2 Analyzer Setup

Without additional options (except for the digital IQ interface) the R&S FSV analyzes digital IQ data with regard to its:

- Magnitude
- Spectrum
- IQ vector
- Real / Imag (I/Q)

This is accomplished by simply switching the input path from *RF Radio Frequency* to *Baseband Digital.* 

The R&S FSQ analyzer cannot evaluate digital IQ data in this way.

However, both instruments can be fitted with instrument options which evaluate data from the digital baseband input. Such options are, for example, the Vector Signal Analysis (VSA) and the personalities for mobile standards such as GSM, CDMA2000, WCDMA, and LTE.

Figure 39 shows a block diagram of the baseband acquisition hardware of the analyzers.



Figure 39: Digital baseband acquisition hardware of the R&S FSV

Both the R&S FSV and the R&S FSQ analyzers resample the incoming digital IQ data.

To make this possible, you have to enter an *Input Sample Rate* (on the R&S FSV, a *Sample Rate* on the R&S FSQ), because the data from the digital baseband input comes without any time information.

An absolute Full Scale Level has also to be entered on the analyzers.

For the direct analysis (R&S FSV only) with regard to Magnitude, Spectrum, IQ-Vector, and Real / Imag I/Q you can define the resample rate.

For the evaluation by instrument personalities (R&S FSV and R&S FSQ) the resample rate is individually fixed.

### Preparation on the R&S EX-IQ-Box / in DiglConf:

- Connect the analyzer, R&S EX-IQ-Box and DUT as shown in Figure 38.
- ► Configure your R&S EX-IQ-Box with *DiglConf*.
- ▶ In particular, set the *Direction* to *Receiver*.
- The analyzers' Word Size is 20 bits. In the R&S EX-IQ-Box, the 18 most significant bits are passed on. If you use a smaller word size, place the word in the R&S EX-IQ-Box's 18-bit space where your data cables are connected (Word Alignment).
- Enter the Clock Rate, even when you are working with an External Clock. The R&S EX-IQ-Box's PLL requires this value in order to establish its capture range.
- Switch State to On.

Configuring R&S FSV evaluating IQ data directly with regard to Magnitude, Spectrum, IQ-Vector, and Real / Imag (I/Q):

- Press the MODE hardkey, then the IQ ANALYZER softkey, then the SIGNAL SOURCE softkey.
- Select the *IQ Digital Baseband* as Input Path.

<b>ROHDE&amp;S</b>	CHWARZ	FSV • SIGNAL ANALYZER	
<u>N</u> Signal Source			IQ Analyzer
RF Radio Frequency	Settings Connected Device: Input Sample Rate Full Scale Level: Level Unit:	ExBox2 :: [15.36 MHz 1.0 V V ¢	Signal Source RF EXIQ Level
Baseband	Adjust Referen	ce Level to Full Scale Level Close	Data Acquisition Display

Figure 40: Select the signal input for the R&S FSV

**Note:** If *IQ Digital Baseband* is selected as input path, the instrument's IQ output will be deactivated.

- ► For the *Input Sample Rate,* enter the value corresponding to real time. (For mobile radio signals, it is the system clock multiplied by the oversampling factor.)
- ▶ Use the Full Scale Level to define the display scaling.

1  $V_{\text{RMS}}$  corresponds to 13.01 dBm at 50 ohms.

Depending on which trigger and sweep you have set, the analyzer might already be measuring and displaying the results on the screen. Select your result representation:

I	Q Analy:	zer 🔿	D					T	IQ Analyzer
dBm	Freq	4 0.0 Hz F	AQT Rec Lengtł	21.6 µs n 332	SRate	15.36 MH	lz		Signal Source DIG IQ
							splay Config Aagnitude	3ur 🔀	EXIQ
			<u>አ</u> ለ	• • • •	0	) () () () () () () () () () () () () ()	Gpectrum Q-Vector		Level
		$\sim$			$\mathbb{N}$	E F	Real/Imag	(I/Q)	Data Acquisition
									Display Config
									Digital Output
									Digital Baseband Info
Λ	~		691	pts	Δ		Span 15	5.36 MHz	

Click on the Display Config softkey.

Figure 41: Signal representation of the digital baseband input

To optimize the display representation

 Click Data Acquisition and enter your Sample Rate for the fractional resampling unit, see Figure 39 on page 38.

FSV • S	GIGNAL ANALYZER	
Data Acquisitio	n 🔀	IQ Analyzer
Sample Rate:	10.0 MHz	Signal Source
Filter BW:	6.25 MHz	DIGIQ
Meas Time:	20.0 ms	EXIQ
Record Length:	200000	Level
	Close	
		Data

Figure 42: Setting of the fractional resampler

To prevent aliasing products this automatically adjusts the filter bandwidth. For more details, see [7].

### Configuring R&S FSV evaluating IQ data by instrument options:

- ▶ Press the *MODE* hardkey.
- ▶ Select your instrument option, e.g. 3G FDD BTS.
- ▶ Press the *Input / Output* hardkey.
- Select the IQ Digital Baseband as Input Path.
- ► For the *Input Sample Rate,* enter the value corresponding to real time. (For mobile radio signals, it is the system clock multiplied by the oversampling factor.)
- ▶ Use the Full Scale Level to define the display scaling.

1  $V_{\text{RMS}}$  corresponds to 13.01 dBm at 50 ohms.



Figure 43: Dig. IQ DataEvaluation by the 3GPP BTS option

Each instrument personality has its own fixed resampling rate which is hidden to the user. You don't have to enter a value as in Figure 42 on page 40.

### Configuring R&S FSQ evaluating IQ data by instrument options:

- ► Select your instrument option, e.g. 3G FDD BTS.
- Press the SETUP hardkey then the SIGNAL SOURCE and BASEBAND DIGITAL softkeys (see Figure 44).

VSA/		
Ļ	RF PATH	
SETUP	BASEBAND ANALOG	
SIGNAL SOURCE	BASEBAND DIGITAL	→ DIGITAL IN FULL SCALE
	DIGITAL BB INFO	DIGITAL IN SAMPLERATE
	EX-IQ-BOX	

Figure 44: Configuring the FSQ for a digital baseband source

► Use the *FULL SCALE* to define the display scaling.

1  $V_{\text{RMS}}$  corresponds to 13.01 dBm at 50 ohms.

- ► For the *Input SAMPLERATE*, enter the value corresponding to real time. (For mobile radio signals, it is the system clock multiplied by the oversampling factor.)
- Return to the personality. Start your measurements just as you would start measurements for RF signals.

### 6.3 Generator Setup

The baseband inputs from the R&S SMU, R&S SMJ and R&S AMU work in real time. For this reason, it does not make sense to control the input of data via a gate signal at the R&S EX-IQ-Box's UI\_Valid port.

To use the digital IQ interfaces, you need the R&S SMU-B17 / B18, SMJ-B17 / B18 or AMU-B17 / B18 option.

Connect the generator, the R&S EX-IQ-Box and the DUT as described in Chapter 6\_1 on page 36.

### Preparations on the R&S EX-IQ-Box:

- ► Configure your R&S EX-IQ-Box with *DiglConf*.
- ▶ In particular, set the *Direction* to *Receiver*.
- The generator's Word Size is 16 bits. Place the generator word in the R&S EX-IQ-Box's 18-bit space where your data cables are connected (Word Alignment).
- ► Enter the *Clock Rate*, even when you are working with an External Clock. The R&S EX-IQ-Box's PLL requires this value in order to establish its capture range.
- Switch State to On.

### Generator configuration:

(The following screen shots are from an R&S AMU; there are minor differences in the graphical user interfaces for the R&S SMU and R&S SMJ.)

- Select the *I/Q IN...* block on the generator.
- ► Click *config*, see Figure 45.



Figure 45: R&S AMU baseband input

State	On	On						
Mode	Digital Input	•						
/Q Swap		□ On						
	Sample Rate							
Source	Digital I/Q In	•						
Value	100.000 000 000	MHz 💌						
Bas	eband Input Level							
Measurement Period	2	s 💌						
Auto Level Set								
Crest Factor	3.01	dB 💌						
PEP	-0.02	dBFS 💌						
Level	-3.03	dBFS 🔻						
Si	gnal Monitoring							
No Overflow	•							
Overflow Hold	🔷 📃 Re	set						
Co	nnected Device							

► Click Baseband Input Settings. The panel of the same name appears:

Figure 46: Configuring the R&S AMU baseband input

- Set the Mode to Digital Input.
- Set the Sample Rate Source to Digital I/Q In
- Switch State to On.

The generator automatically takes on the sample rate that is derived from the R&S EX-IQ-Box's settings. This is the case for both the internal and external clock.

Establish the level scale:

Click Auto Level Set.

This measures the digital IQ signal that is currently being applied. The *Measurement Period* determines the length of the measurement. After that, a standardization takes place, so that the PEP value does not exceed 0 dBFS.

The signal used here has a crest factor of approximately 3 dB. For full-scale input, the RMS level has been lowered to the corresponding level.

In the last field in Figure 46 on page 44, you can see that the generator with the IQ OUT output for the R&S EX-IQ-Box (with the serial number 101274) is connected. This information was automatically supplied via the IQ interface's protocol.

**Notes:** Make sure that the DUT is actually outputting data and the R&S EX-IQ-Box is inputting it. To do this, use the transient recorder (see page 18). Otherwise, the output power cannot be measured properly.

*State On* or *Off* in the *DiglConf* program starts or stops the data transmission to the generator.

### 6.4 Radio Communication Tester Setup

This section will discuss the R&S CMW radio communication tester configured as a protocol tester. For such tasks, the instrument works through test cases stored on the harddisk.

To use the digital IQ interfaces, the tester requires the R&S CMW-B510A option. With this option, the device has two digital IQ outputs and inputs available.

On the instrument you find test cases for one and for two (IQ) channels; a singlechannel application has been selected as an example for the discussion in this section. The procedure is essentially the same for two-channel cases.

As a mobile tester, the R&S CMW can either only generate downlink signals or generate downlink signals and analyze uplink signals. (Uplink-only is not available). This makes sense, because a mobile device must match its frame timing to fit exactly into the downlink signal's frame timing.

This seams not possible at first with uplink-only setups.

However, the R&S CMW can properly analyze the uplink signal if the data from the DUT begins exactly with the slot start. To make this possible, the DUT must supply a slot-start signal that, as a gate signal, controls the user interface's UI\_Valid. A high level at UI\_Valid starts the data transmission to the R&S CMW with the next clock.

### Real time operation / Slow IQ mode (non-real time operation)

As a mobile tester, the R&S CMW generates downlink signals and analyzes uplink signals. In general, the *sample rate* relevant for the generation of the modulation data is the mobile radio standard's system clock, multiplied by an oversampling factor. For a WCDMA signal (3.84 MHz system clock) with fourfold oversampling, for example, this leads to a *Sample Rate* of 15.36 Msps.

The R&S CMW can supply this data in real time. However, the R&S CMW can also output or input the same data via the R&S EX-IQ-Box more slowly, for instance at 1 MHz. This mode is called *Slow IQ*.

In this mode, you can also perform measurements on breadboard models that do not yet operate in real time.

To do this, you <u>only</u> need to reduce in *DiglConf* the *Clock* frequency of the *User Interface* to 1 MHz. The FIFO mechanism within the R&S EX-IQ-Box then automatically reduces the transfer quantity between the box and the R&S CMW.

In particular, this requires no changes in the configuration for the R&S CMW. The sample rate you enter on the R&S CMW remains the same (e.g. 15.36 Msps).

#### Hardware setup:

- Connect the R&S CMW, R&S EX-IQ-Box and DUT as shown in Chapter 6\_1 on page 41. Connect the R&S CMW's DIG IQ IN/OUT 1 with the R&S EX-IQ-Box's DIG IQ IN/OUT 2. Only use the cable supplied with the R&S EX-IQ-Box.
- ► Feed UI\_Valid in Figure 38 with a slot-start signal.

#### Preparations on the R&S EX-IQ-Box:

- Configure your R&S EX-IQ-Box with DiglConf.
- ▶ In particular, set the *Direction* to *Receiver*.
- Set the required Clock Rate. In real time operation, this corresponds to the R&S CMW's sample rate. In slow IQ mode, it is lower.
- Enter the Clock Rate, even when you are working with an External Clock. The R&S EX-IQ-Box's PLL requires this value in order to establish its capture range.
- The R&S CMW's Word Size is 16 bits. Place the data word in the R&S EX-IQ-Box's 18-bit space where your data cables are connected (Word Alignment).
- Switch State to On.

### Configuring the R&S CMW:

Start the Project Explorer on the R&S CMW (see Figure 47):

🖃 🖓 Test Project Description
🖶 🖬 LTE Test Project
🖃 🔚 Test Sequences
🕒 🔽 🗄 LTE Tests
🕀 🔁 Test Cases
🔤 🔽 🖬 II_001 Cell Setup
🔲 🖬 ml_001 Cell Setup
🔤 🛄 🖬 ml_002 EPS Bearer Setup
🔤 🔽 ml_003 MT call with data generator

Figure 47: Test cases in the Project Explorer

Select a test case here.

Now configure the system parameters and the signal paths.

• Click in the toolbar on the device icon in order to open the Configuration Dialog:

in ∧ ∨ 號 (		⊳	41	10-	0		86	
	 0	pen :	5yste	em C	onfig	urati	on Dia	alog.

Figure 48: The path to configuration

This takes you to the System Configuration menu:

UE Connected To-	Configuration	on Files							
DIGITAL IQ	✓ test								ß
			Configuration	is applicable for	all test	cases			
Ionnector Settings	Signal Routing Se	lected Te	st Cases   General Se	ettings					
IO Board 1									
DIG IQ IN / OUT 1			DIG IQ OUT 2						
Direction	IN		Direction	OUT		Direction	OFF	~	Ĩ
RAT(s)	LTE		RAT(s)	LTE		Function	None	~	
Monitor Source	NONE	~	Monitor Source	NONE	~	Clock Freq. [MHz]	100.0		
Sample Rate	15.36 Msps	~	Sample Rate	15.36 Msps	~	1			
Start Source	Auto Internal	~	Start Source	Auto Internal	~	FAUX B			
Enable Source	Auto Internal	~	Enable Source	Digital IQ Out	~	Direction	OFF	~	
Additional Filter	None	~	Additional Filter	None	~	Function	None	~	
Connected Device			Connected Device			Clock Freq, [MHz]	100.0		
DIG IQ IN / OUT 3			PDIG IQ OUT 4			PDirection Settings-			
	OFF		Direction	OFF	(	Downlink Only			
RAT(s)			RAT(s)						
Monitor Source	NONE	~	Monitor Source	NONE	~				
Sample Rate	100.0 Msps	~	Sample Rate	100.0 Msps	~				
Start Source	Auto Internal	~	Start Source	Auto Internal	~				
Enable Source	Auto Internal	$\sim$	Enable Source	Auto Internal	~				
Additional Filter		in the second	Additional Filter		1757				[

Figure 49: Setting for downlink only

- Set (in the top left) UE Connected To to DIGITAL IQ.
- Deactivate, when applicable, *Downlink Only*.
- Enter your Sample Rate for the uplink and downlink. This rate is determined by the DUT. It generally corresponds to the system clock of the mobile radio standard, multiplied by the oversampling factor.
- Set Enable Source to Digital IQ-Out.

You have now defined the calculation of the output data and selected the IQ input and output.

► Click on the Signal Routing tab.

Connector Settings Signal Routing	Selected Test Cases Ge	eneral Settings			
A					
	OUT		IN		
1 SUW [WCDMA,LTE]					
IQBoard 1	DIG IQ 2	DIG IQ 4	DIG IQ 1	DIG IQ 3	
I_001 Cell Setup	LTE		LTE		
I see a second of the set of the second seco					

Figure 50: Input / Output routing

▶ Make sure that your test case uses the DIG IQ OUT 1 port.

Click the General Settings tab:

Connector Settings Signal Routing	Selected Test Cases	General Settings			
Reference Frequency			External Trigger		
Frequency Source	External	~	TRIG A	OFF	~
Ext. Ref. Frequency [MHz]	10.0		TRIG B	OFF	~
·					

Figure 51: Synchronization of the R&S CMW and DUT

Set the Frequency Source to External, and enter your Ext. Ref. Frequency.

- ► Close the System Configuration menu.
- Save the System Configuration.

When you start a test case, the *System Configuration* loads from the hard disk. If you have forgotten to save your configuration, the last stored configuration overwrites your current settings.

Start the test case via the *Run test project* icon in the toolbar:

_Sar	nple	_Scr	n.tpd	[C:\	Rohde	-Schv	varz	Sce	nari	os\1	5.11	APPL	.WLA
Ū	~	¥	<del>8</del> 8	8			Þ	41	10-	0		86	1
							R	un te	est pi	rojec	t		

Figure 52: Running the test

Some test cases expect a trigger at the digital IQ interface's AUX A or AUX B.

▶ In such a case, activate the start via a signal applied here.

The recording starts.

### 7 Mixed Mode: How to Stimulate and Analyze DUT Data

Figure 53 shows a combination of the application cases for transmitter mode and receiver mode. The IQ data source is the R&S SMU vector signal generator, the IQ data sink is the R&S FSQ signal analyzer.



Figure 53: DUT between the IQ transmitter and IQ receiver

### **Reference frequency**

A *REF IN* signal is only required for R&S EX-IQ-Box(es) that are operated using the *Clock Internal* setting.

If both boxes need a reference signal, they share the generator's REF OUT signal without reflections through a resistive power divider as shown in Figure 53. This divider reduces the signal level by 6 dB. Nonetheless, for the R&S EX-IQ-Boxes (with higher input sensitivity) the generator reference signal is reliably sufficient.

The transmitter and receiver branches are independent of one another. You can, for instance, operate R&S EX-IQ-Box 1 with the internal clock and R&S EX-IQ-Box 2 with an external clock. The clock and the sample rates, the data formats and the timing settings can also differ.

The generator in the TX branch always works in real time. The analyzer can feed in data both in real time or in slow IQ mode.

A PC with the *DiglConf* program controls both boxes (PC not shown in Figure 53).

Put the transmitter and receiver unit into operation one after the other as described in the previous chapters.

Figure 54 shows a typical application for testing a mobile radio chip. The R&S CMW radio communication tester generates a downlink signal and analyzes the uplink signal of the DUT.



Figure 54: DUT between the R&S CMW's IQ input and output

R&S EX-IQ-Box 1 works in transmitter mode and R&S EX-IQ-Box 2 in receiver mode. Again, a PC that is running *DiglConf* controls both boxes (not shown in Figure 54). A *REF IN* signal is only needed for the R&S EX-IQ-Box(es) that are operated using the *Internal Clock* setting.

If both boxes need a reference signal, they share the generator's REF OUT signal without reflections through a resistive power divider as shown in Figure 54. For the R&S EX-IQ-Boxes, the R&S CMW's reference signal is reliably sufficient.

Again, it makes sense to proceed step by step as described in the sections that cover the TX and RX modes.

Begin with the downlink, then tackle the uplink.

### 8 Testing the User Interface

A test mode has been implemented in the R&S EX-IQ-Box and *DiglConf* software. This function can be used to examine the interface to the DUT without R&S generators, analyzers, or radiocommunication testers.

With this feature, you can perform a check in both transmitter mode and receiver mode to see if the data transfer is being accomplished without errors and determine if the setup and hold times are being maintained.

The test setup is reduced to a minimum (see Figure 55).



Figure 55: Small setup for the test mode

The connection made between the breakout board and the DUT is the same as the one that will be used later in the application. The setup shown in Figure 55 is equally sufficient for the TX and for the RX test.

If you are working with an external clock, the reference connection is not required. Also use this mode if the DUT cannot provide a suitable reference frequency.

### TX test

In TX test mode, the R&S EX-IQ-Box generates a continuous output signals.

First, completely configure your R&S EX-IQ-Box using the *DiglConf* program. For now, you can leave the *Clock Phase* and the *Clock Skew* at the default settings.

In the DigIConf program's main window, set the direction to Transmitter and open the Test tab. The TX Test window appears (see Figure 56).

		EX-IQ-BOX 1 (101274): User Defined					
t To Default	Set	-	3.3V CMOS	Logic Type	On		State
ve/Recall	Save	-	Transmitter	Direction			
On				1	Clock VTest	ol V Data V	Protoco
s J	PRBS					Signal	Test Si
	PRB					Signal	Test Si

Figure 56: TX Test: Select the pattern and go

You now have a choice between three test signals: PRBS, counter, and sine.

*PRBS* supplies the pseudo-random bit sequence 16 on the data cables. It is primarily used to check the reliability of the data transmissions in long-term tests. The I-data and Q-data are the same. The test output is according to the setting you made under the *Protocol* tab. E.g. if the word size is set to 7 bit the sequence is output in pieces of 7 bits. For information about the building polynomial, see [1].

*Counter* generates an sequence of ascending binary numbers. The I-data and Q-data are the same.

*Sine* supplies sampled values from a sinus signal. The word size that is set on the *Data* tab determines the number range. I-traces and Q-traces have a 90-degree phase shift.

Switch Tx Test to On.

Pattern output begins.

- Use the counter signal to check the connections you have made. Use an oscilloscope to examine all data cables: The LSB changes with the clock frequency, the next-higher bit with half the clock frequency, etc.
- Use the counter signal to check the setup and hold times, too. The periodic nature of the signals provides you with a stable display on the oscilloscope screen. Measure at the transfer point to the DUT. If necessary, optimize the clock phase and clock skew to ensure a reliable data transfer (see the chapter on Setup and Hold Times on page 54).

- Check whether the DUT reads in the R&S EX-IQ-Box's data without error. Therefore it is necessary to check the output of the DUT input registers, not the signals at the DUT input. (How you accomplish this depends on your design and control software. No hints can be given here.)
- Examine the data transmission in test mode at higher temperatures as well. In general, semiconductor chips have poorer reaction times when they heat up.

### RX test

In the RX test mode, the R&S EX-IQ-Box expects defined input patterns, compares them with patterns that have been generated internally, and counts any errors that arise.

- ► First, completely configure your R&S EX-IQ-Box with the *DiglConf* program. For the time being, you can leave the *Clock Phase* and the *Clock Skew* at the default values.
- ► In the *DiglConf* program's main window, set the direction to *Receiver* and open the *Test* tab. The RX Test window appears (see Figure 57).

EX-IQ-BOX 1	(101274): Use	8				
State	On	Logic Type	3.3V CMOS	•	Set To De	fault
		Direction	Receiver	•	Save/Rec	all
Protocol VDa	ata VClock VT	est \			0	n
Test Signal					PRBS	•
IQ Words					10	83 284 995
Rx BER						5.04 E-01

Figure 57: RX test: BER algorithm implemented

Two predefined test signals can be evaluated: PRBS and Counter.

*Counter* expects a data word that is incremented with every clock; *PRBS* expects the pseudo-random bit sequence 16. This sequence is described in detail in the R&S EX-IQ-Box manual [1].

- If cable connection problems or short circuits arise, Counter signals lead to constant bit error rates. Varying rates while using Counter signals point to insufficient setup times or hold times.
- If you measure a bit error rate (BER) of 50 % for a PRBS pattern, this means that no data at all has been received properly. In this case, the evaluation logic in the R&S EX-IQ-Box was not able to synchronize. (Due to the statistical rectangular distribution, half of the bits appear to be correct). In this case, check the cables, bit order, clock source, clock rate and timing.

- Varying bit error rates < 50 % are generally caused by insufficient setup times or hold times. However, disconnected signal cables and short circuits could also be responsible.
- Check the data transmission in the test mode at higher temperatures as well. In general, semiconductor chips have poorer reaction times when they heat up.

### 9 Setup and Hold Times

This chapter covers the timing of synchronous data transmission. Synchronous means that a clock signal is supplied along with the data which controls the data acquisition.

For clock rates below about 30 MHz normally no problems arise. For these low rates

- Switch the Clock Phase to 180 deg. in the DiglConf program if you use Single Data Rate (SDR), see Figure 58.
- Switch the *Clock Phase* to 90 deg. if you use Double Data Rate (DDR).

R&S	→ Clock ] ← I Data <u>}</u>		
EX-IQ-BOX	(Q Data)	χ_	χ

Figure 58: Safe Clock Phase for low data rates

For low as well as for high clock rates

Always check the clock signal using an oscilloscope with a bandwidth of at least 500 MHz. Inspect the signal at that point where the data is logged in, also see section 10 on page 59. This point is the DUT input for the transmitter mode; it is the breakout board for the receiver mode.

The clock edges have to be "clean" without any uncertainty in the level range around the threshold. There should be no ringing and no crosstalk on the signal.

If you observe such impairments, terminate the clock line using two resistors, see Figure 68 on page 61.

For higher clock rates the setup and hold times should be carefully checked.

The discussion below applies regardless of whether parallel or serial data is being transmitted or whether single-ended or differential breakout boards are used.

Initially, it is assumed that the signals are ideal (have steep edges). In practice, however, the cables that are used tend to weaken the signal transitions so that additional time delays can be expected. The chapter entitled *Actual Signal Shapes*, on page 59, covers that.

Here, we assume ideal cables between the breakout board and the DUT. We only take their signal propagation time into consideration.

Use short cables between the breakout board and the DUT. We recommend not exceeding a cable length of 30 cm.

The signal delay across a 30 cm long cable is approximately 1.5 ns (at  $\varepsilon_r = 2.2$ ).

We must differentiate between four different scenarios:

- Transmitter mode, internal clock
- Receiver mode, external clock
- Transmitter mode, external clock
- Receiver mode, internal clock

In the first two cases, the clock and data flow in the same direction; timing proves to be uncritical with regard to time requirements. In the other two cases, the delays add up unfavorably; more care needs to be taken.

### Transmitter mode, internal clock

In this case, the data and clock come from the EX\_IQ\_Box (see Figure 59).



#### Figure 59: Case 1 - TX, internal clock

In general, that data pattern is logged in which is present before the active clock edge. In the following discussion, we are assuming that the rising edge is the active one.

Figure 59 shows the signals the DUT. Since the clock and data signals flow in the same direction, the cable propagation time does not influence the time relationship between the signals. Data changes after the internal delay within the R&S EX-IQ-Box, which is typically 1 ns.

The DUT requires stable data during its acquisition window (green in Figure 59), which is compromised of the setup and hold time. Typical values for this are 2 ns for the setup time and 0 ns for the hold time.

► Here, take your DUT's actual requirements into consideration.

The acquisition window is permanently coupled with the clock edge. If the hold time is insufficient, you can use the *Clock Skew* parameter to shift the clock edge in relation to the data transfer using the *DiglConf* program (see Figure 60).



Figure 60: Clock shifted by 90 °

Positive values for the *Clock Skew* shift the clock to the "left" (which delays the data phase). You also can cope with hold times < 0.

It is easy to stay within the setup time.

### Receiver mode, external clock

Figure 61 shows the signals on the breakout board. The data and clock come from the DUT. Here, the situation is similar to the previous case. The clock and data flow in the same direction; as a result, the cable propagation time does not change anything in the time relationship between the signals. Here, data changes after to the internal delay in the DUT.



Figure 61: Case 2 - RX, external clock

The R&S EX-IQ-Box's acquisition window is shown in blue in Figure 61. Since the hold time is approximately 0 ns, it is only necessary to stay within the setup time (theoretically < 1 ns). There is no problem.

### Transmitter mode, external clock

Figure 62 shows the signals on the DUT. The DUT's clock appears, after the cable propagation time, at the R&S EX-IQ-Box. This changes the data after the box's internal reaction time. The data reaches the DUT after the cable propagation time.



Figure 62: Case 3 - TX, external clock

The *Delay* shown here can be calculated as the sum of the:

Cable propagation time (approx. 1.5 ns) + Reaction time for the R&S EX-IQ-Box (typ. 1 ns) + Cable propagation time (approx. 1.5 ns)

The DUT's acquisition window is – regardless of the *Delay* mentioned above – tied to its own clock edge. Prior to this delay, during the DUT's setup time, the data must be applied in a stable manner.

At the maximum clock frequency of 100 MHz, the data transfer takes place every 10 ns. With ideal signals, the sum of the delay and setup time remains well below this value. Nonetheless, in reality, the signal edges flatten, which leads to an additional time delay for the clock and for the data. Both elements add together with destructive results: The R&S EX-IQ-Box transfers the data later; in addition, the data signals on the DUT settle at a later point in time.

A problem could arise, if the sum of the actual delay and the DUT setup time reaches or exceeds 10 ns (see Figure 63).



Figure 63: Delay + setup time reaches clock period

In this case, the data is not stable during the DUT's setup time.

To solve this problem, use the *Clock Skew* parameter in *DiglConf* program to shift the clock edge to the "right" virtually. You can accomplish this with negative values for the *Clock Skew*. (In practice, this means that the data change is delayed to such an extent that the previous data word falls properly into the window.)

In this case, short cable lengths are particularly important.

### Receiver mode, internal clock

A similar situation arises when the clock is supplied by the R&S EX-IQ-Box in receiver mode.

Figure 64 shows the situation at the transfer point, the breakout board.



Figure 64: Case 4 - RX, internal clock

The clock reaches the DUT after the cable propagation time. The DUT changes the data after its internal reaction time. In turn, the data reaches the R&S EX-IQ-Box after the cable propagation time.

The delay shown here is calculated as the sum of the:

Cable propagation time (approx. 1.5 ns) + DUT's reaction time + Cable propagation time (approx. 1.5 ns).

If you are working with a data period of 10 ns and the sum of the actual delay and the R&S EX-IQ-Box setup time exceeds this value, you can solve this problem by using the *DiglConf* program to shift the clock edge to the "right" virtually. You can accomplish this with negative values for the *Clock Skew*.

Short cable lengths are also particularly important in this case.

In cases in which time is critical, inspect the actual relationship between the data and the clock at the given transfer point. The next chapter will provide you with additional information about how to do this.

### 10 Actual Signal Shapes

In the previous chapter, we assumed the presence of ideal signals. In practice, neither DUTs nor the R&S EX-IQ-Box generate signals with ideally steep level transitions. In addition, the cables between the data transmitter and receiver and the RX input capacitance weaken the edges significantly.

Even though theoretical examinations of the setup and hold times would appear to ensure a trouble-free data transfer, inspecting the actual signals and the timing of the clock and data at the specific transfer point is absolutely necessary. Flat edges on the clock signal lead to delayed data acquisition and must, therefore, be compensated for via the *Clock Skew* parameter in the *DiglConf* program.

### The goal is to measure the actual timing of the clock and data.

- Check the clock and the data with a two-channel oscilloscope. Measure at the transfer point: at the DUT for transmitter mode, at the breakout board for receiver mode.
- Use an oscilloscope with a bandwidth of at least 500 MHz. Ensure that the probes, too, offer sufficient bandwidth. Use 10:1 or 100:1 probes. These probes feature high-impedance and low capacitance; consequently, they influence the signal shape less than 1:1 probes do.

The probe itself changes the situation at the measurement point. This is partially due to its capacitance, and partially to the connection of a cable that feeds in reflections. The probe capacitance can also further reduce the quality of the signal edges, and connecting a cable can generate positive overshoot. You can estimate the extent of these influences by temporarily connecting a second probe and observing how the signal changes.

- Don't use the ground cable on the probe; instead, connect the ground on the test point with a small piece of wire directly to the probe's ground ring.
- Use the DiglConf program's test mode (see Chapter 7). In transmitter mode, the R&S EX-IQ-Box supplies continuous data streams. In receiver mode, you generate continuous signals with your DUT.
- Check the timing at high temperatures as well. Experience has shown that semiconductor chips have poorer reaction times when they heat up.

Fortunately, the requirements for applications using the R&S EX-IQ-Box are not particularly stringent. The setup and hold times in particular are short compared to the data transfer rate. The cable connections between the R&S EX-IQ-Box and the DUT are short. Cable attenuation is not relevant. Crosstalk can be ignored if you use all ground wires from the connectors X2 and X3 on the breakout board to the DUT, and connect them directly to ground on the DUT side.

Whereas the data lines are almost settled in time, the clock signal has to be checked carefully.

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Figure 65 and Figure 66 show the essential components for a data transmission path. A source (TX) that usually has a low impedance feeds a cable that typically has a characteristic impedance (Z) of 100 ohms. There is a receiver (RX) at the end of the cable.

There are significant differences between differential and single-ended data transmission.

### **Differential data transmission**

The data transmission uses two active cables.



Figure 65: Differential data transmission

In particular in the receiver IC, the cable is terminated with 100 ohms – the approximate characteristic wave impedance (Z). For this reason, there is no overshooting or signal collapsing.

Nevertheless, inspect the signals at the RX port in order to verify the theoretically calculated setup and hold times.

### Single-ended data transmission

The data transmission uses an active cable.



Figure 66: Single-ended data transmission

In this case, the components are not matched to each other. The receiver input usually has high-impedance; a small capacitive component is generally negligible compared to the cable capacitance. At the RX port, and impedance step occurs from the characteristic wave impedance (Z, approx. 100 ohms) to high-impedance.

For this reason, it is important to inspect the settling process especially of the clock signal. The high-impedance RX input generates an overshoot. This overshoot is reflected back over the cable to the transmitter. There, the impedance is low; a signal collapse arises that then returns to the receiver, and so on.

This "ringing," however, is highly attenuated by the cable's low-pass character, and it drops off after just a few nano seconds. The strength at which these effects arise also depends on the cable that you use.

For the data cables, these settling processes are generally insignificant. It must be ensured, however, that the clock signal has no uncertainty in the level range around the signal threshold.

If you observe distortion of the Clock signal near the threshold, terminate the cable at the transfer point with two 220 ohm resistors (see Figure 68).



Figure 67: Signal distortion near the threshold



Figure 68: Recommended line termination

Both resistors should be attached with very short connections and as close as possible to the RX chip. In transmitter mode, this point is on the DUT. In receiver mode, you have to terminate them at the breakout board.

If the Vcc arrives via a long path, add a capacitor of 470 pF to ground. In this way, with regard to high frequency, the two 220 ohm resistors are connected in parallel, and they terminate the cable properly; in each case, the TX output stage needs only drive 220 ohms.

In rare cases, data signal crosstalk can be observed on the clock cable. Here, too, termination in accordance with Figure 68 offers a reliable remedy.

Based on the actual measured relationship between the clock edges and data edges, optimize your settings for the Clock Skew in the DiglConf program.

### 11 The Breakout Boards

The breakout boards distribute the connections from the R&S EX-IQ-Box's user interface across two connectors. Additional pins supply Vcc potential and ground potential.

The R&S EX-IQ-Box's delivery package includes two breakout boards: one for singleended and one for differential data.

The setup and hold times for the inputs are the same for both boards:

Setup time: 0.6 ns Hold time: -0.2 ns

These values are for ideal signals with ideal signal edges. Since the connection cables flatten the signal edges (especially including those for the clock signal as well), it is a good idea to reserve several nanoseconds for the setup time.

### Single-ended breakout board

Two 50-position standard connectors are planned for connecting ribbon cables. (Manufacturer: Harting, part number: 0919 550 6323 ).



Figure 69: Single-ended breakout board

Table 11\_1 shows the pin assignments. For each logical channel, there is one active and one ground conductor.

Connections that are not needed in user-defined mode are grayed out.

All inputs feature high-impedance with a fringing capacitance of approximately 8 pF. The output power depends on the logic family:

CMOS12:	8 mA
CMOS15, CMOS18:	16 mA
CMOS25, CMOS33, LVTTL:	16 mA

Pinout X2	Pinout X2, X3 for the single-ended breakout board (3585.7280.00)					
Pin	Signal name	Direction	Description			
X2.1	UI_I_P0					
X2.3	UI_I_P1					
X2.5	UI_I_P2					
•		in / out	I-component (single ended)			
•						
	•					
X2.35	UI_I_P17					
X2.37	AUX_IO0	in / out	auxiliary signals			
X2.39	AUX_IO1					
X2.41	GP0					
X2.43	GP1	in / out	additional protocol-dependent control / signaling			
X2.45	GP2					
X2.47	D_CLK_UOUT_ P	out	internal data clock, when R&S EX-IQ-Box is set to Clock Internal			
			is set to Clock External			
X2.49	UI_VALID_P	out	data-valid signal (active, high) in TX mode			
		in	gate signal (active high) in RX mode pulled up by internal resistor			
X3.1	UI_Q_P0					
X3.3	UI_Q_P1					
X3.5	UI_Q_P2					
		in / out	Q-component (single ended)			
•						
•	•					
X3.35	UI_Q_P17					
X3.37	AUX_IO2	in / out	auxiliary signals			
X3.39	AUX_IO3					
X3.41	GP4	in / out	additional protocol-dependent control / signaling			
X3.43	GP5	in / out	marker, strobe			
X3.45	GP3	in / out	additional protocol-dependent control / signaling			
X3.47	D_CLK_UIN_P	in	external clock			
X3.49			not connected			
All even numbered pins	GND					

Table 11\_1: Pinout X2, X3 for the single-ended breakout board

Differential breakout board



The differential breakout board supplies the user-interface signals on two 100-pole SMD connectors. (Manufacturer: Samtec, part number: ASP-65067-01).

Figure 70: Differential breakout board

Table 11\_2 shows the pin assignments. For each logical channel, there are two active and two ground wires.

All inputs feature high-impedance with a fringing capacitance of approximately 8 pF. The power of the outputs is optimized for RX chips with an internal 100 ohm termination.

Pinout X2, X	Pinout X2, X3 for differential breakout board (3585.7296.00)					
Pin	Signal name	Directi on	Description			
X2.1, X2.2	GND					
X2.3 X2.4	UI_I_N0 UI_I_P0					
X2.5, X2.6	GND					
X2.7 X2.8	UI_I_N1 UI_I_P1					
X2.9, X2.10	GND					
X2.11 X2.71 X2.72	UI_I_N2 UI_I_N17 UI_I_P17	in / out	I-component (differential)			
X2.73, X2.74	GND					

Pinout X2, X3 for differential breakout board (3585.7296.00)					
Pin	Signal name	Directi on	Description		
X2.75	AUX_IO_N0	in / out	auxiliary signals		
X2.76	AUX_IO_P0	-			
X2.77, X2.78	GND				
X2.79	AUX_IO_N1	in / out	auxiliary signals		
X2.80	AUX_IO_P1				
X2.81, X2.82	GND				
X2.83	GP_N0	in / out	additional protocol-dependent control / signaling		
X2.84	GP_P0	-			
X2.85, X2.86	GND				
X2.87	GP_N2	in / out	additional protocol-dependent control / signaling		
X2.88	GP_P2	-			
X2.89, X2.90	GND				
X2.91 X2.92	GP_N1 GP_P1	in / out	additional protocol-dependent control / signaling		
X2 93 X2 94	GND	-			
X2.05, X2.04		out			
X2.96	D_CLK_UOUT_P	out	internal data clock, when R&S EX-IQ-Box is set to Clock Internal		
X2.97, X2.98	GND	-	buffered external clock, when R&S EX-IQ-Box is set to Clock External		
X2.99	UI_VALID_N	out	data-valid signal (active, high) in TX mode		
X2.100	UI_VALID_P	in	gate signal (active, high) in RX mode pulled up by internal resistor		
X3.1, X3.2	GND				
X3.3	UI_Q_N0				
X3.4	UI_Q_P0				
X3.5, X3.6	GND				
X3.7	UI_Q_N1				
X3.8	UI_Q_P1				
X3.9, X3.10	GND	in / out	Q-component (differential)		
X3.11	UI_Q_N2				
•					
·					
• X3.71	UI_Q_N17				
X3.72	UI_Q_P17				
X3.73, X3.74	GND	1			

Pinout X2, X3 for differential breakout board (3585.7296.00)						
Pin	Signal name	Directi on	Description			
X3.75 X3.76	AUX_IO_N2 AUX_IO_P2	in / out	auxiliary signals			
X3.77, X3.78	GND					
X3.79 X3.80	AUX_IO_N3 AUX_IO_P3	in / out	auxiliary signals			
X3.81, X3.82	GND					
X3.83 X3.84	GP_N4 GP_P4	in / out	additional protocol-dependent control / signaling			
X3.85, X3.86	GND					
X3.87 X3.88	GP_N3 GP_P3	in / out	additional protocol-dependent control / signaling			
X3.89, X3.90	GND					
X3.91 X3.92	GP_N5 GP_P5	in / out	marker, strobe			
X3.93, X3.94	GND					
X3.95 X3.96	D_CLK_UIN_N D_CLK_UIN_P	in	external clock			
X3.97, X3.98	GND					
X3.99, X3.100			Not connected			

 Table 11\_1: Pinout X2, X3 of differential breakout board

### 12 Summary

In order to ensure ideal coupling of Rohde & Schwarz test and measurement instruments via the R&S EX-IQ-Box with a device under test, this Application Note contains detailed recommendations on how to connect the hardware and configure the instruments.

The introductory functional and operational description explains how to operate the R&S EX-IQ-Box as a transmitter or receiver – in real time and in slow IQ mode. Then the document describes the applications in sections divided according to transmitter mode and receiver mode; in each case, this includes instructions for the generator, analyzer and radio communication tester. The focus is on the individual input parameters and the meaning of the interface signals.

Additional chapters cover the R&S EX-IQ-Box's test mode and the physical characteristics of the interface between the R&S EX-IQ-Box and the DUT.

1MA168 is designed to supplement the individual device manuals. The Application Note summarizes all important steps in a single document to get you started successfully.

### 13 Literature

- [1] <u>R&S EX-IQ-BOX, Operating Manual, Rohde&Schwarz, 2010</u>
- [2] R&S CMW500, Operating Manual Volume 1, Rohde&Schwarz, 2010
- [3] R&S CMW500, Operating Manual Volume 2, Rohde&Schwarz, 2009
- [4] R&S AMU100A, Operating Manual, Rohde&Schwarz, 2010
- [5] R&S SMU200A, Operating Manual, Rohde&Schwarz, 2010
- [6] R&S SMJ100A, Operating Manual, Rohde&Schwarz, 2010
- [7] R&S FSV, Operating Manual, Rohde&Schwarz, 2010
- [8] <u>R&S FSQ, Operating Manual, Rohde&Schwarz, 2009</u>
- [9] R&S FSG, Operating Manual, Rohde&Schwarz, 2009
- [10] <u>R&S FMU36, Operating Manual, Rohde&Schwarz, 2007</u>

### 14 Ordering Information

Ordering Information								
R&S EX-IQ-BOX								
R&S EX-IQ-BOX	Digital Interface Module	1409.5505K04						
Wideband Radio Commun	Wideband Radio Communication Tester							
R&S CMW500	Base Unit	1201.0002K50						
R&S CMW-B510	Digital IQ interface (inputs/outputs/monitor)	1202.8007.02						
Signal Generators								
R&S AMU200A	Baseband Signal Generator	1402.4090.02						
R&S AMU-B13	Baseband Main Module	1402.5500.02						
R&S AMU-B9	Baseband Generator (128 Ms)	1402.8809.02						
R&S AMU-B17	Baseband I/Q Input	1402.5900.02						
R&S AMU-B18	Baseband I/Q Output	1402.6006.02						
R&S SMU200A	Vector Signal Generator	1141.2005.02						
R&S SMU-B106	Frequency Option 6 GHz, 1 <sup>st</sup> RF path	1141.8803.02						
R&S SMU-B203	Frequency Option 3 GHz, 2 <sup>nd</sup> RF path	1141.9500.02						
R&S SMU-B13	Baseband Main Module	1141.8003.04						
R&S SMU-B9	Baseband Generator (128 Ms)	1161.0766.02						
R&S SMU-B17	Baseband I/Q Input	1142.2880.02						
R&S SMU-B18	Baseband I/Q Output	1159.6954.02						
R&S SMJ100A	Vector Signal Generator	1403.4507.02						
R&S SMJ-B106	Frequency Option 6 GHz, 1 <sup>st</sup> RF path	1403.8702.02						
R&S SMJ-B13	Baseband Main Module	1403.9109.02						
R&S SMJ-B9	Baseband Generator (128 Ms)	1404.1501.02						
R&S SMJ-B18	Baseband I/Q Output	1410.5705.02						

Ordering Information							
Signal Analyzers, Spectrum Analyzers							
R&S FSV	Up to 40 GHz	1307.9002.xx					
R&S FSV-B17 (not for R&S FSV40)	Digital Baseband Interface	1310.9568.02					
R&S FSQ	Up to 40 GHz	1155.5001.xx					
R&S FSQ-B17	Digital Baseband Interface	1163.0063.02					
R&S FSG	Up to 13.6 GHz	1309.0002.xx					
R&S FSQ-B17	Digital Baseband Interface	1163.0063.02					
R&S FMU36	Baseband Analyzer	1303.3500.02					

xx stands for the different frequency ranges (e.g. 1155.5001.26  $\,$  up to 26 GHz)

**Note:** Not all available options are listed. Please contact your local Rohde & Schwarz sales office for further assistance.

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- Continuous improvement in environmental sustainability
- ISO 14001-certified environmental management system



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