Application Note

DEEMBEDDING TEST FIXTURES FOR HIGH-SPEED DIGITAL APPLICATIONS

In high-speed digital measurement applications, test fixtures are commonly used to connect devices under test to measurement equipment. Characterization, and analysis in the time and frequency domains that accounts for various constraints helps to remove the influence of these fixtures.

Products:

- R&S®RTP
- R&S®RTO
- R&S®ZNB
- R&S®ZNA
- R&S®ZNPC

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https://www.rohde-schwarz.com/appnote/1SL393

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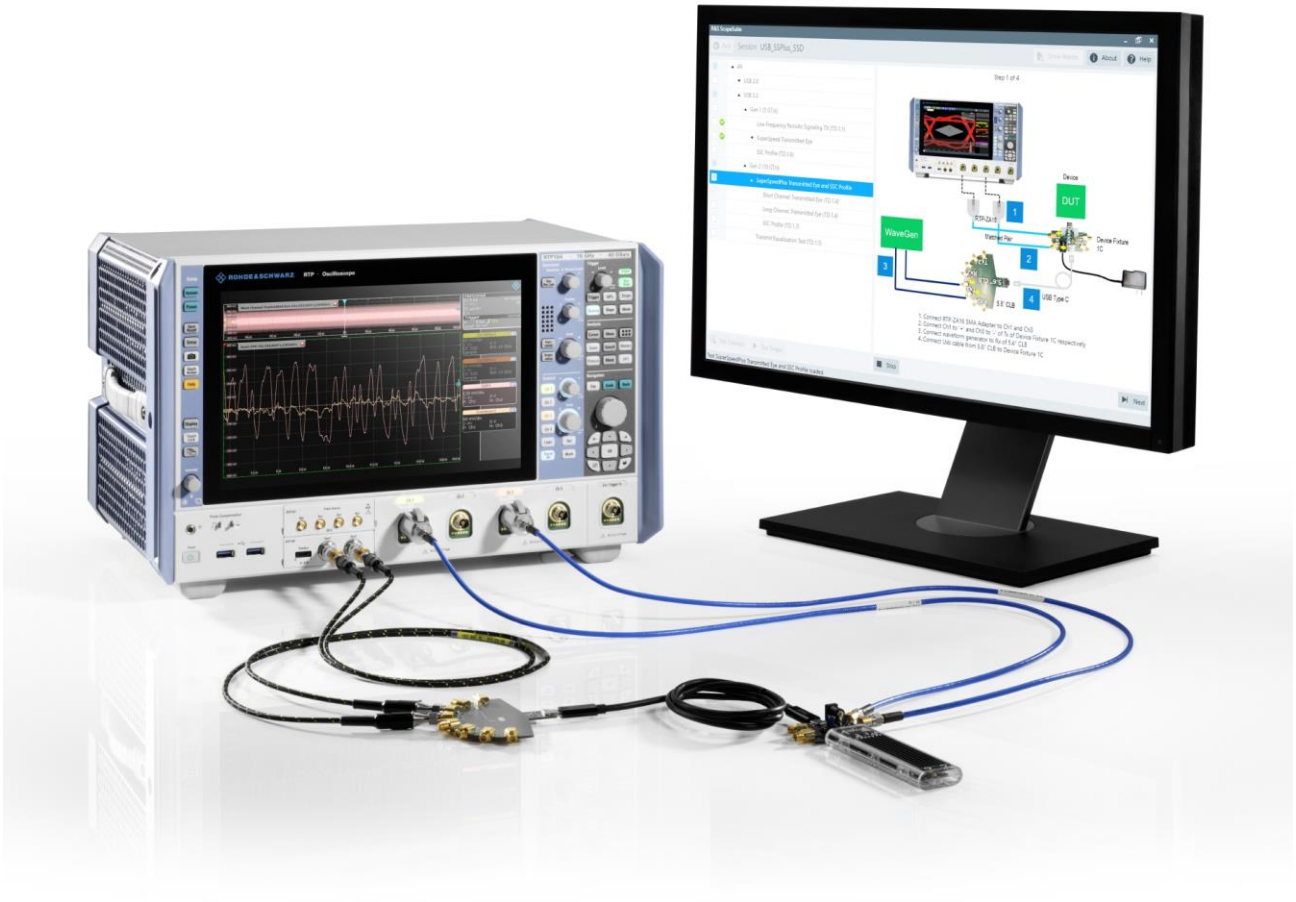
1 Overview

High-speed digital interfaces like USB, PCIe and HDMI are found on much of the commercial and industrial equipment available today. Such interfaces are used to transfer data both internally within the equipment and to other peripheral devices. With every new generation of digital system, these interfaces are pushed to increase the speed of data transfer and also reduce the form factor.

This presents a challenge for the measurement setup to reliably contact the interface and accurately acquire the signals for verification, debug and compliance testing. One solution is to use a test fixture to access the device under test (DUT) signals on the connector on one side and lead it to another connector on the other side – typically a coaxial connector.

At higher data rates, however, the influence of these fixtures cannot be neglected, particularly in debug measurements and sometimes also in compliance testing. To address this matter, this application note explains methods that can be used to characterize a test fixture, deembed the characterized model into the time domain measurements on an oscilloscope and show the effects on the signal integrity. The well-known USB Type-C® interface is used as an example. It has the advantage of offering two different data rates (Gen1: 5 Gbps, Gen2: 10 Gbps) providing more details in the analysis.



2 Deembedding Concepts

Test fixtures, probes or other structures are used to adapt the coaxial interface of the test setup to the device under test (DUT) when performing measurements of non-connectorized devices. To ensure accurate measurements of the DUT, these lead-ins and lead-outs need to be characterized, so that their effects can be mathematically subtracted, i.e. deembedded, from the measurement results.

This application note provides practical hints for accurately characterizing and deembedding these lead-in and lead-out structures with the R&S®ZNA, R&S®ZNB, R&S®ZNBT and R&S®ZND vector network analyzers. This application note also describes how the characterized lead-ins and lead-outs can be exported as an S-parameter file for use with other test instruments like oscilloscopes. Various S-parameter models are generated and compared.

For most electrical high-speed digital applications, differential signaling is the method of choice, and this will be the focus in this application note.

As mentioned before, the DUT chosen for this analysis is the USB3.2 Type-C device test fixture (see Figure 1). Even though the USB interface is commercially available and widely used, it does not come with S-parameter data. The USB3.2 Gen 1 operates at 5 Gbps and the USB3.2 Gen 2 operates at 10 Gbps. This makes it well suited for detailed analysis because the occupied bandwidth changes from one mode to the other, allowing for a comprehensive comparison. The results of this analysis can be easily transferred to other technologies.

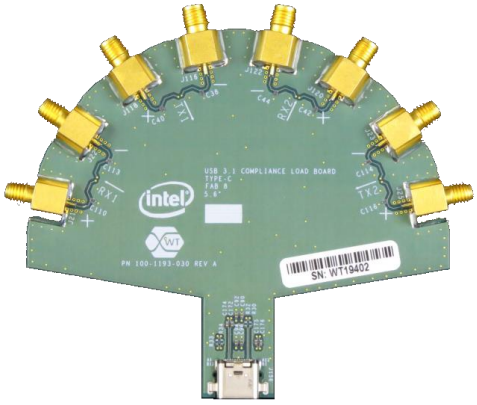
USB 3.1 TPAC DEVICE 1C plug	USB 3.1 TPAC CLB 5.6 receptacle
	
Left side	Right side

Figure 1 USB 3.2 device fixture and CLB fixture

2.1 Motivation for deembedding

To understand the motivation for deembedding it is helpful to differentiate between an interface defined by an industry standard, like USB, and a proprietary interface used solely for a certain application. For the latter, deembedding is essential to enable accurate measurements for characterization.

For standard interfaces, the compliance parameters that have to be met may be established based on a well-defined and typically mandatory test fixture. In this case deembedding is not necessary. If the compliance test fails in its assessment of the true device data (voltage, current, timing) of the DUT, deembedding is again necessary.

2.2 Time domain vs. frequency domain

Depending on the interface, parameters that have to be met are specified in either the time or the frequency domain. For example, rise and fall time, jitter and overshoot preemphasis/postemphasis are specified in the time-domain. Other parameters like data rate, spread spectrum clocking (SSC) or return loss are specified in the frequency domain.

Several techniques are available to characterize the test fixture, but the most promising method is analysis in the frequency domain using a vector network analyzer (VNA). It has a large dynamic range, and the excitation is kept constant over the entire sweep range, as opposed to TDR measurement with an oscilloscope when the spectral content of the excitation has a steep roll off with $1/f$ at higher frequencies in combination with the lesser input sensitivity of the oscilloscope acquiring the TDR signals.

2.3 Consistency tests

Once the characterization is accomplished and data in the form of S-parameters can be loaded into the oscilloscope for deembedding, the instrument will display traces without the effects of the test fixture. But a question remains of how accurate the displayed data will be. How much will accuracy depend on the modeled S-parameter data, rather on the oscilloscope's accuracy? A consistency check is a helpful way to judge the model accuracy independently of the oscilloscope.

The IEEE370 [1] provides guidance on evaluating model data with respect to the expected results. There are two normative tests labeled 1 and 2, and two informative tests labeled 3 and 4.

- **Consistency test #1**: (normative) Self deembedding of 2X-Thru
- **Consistency test #2**: (normative) Compare the TDR of the fixture model to the FIX-DUT-FIX
- **Consistency test #3**: (informative) Compare a DUT-DUT measurement with two concatenated DUT models
- **Consistency test #4**: (informative) Consistency tests based on verification structures

Because this standard was developed for RF applications, it is not entirely suitable for fixtures designed for high-speed digital signals. One key reason for this is that a high-speed digital element behaves differently than an amplifier, making a test like #3 impossible. Also, there is not necessarily a 2xthru (see the next subchapter Setup constraints), which implies that test #1 is not feasible.

The most practical consistency check is test #2, which gives a good indication of the accuracy of the model. It is based on the S-parameter transformed into a time domain reflectometry (TDR).

Test #1 is not possible under all circumstances. The reason for this is that self deembedding requires S-parameter models for both test coupons (left & right) in Figure 4. So, either the right coupon of the deembedding structure is not available at all or, as is the case with USB3.2 Type C, the right coupon is the CLB with a long trace (5.6”, 7.1”, 8.1”), which shows a significantly higher insertion loss. This then degrades the consistency check for the “better” left side model.

Table 1 below shows fixture performance characteristics according to IEEE Std 370. The derived models for the high-speed digital fixtures are typically in the class C limit.

	Class A limit	Class B limit	Class C limit
Insertion loss of 2x-Thru in [dB]	–10	–15	–15
Return loss of 2x-Thru in [dB]	–20	–10	-6
Insertion loss minus return loss of 2x-Thru in [dB]	5	0	0
'Fixture - DUT - Fixture' crosstalk minus 'Fixture - Fixture' crosstalk (using dogleg / spiderleg structure) in [dB]	6	6	6
Impedance variation between 2x-Thru coupon and actual lead-ins / lead-outs in %	+/–2.5	+/–5	+/–10
Line to line or pair to pair skew between lead-ins / lead-outs / 2x-Thru halves	1 / (10 x fmax) for 50 GHz: 2 ps	1 / (10 x fmax) for 50 GHz: 2 ps	1 / (10 x fmax) for 50 GHz: 2 ps
Min length of 2x-Thru [wavelengths at highest frequency]	3	3	3
Additional requirement for mixed mode deembedding: Differential to common mode conversion loss minus insertion loss) in [dB]	–15	–15	–15

Table 1 - Fixture electrical requirements (FER) according to IEEE Std 370

Although not covered in the standard, another method to ensure a good model and test consistency is to deembed the left coupon for the open and short measurements. This is referred to in this application note as **Consistency test #5.** The impedance over time in a TDR plot based on the return loss (S_{DD11}) is displayed for open and short. Then, the left side coupon is deembedded. In this case, the criteria for a good fixture model is a deviation of impedance from the nominal one (t<0s). This defined setup works with just one coupon.

2.4 Redefining the 2xthru

IEEE370 defines the 2xthru as a symmetrical pair of coupons with coaxial connectors on both ends for the measurement device, but no high-speed connector in-between, see top drawing below. This structure is

supposed to have the same line impedance, delay and loss as the test fixture. The reference plane is at one-half of the delay of the 2xthru standard and each half of the 2xthru is symmetric.

This has limited applicability for a high-speed digital test fixture for several reasons.

First, most of the DUTs do not have two ports, and even if they have two, like a USB hub, these are not transparent with analog means; rather, they have digital processing inside.

Second, ignoring the connector in the model excludes the dominant part of the transfer function. Vendors have several versions of these high-speed connectors. They can be vertically or horizontally oriented; they can have a through hole or SMD connectors to the board with different pin-outs; and last but not least, the pin escape of the PCB might vary a lot and be subjected to several design constraints. The result could be that that the characterization of the DUT is done with one specific connector, but in use the DUT will use a quite different one.

Third, due to the high-speed connector structure, the 2xthru will never be symmetric.

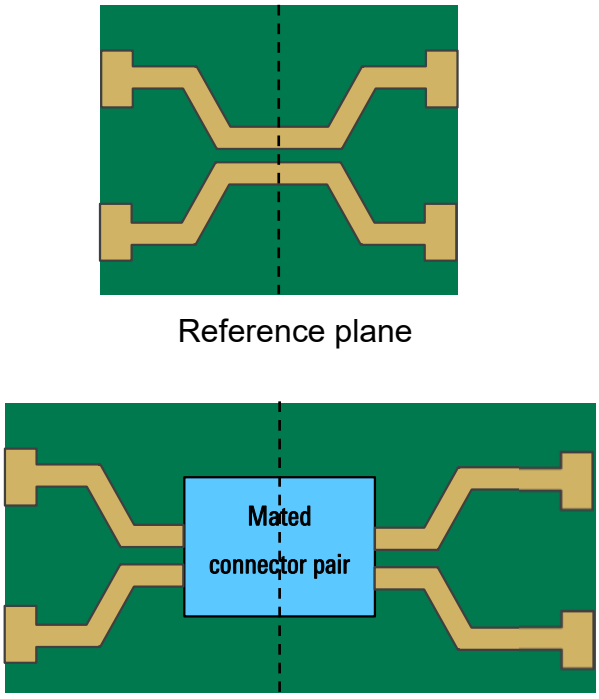


Figure 2 2xthru definition

So, the suggestion is to redefine the 2xthru in such a way that the high-speed connector is included in the structure and that the open measurement determines the electrical length. The short measurement will improve this determination. This way the fixture high-speed connector is taken out of the analysis with the oscilloscope and the DUT characterization becomes independent of the fixture.

2.5 Setup constraints

The main constraint is the fact that none of these high-speed digital interfaces supports suitable RF connectors, as these are coaxial, wave guide or probe tips. A typical test fixture has a coaxial interface on one side and the high-speed digital connector on the other side. Examples are USB, PCIe or HDMI. This makes it impossible to connect the test fixture directly to a VNA and move the reference plane of the VNA measurement to the high-speed connector using typical VNA calibration algorithms, where high-precision coaxial calibration standards are the most common way to perform a calibration. With these calibration standards, the reference plane is at the end of the coaxial connectors where the calibration standards are presented. If the reference plane needs to be shifted, deembedding can be used. For more information about this approach, please refer to the application note “Accurate Test Fixture Characterization and Deembedding” [2].

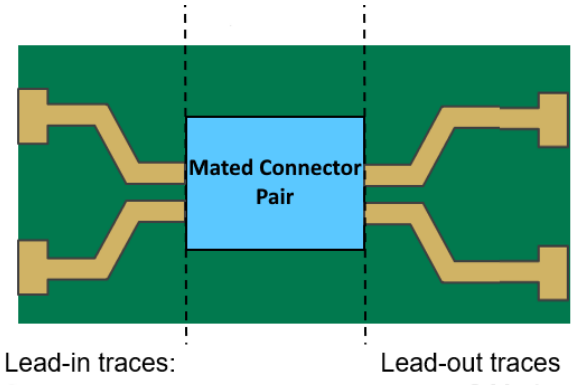


Figure 3 Mated connector pair with left and right coupons

A typical workaround for the missing coaxial connector is to design a counterpart fixture with the mate connector. These connectors come with a paired plug and receptacle, and both fixtures plugged together with coaxial connectors can be characterized with a VNA. The idea is to split the measured S-parameters S_m into two identical parts with S-parameters S_c, which satisfy the equation below.

$$[S_m] = [S_c] \cdot [S_c]$$

This means that the matrix product (catenation) of the calculated fixture S-parameters S_c equals the measured S-parameters S_m. This is mathematically possible and correct, but the pair of mated connectors is not symmetrical at all with the consequence that the calculated S-parameters S_c do not represent the S-parameter model of the single-side fixture.

Another constraint is the fact that depending on the standard, only one selected connector pair is used for characterization. For instance, for USB3.2 Type C, all cables will have only plugs, whereas hosts and devices will generally use the receptacle.

The in-situ deembedding option for R&S vector network analyzers, will be discussed in the next section as a solution for this dilemma. In some setups, in-situ deembedding depends on a single port return loss measurement of the fixture left open. In this case, the tool that generates the fixture model expects a reasonable, but not necessarily perfect, termination – not just an open or a short. Several constraints exist in this situation: one is that a DUT with a high-speed digital interface typically has a dynamic termination and must be powered in order to apply the nominal termination impedance. A second constraint in this regard is the fact that a termination might only be applied after a specific link initialization. In the example of the USB3.2 the transmitter is terminated once it is powered up, but the receiver is in a state called Rx.Detect, and it expects an Rx.Detect sequence, before it applies termination (see [3] Chapter 6.11). Other standards have similar mechanisms for link initialization. A VNA cannot issue the Rx.Detect sequence. To switch the DUT into the Rx.Detect sequence, additional SW or HW tools are needed.

3 VNA measurements

The goal of VNA measurements is to provide all inputs for the tool to create the S-parameters of the test fixture. The tool of choice for this application note is the ISD tool [4] integrated into the graphical user interface of the R&S®ZNB20. The reason for choosing this tool is that its impedance correction [5] seems to be more advanced than that of other tools.

The stimulus for the frequency domain has to be set to satisfy two requirements. It should have a harmonic grid and at least 8 points per wavelength. In a harmonic grid, the start frequency is equal to or a multiple of the step size and consequently, the stop frequency is a multiple of the step size. The second requirement is that the TDR calculation of the VNA have an unambiguous range. The VNA measures in the frequency domain, and the TDR is an analysis in the time domain. The TDR can be calculated based on the inverse, discrete Fourier transform of the measured data. For the (inverse) Fourier transform, the relation below gives the time step size t_s, and the time window t_w based on the stop frequency f_{max}, the frequency step size f_s and the number of frequency samples N:

$$t_s = \frac{1}{2 \cdot f_{max}} \wedge t_w = \frac{1}{f_s} = \frac{N}{f_{max}}$$

When the displayed time in the TDR exceeds the time window t_w, the TDR becomes ambiguous due to the discrete Fourier transform. To avoid this situation, the necessary sample points, which cover at least the delay of the fixture, can be calculated with a typical delay of 4 ns up to a stop frequency of 20 GHz. This yields a minimum number of points of 80 (= 4 ns * 20 GHz).

In the above setup, all measurements were carried out as 4-port S-parameter measurements to enable analysis as balanced or differential S-parameters. For the step size, it is assumed that any resonance in the measured structure will have a q-factor larger than 1 MHz, which means that no resonance will go undetected.

The following stimuli parameters were used in order to satisfy the above requirements:

Start frequency	0.001 GHz
Stop frequency	20.00 GHz
Frequency step size	0.001 GHz
Bandwidth	10 kHz
Power level	–10 dBm

Table 2 VNA setup parameters

3.1 Measurement setup for the VNA

Regular measurements to characterize a test fixture according to the IEE370 are already described in an application note [2]. At this point, the focus shifts to the characterization of test fixtures with a high-speed

connector. In this case, the measurement setup for the VNA consists of four setups. Whether all measurements are necessary will be discussed in Chapter 3.2.

One specific setup is the USB short, which is not commercially available. It consists of metal with geometry corresponding to the USB 3.0 type C plug (see Figure 5). It is not necessarily required by the standard [6], but it improves the characterization. The index of the measurement is shown in Table 3.

1. Open connector: two of the VNA ports are connected to the left or right fixture in a differential manner, and the USB connector is open – left in the case of the plug and right in the case of the receptacle
2. Shorted connector: two of the VNA ports are connected to the left or right fixture in a differential manner, and the USB connector is shorted – left in the case of the plug and right in the case of the receptacle (see Figure 5).
3. 2xthru with a mated connector: two of the VNA ports are connected to the left fixture in a differential manner and a further two to the right test fixture in the same manner. Both are connected to each other as a mated pair.
4. DUT terminated: two of the VNA ports, are connected to the left fixture in a differential manner and; in this case, the plug – connected to a DUT

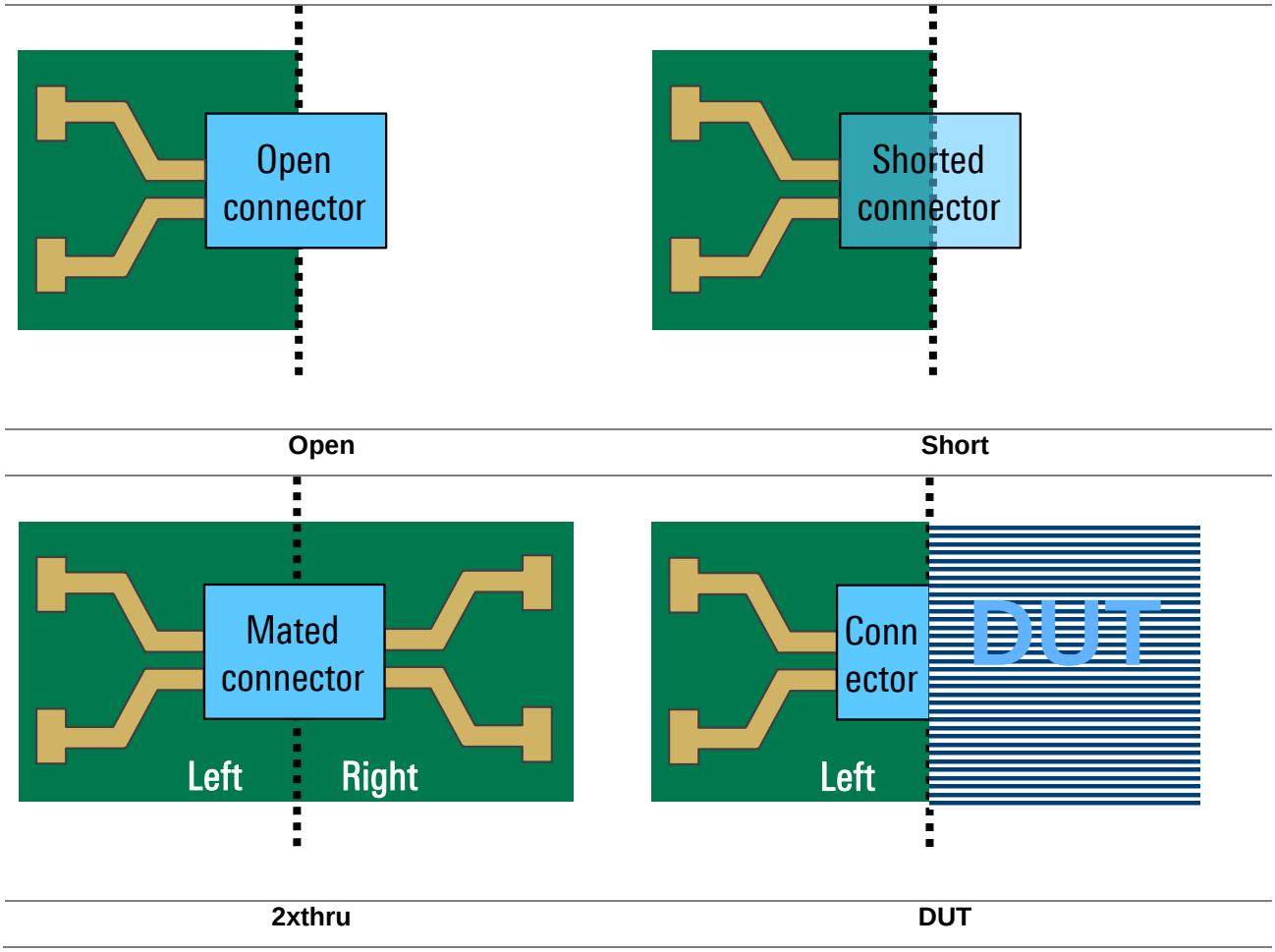


Figure 4 VNA measurements

It is important to note that the USB short used is not a commercially available part, but rather an engineering sample, which was kindly provided by the connector vendor Würth Elektronik eiSos GmbH & Co. KG. It is a piece of metal with the outline of a regular USB Type C plug. The receptacle has several GND leads and this creates a sufficiently accurate short at the correct contact point.

Considering other Interface standards like PCIe card edge connectors or USB 3.2 Type A, the reader should be encouraged to design a short for engineering purposes.

Figure 5 USB type C connector short

The setup for the VNA measurements deployed a 4-port VNA (ZNB20) with the following connection: Port 1 -> TX1+(left-side), Port 3 -> TX1-(left-side), Port 2 -> TX1+(right-side), Port 4 -> TX1-(right-side)

Figure 6 VNA measurement setup

3.2 Model generation

These measurements are not all necessary for the model generation, but they allow an interesting combination for different needs. The following table provides on overview of the configuration and associated constraints. The measurements, labeled with 1through 4 were described on page 10.

Configuration	Measurement				Pros	Cons
	1(O)	2(S)	3(2)	4(D)		
sym-2xthru			✓		Simple setup, only one measurement required	Wrong model (see chapter 3.3.2 and 4.4)
open-2xthru	✓		✓		No short required	Lower accuracy Requires two fixtures (left, right)
open-short-2xthru	✓	✓	✓		High accuracy Allows model generation for left and right side No power supply or start-up pattern required	Requires two fixtures (left, right) and a short
open-DUT	✓			✓	No short required Allows model generation with only one fixture	Lower accuracy May require special start-up for RX
open-short-DUT	✓	✓		✓	High accuracy Allows model generation with only one fixture	DUT sends out data on TX May require special start-up pattern for RX Requires a short

Table 3 Model configurations with pros and cons

One drawback of the configuration without a short is reported lower accuracy in the time domain, which results in limited bandwidth in the frequency domain. So, the question remains, what is the bandwidth bound? Based on the documentation the lower limit of the bound is the cross-over point, where the magnitude of the return loss (S_{DD11}) becomes larger than the magnitude of the insertion loss (S_{DD21}).

Figure 7 shows the measurement of the 2xthru with a marker set to this point (**M1** 8.564 GHz @ –12.4dB). This is the lowest limit but a better judgement is possible with the TDR plot and the deviation using the left side model to deembed the open and short, referred to here as Consistency Check #5. The results will be discussed in Chapter 3.3.3, but for now it is important to understand that there is an iterative process for finding a good tradeoff between the permissible bandwidth of the model set in the “Advanced Settings” menu tool and the deviation in the deembedding, for example TDR analysis. It turns out that for all models, the full bandwidth of the VNA can be used.

Figure 7 return loss (blue) and insertion loss (red) of balanced S-parameters of the 2xthru measurement. (2 GHz/div)

For reference the symmetrical 2xthru model (sym-2xthru) will also be generated to show the deficiencies in the measurement results, and encourage the reader not to use this approach.

The R&S high-end vector network analyzers (VNA) –in this case the R&S®ZNB20 –have a tool that can create the S-parameter model for a single side (left or right) based on the measurements performed. The starting point of this tool is the “Offset Embed” menu. The ZNB20 offers several deembedding tools but the one of interest in this context is the ISD tool, which can be selected via the “Fixture Tool”. Once this is selected the “Deembed Assistant” will open the menu as displayed in Figure 8.

It should be noted that the following menus are created for typical VNA deembedding applications, where the DUT is not a high-speed digital device as in this document, but any kind of RF component.

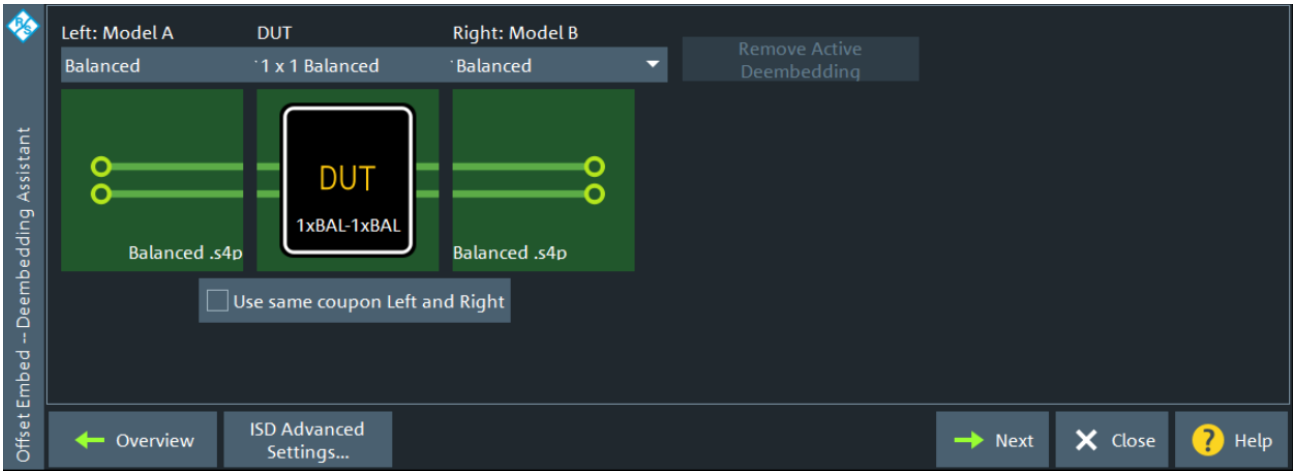


Figure 8 “Deembedding Assistant” menu setup for the 2xthru case

As a first step the ISD settings are configured by selecting the “ISD Advanced Settings” menu. Figure 9. In this menu (Figure 6) the “Port Sequence” is set to “Odd on left”, the “DUT Type” is set to “Active”, “DC Extrapolation” is checked, and the user has the option to limit the bandwidth to a lower value for “Max Freq to Deembed” than the maximum VNA bandwidth (20 GHz) as discussed in one of the previous sections. All other settings are defaults as seen in Figure 9.

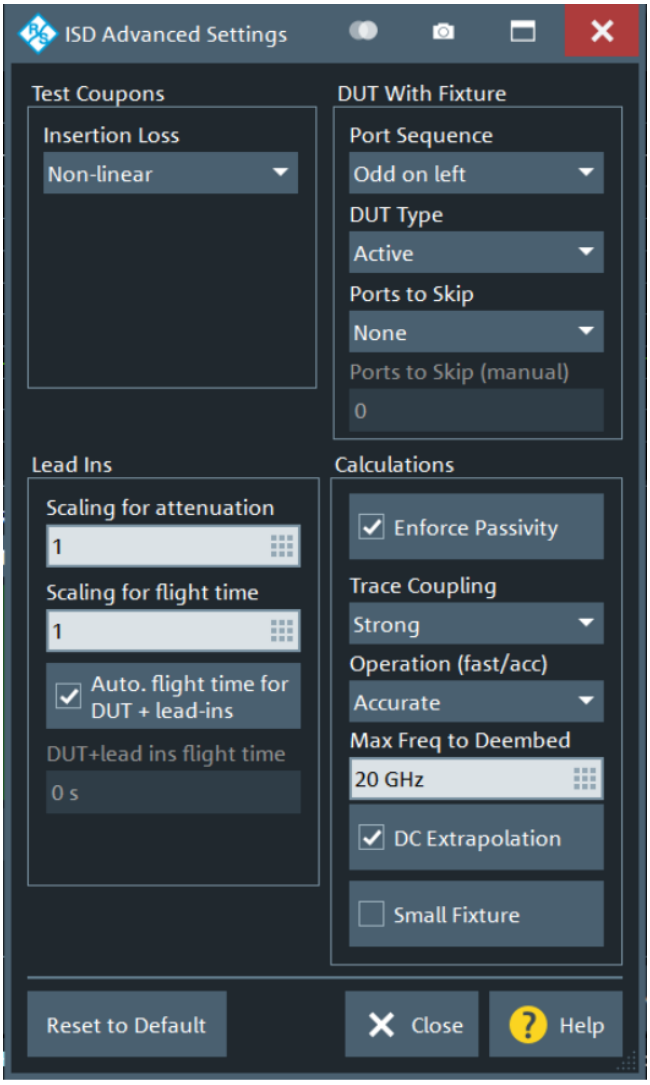


Figure 9 “ISD Advanced Settings” menu

After closing the “ISD Advanced Settings” menu, configuration is completed in the “Deembedding Assistant” menu (see Figure 8).

Figure 10 “Deembedding Assistant” menu setup for the DUT case

► For the left-side fixture model, select *"*Balanced" because the test fixture has a differential trace.

► For the DUT and the right-side fixture, the setting depends on the configuration, either DUT or 2xthru

– For the DUT case, the model is set *to "*1 x Balanced" and the right-side model is automatically set to *"*None" (see Figure 10)

– For the 2xthru case the DUT is considered as an ideal thru and the model is set *to "*1 x 1 Balanced". Additionally, it is necessary to uncheck *"*Use same coupon Left and Right", because this is not the case as discussed before (see Figure 8). The DUT displayed in the graphical user interface for the 2xthru case is just the identity, meaning the ideal short with $|H(\omega)| = 1 \wedge \measuredangle H(\omega) = 0$.

► The 2xthru case is the only one for which the right-side model is set to *"*Balanced"

► For the sym-2xthru case, *"*Use same coupon Left and Right" should be unchecked; the left and right models should both be "Balanced".

Once this step is configured, select *"*Next" to bring-up the next menu, where the measurement is taken. To create multiple models for comparison reasons, it is helpful to perform the individual measurements (open, short, thru, DUT – left, right), store the results as an .s2p or .s4p file and use the *"*Load" option to load the measurement. Otherwise, set up the circuit and press *"*Measure" to take the measurement. This needs to be done two or three times, depending on the setup. The GUI guides the user through the steps.

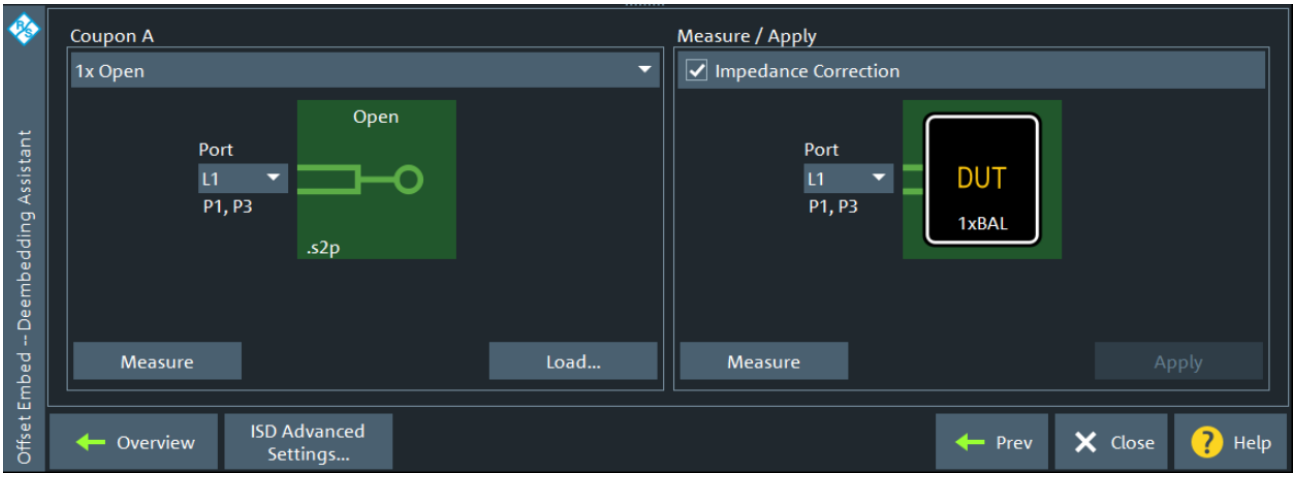


Figure 11 "Deembedding Assistant" menu setup **open-DUT** case

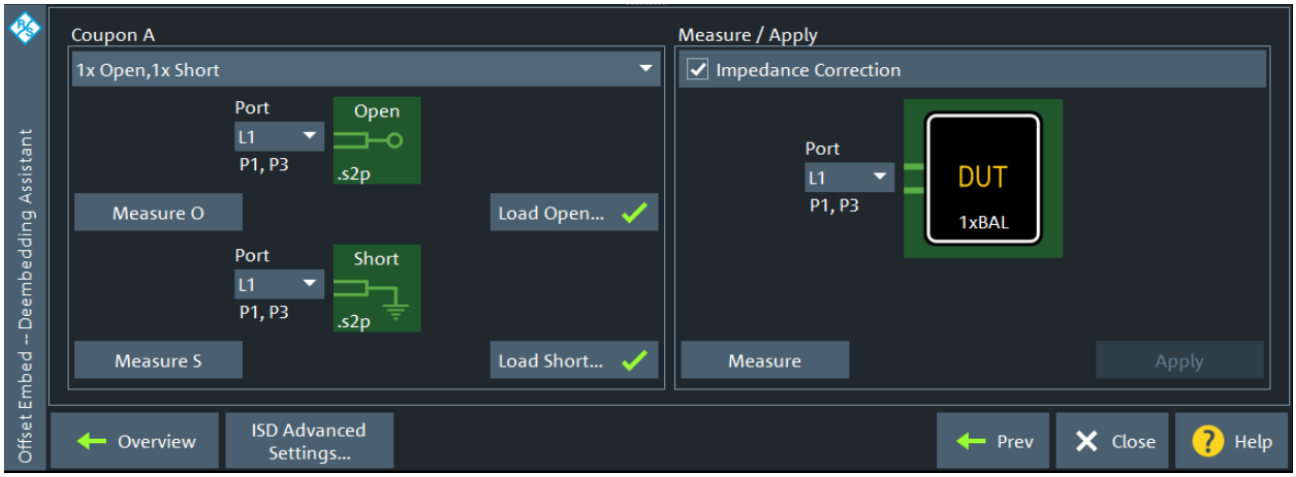


Figure 12 “Deembedding Assistant” menu setup **open-short-DUT** case

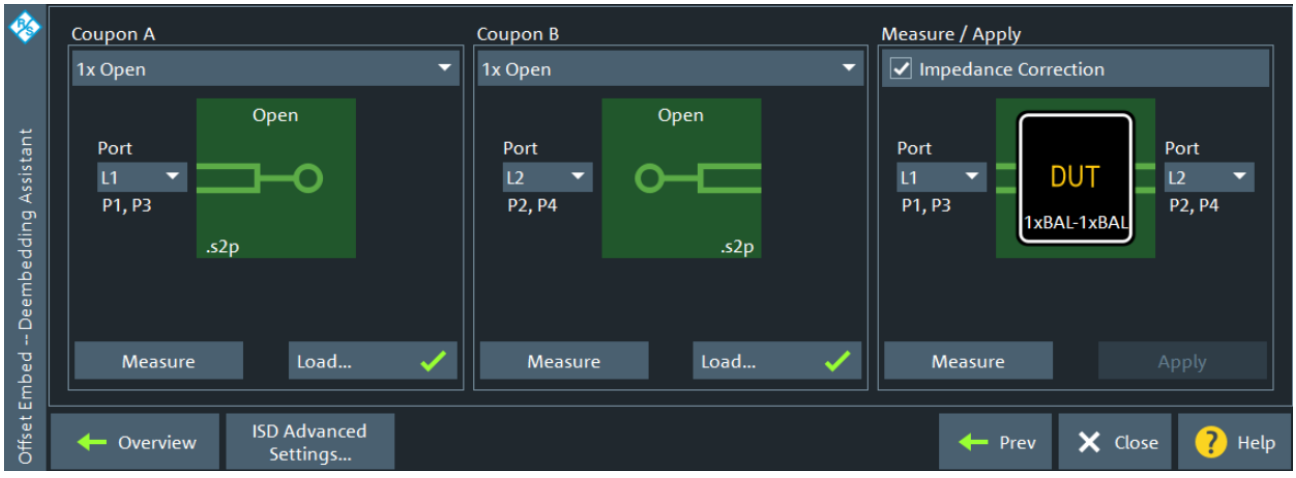


Figure 13 “Deembedding Assistant” menu setup **open-2xthru** case

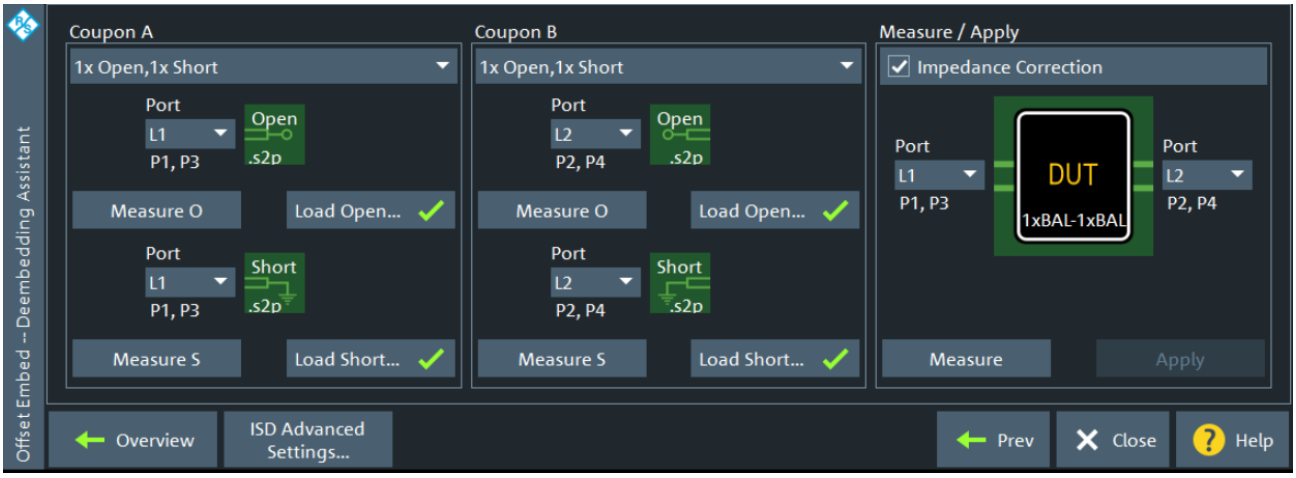


Figure 14 “Deembedding Assistant” menu setup **open-short-2xthru** case

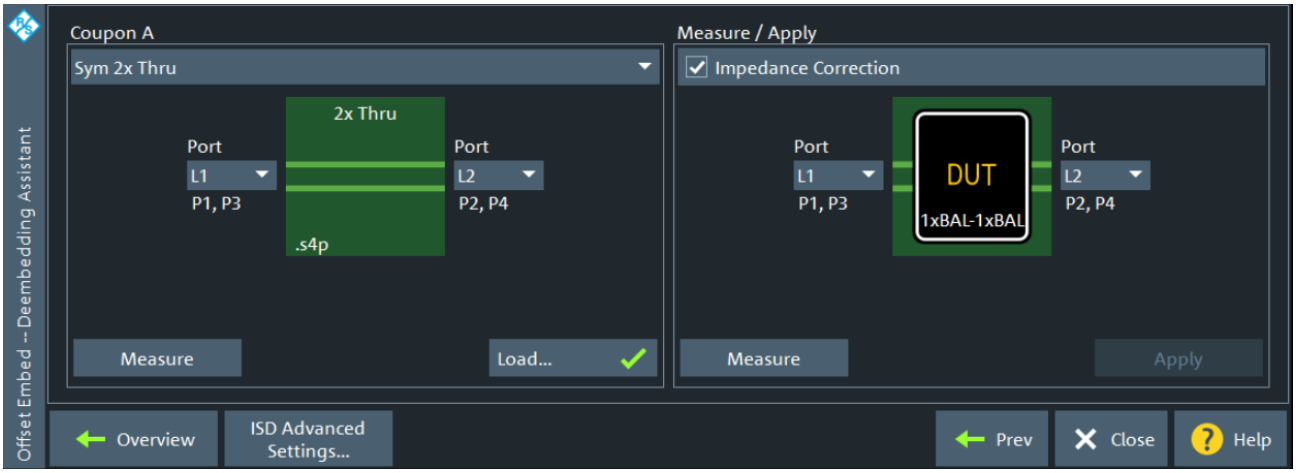


Figure 15 “Deembedding Assistant” menu setup **sym-2xthru** case

Once this is complete, press “Apply” to start the tool and load the newly created model as a deembedded file (see Figure 16) into the VNA “Deembedding” menu. After that, the effect of deembedding these files can be seen on the screen in the displayed results

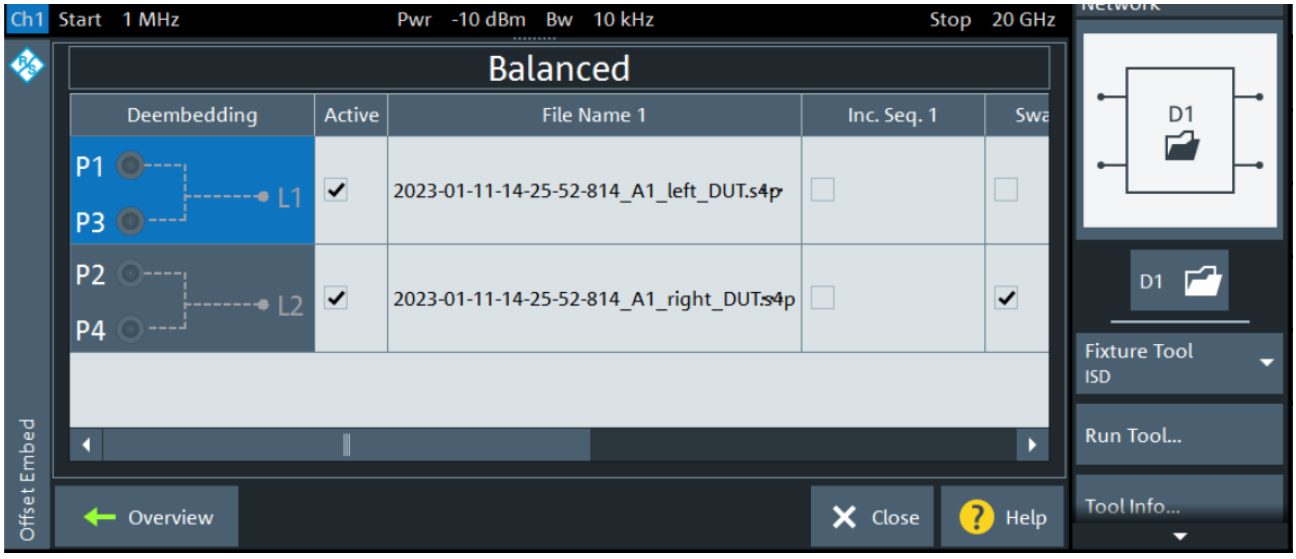


Figure 16 deembedding of the generated model

3.3 VNA measurement results

A VNA simulation is beneficial because it enables a comparison of all the measurement results. For the purposes of this application note, the comparison is done with the R&S®ZNPC. This is a regular PC with a licensed version of the ZNB20 FW is installed on it, making it an R&S®ZNPC.

The VNA results are examined in a sequence of analysis steps starting with the simple setup of sym-2xthru, continuing with open-DUT, open-short-DUT and switching to open-2xthru and open-short-2xthru.

3.3.1 TDR analysis of measurements

The next step is to display all measured traces in a TDR plot (see Figure 17). The left side corresponds to the S_{DD11} and the right side to the S_{DD22}. The plot shows that the short has a sharper roll off than the open, which implies that the electrical length is more precisely defined. Using the M1 marker (in blue) for the left-side and the M2 marker (in red) for the right-side, the electrical length can be read out. The right-side (2.09 ns) appears to be 5 times longer than the left-side (0.47 ns). These markers are helpful, and will be used in a subsequent step.

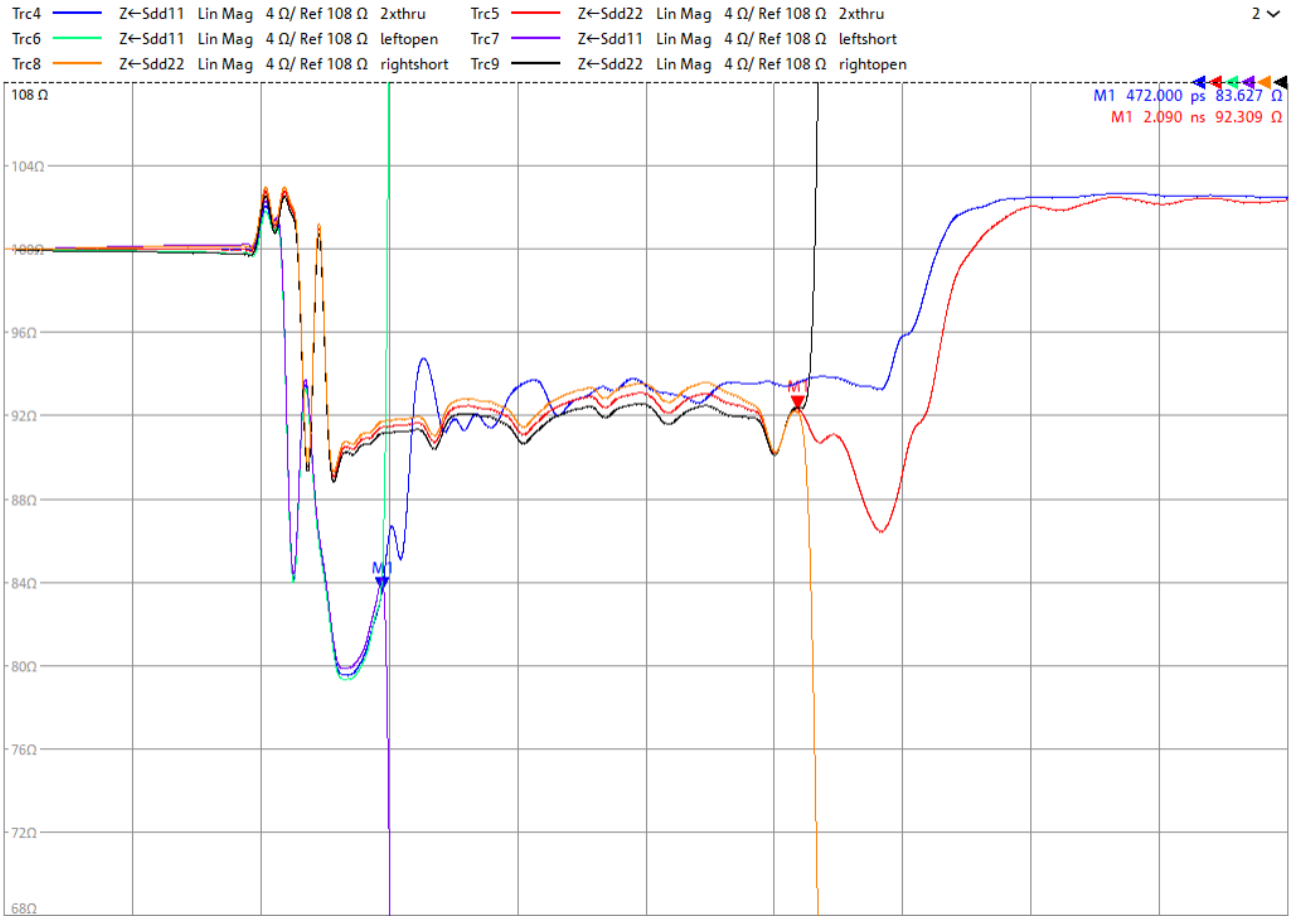


Figure 17 TDR plots of the measured traces

3.3.2 TDR analysis of models

The next step is to compare all of the generated models for the left side with the original 2xthru measurement (see Figure 18). The return loss (S_{DD11}) is plotted as a TDR and the M1 marker from the previous slide was preserved to show the electrical length. The original measurement is shown as trace 10 and serves as a reference for the generated models. The expectation is that the TDR (S_{DD11}) of the generated models would closely follow the original measurement up to the M1 marker, which is essentially consistency test #2.

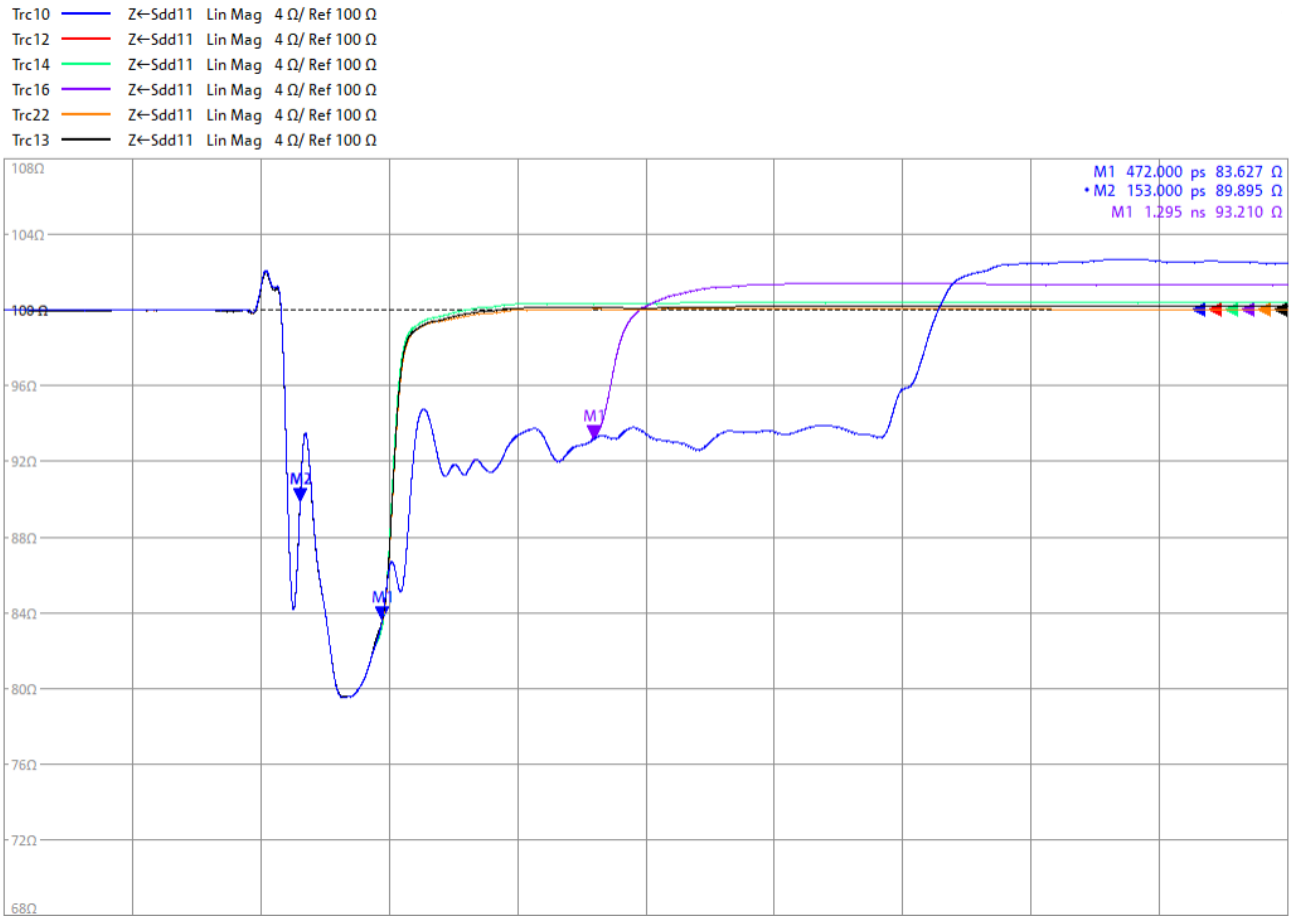


Figure 18 TDR plot comparing the left-side models

Going through the list of models, the first is the symmetrical 2xthru (sym-2xthru), displayed as trace 16 (Trc16). It is obvious that it splits the two fixtures, the left-side and the right-side, in the middle of the electrical length and it is far from the true connector location. The difference between the markers (Trc10 and Trc16) is 820 ps, which shows that the symmetrical split is not the best approach under all circumstances.

The remaining traces show that the results for the open-DUT model (Trc12), open-short-DUT model (Trc13), the open-2xthru model (Trc22) and the open-short-2xthru model (Trc14) coincide very well with the original trace.

It is worth mentioning that the bandwidth limit is 20 GHz and, although this consistency test is necessary, it is insufficient for assessing the quality of the model because all of the models defined up to 20 GHz follow the original waveform closely.

For the right-side models, there are fewer options because the DUT measurement was not possible with the given DUT; only the result of 2xthru measurement is available. All of the models generated for the right side are compared with the original 2xthru measurement (see Figure 19). The return loss (S_{DD22}) is plotted as the TDR and the rest is comparable to the Figure 17.

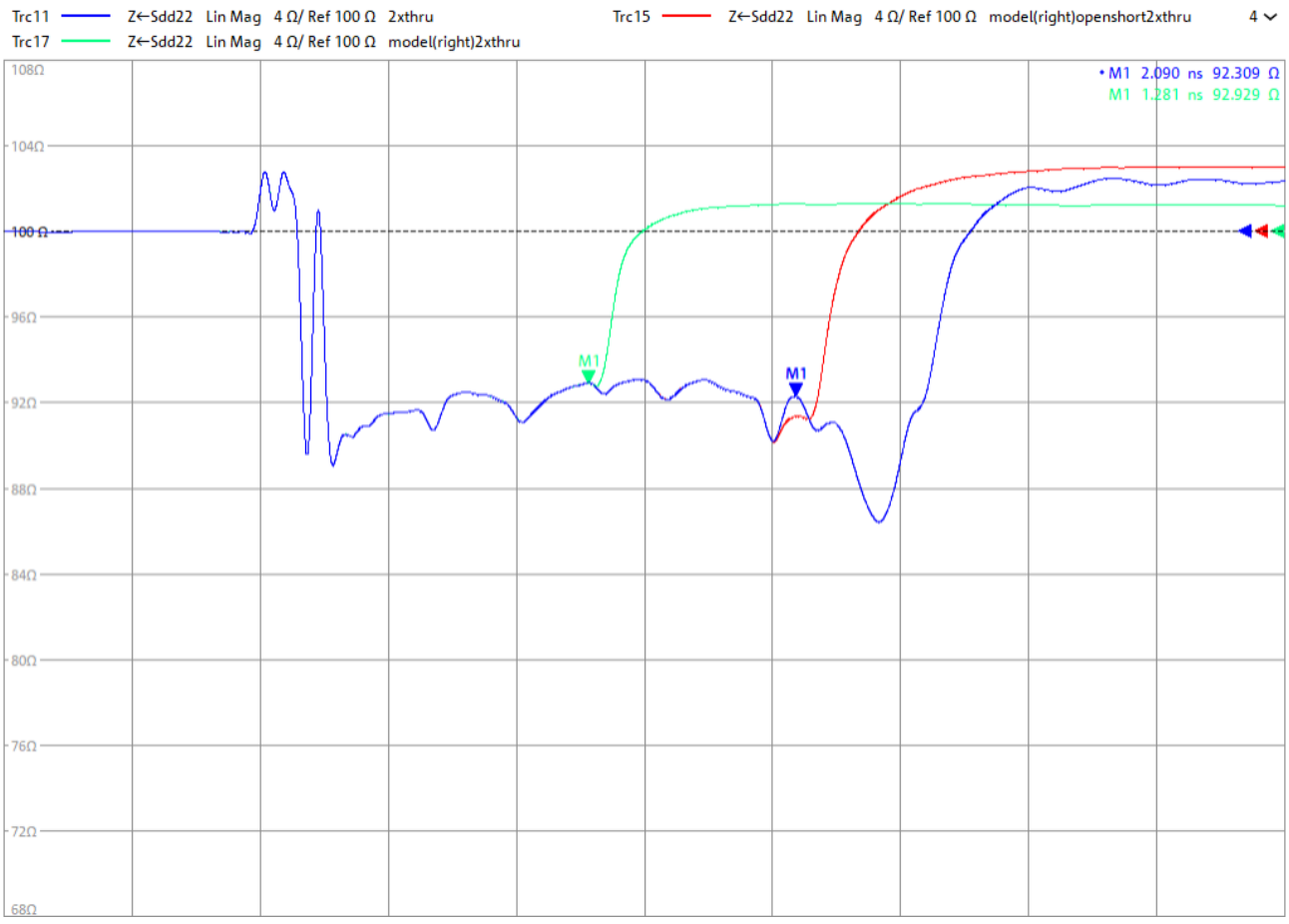


Figure 19 TDR plot comparing the right-side models

Like the previous model, the sym-2xthru model shows an incorrect electrical length, and the difference between Trc17 (M1) and Trc11 (M1) is 0.81 ns.

The open-short-2xthru model (Trc15) coincides well with the measured trace, except where it deviates at the M1 marker (Trc11). This occurs for two reasons: first, the short for the plug is not as good as the short for the receptacle, and second, the right-side fixture (CLB) has significantly longer, meandered traces with higher insertion loss.

3.3.3 TDR analysis of measurements with embedded models

The final analysis performed on the VNA is consistency check #5, described above. As explained above, the IEEE370 bases consistency checks on the left and right fixtures. In the following examples, only the left side is used for the quality assessment, though one of the models was generated based on the 2xthru.

As quality indicator, a limit line was set for the open and short traces with the respective deembedded model. The limit was set to 1.5% accuracy vertically for the resulting trace impedance. The horizontal limit was set close to the electrical length of the fixture.

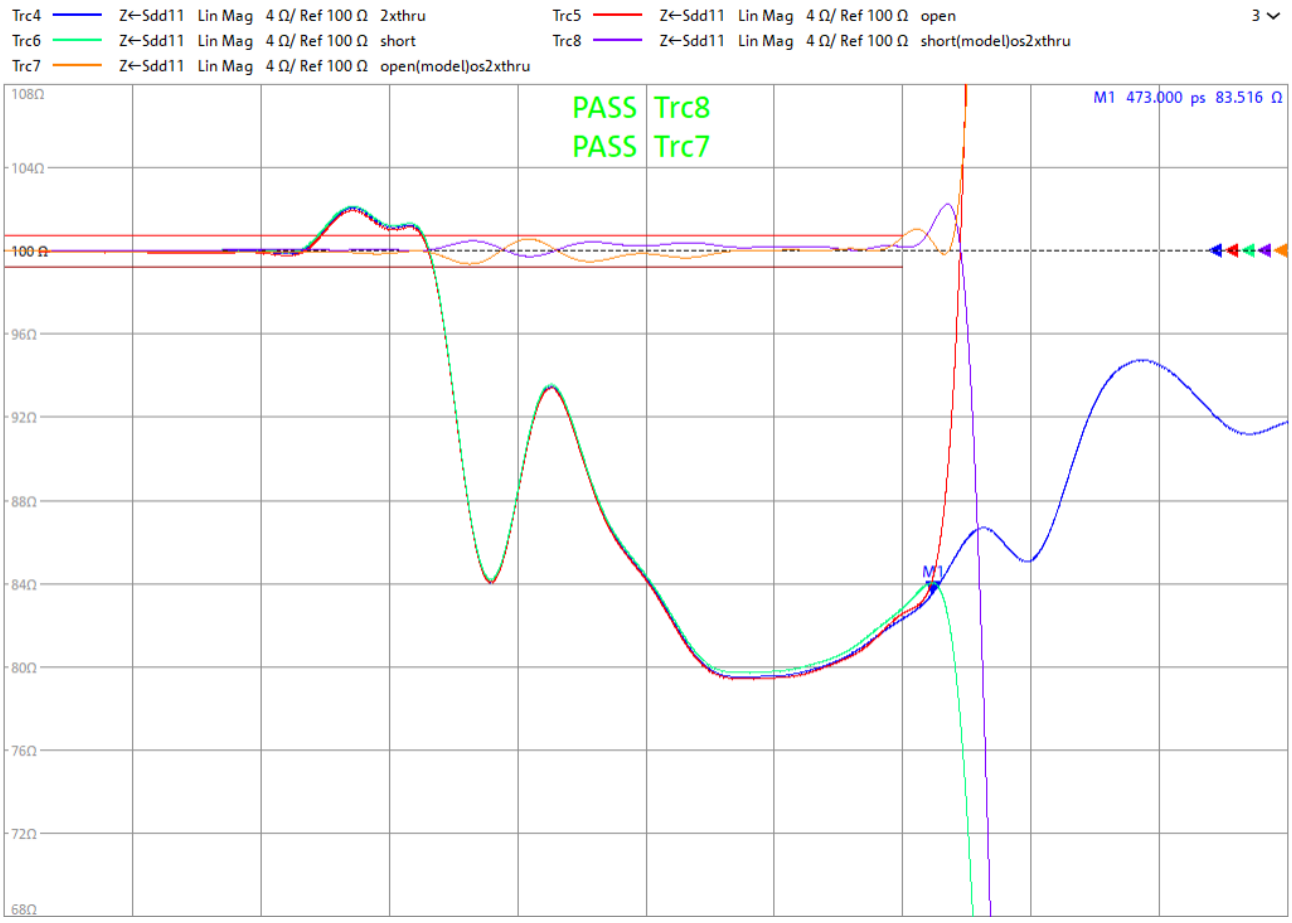


Figure 20 TDR plot comparing the deembedding of the open-short-2xthru left-side model (100 ps/div)

Figure 20 shows the TDR analysis. Based on the measurements, the TDR analysis for 2xthru, open and short is displayed as Trc4, Trc5, Trc6, respectively. Two new traces (Trc7, Trc8) are added based on the open and short measurements, which are embedded using the open-short-2xthru model. Deembedding shifts the reference plane to the connection point inside the connector, and traces appear as shifted in time. This is corrected in the diagram for comparison reasons, the shift in time is essentially the fixture delay indicated by the M1 marker (0.473 ps). The deviation of the deembedded traces from the reference impedance of 100 Ω is less than ±0.75%.

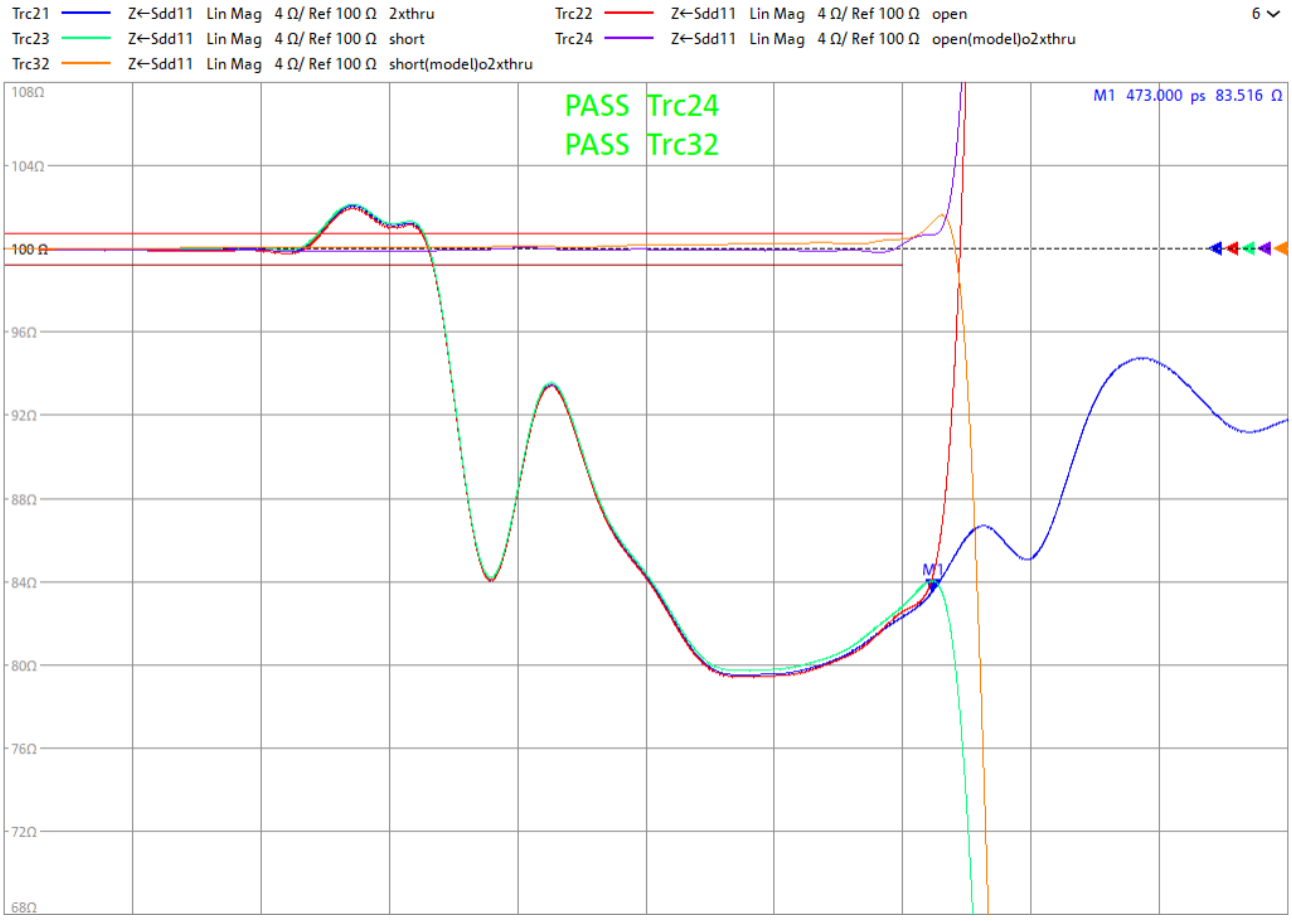


Figure 21 TDR plot comparing the deembedding of the open-2xthru left-side model (100 ps/div)

Figure 21 Shows the same setup with the deembedding of the open-2xthru model. The limits are maintained, but the traces deviate a bit more at the end of the fixture.

The next analysis is essentially the same configuration, but the model used for the deembedding is changed from the open-short-2xthru to the open-short-DUT. This model is dependent on *only one* left-side fixture – both in generation and quality evaluation. The 2xthru plot is for reference only but not required.

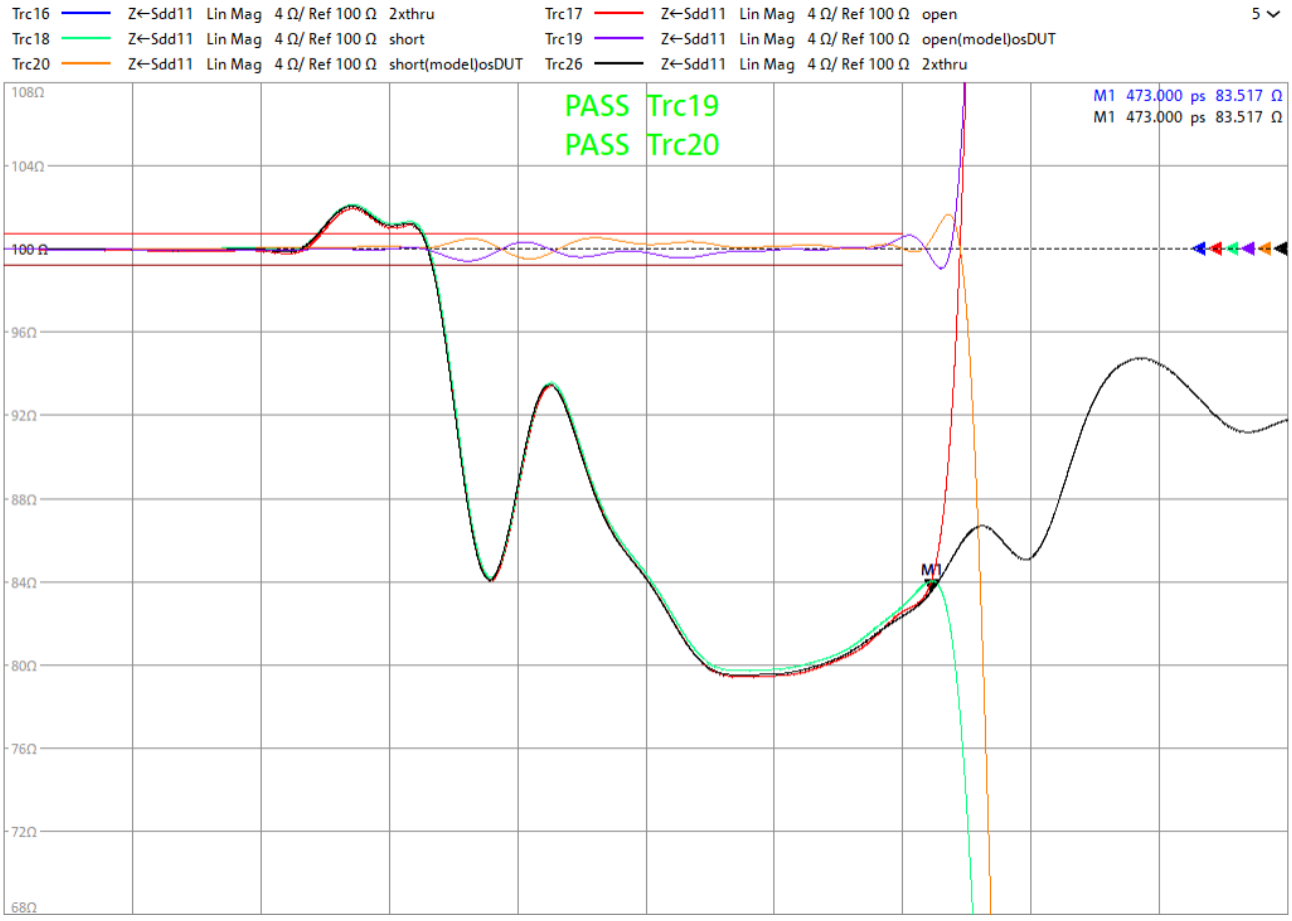


Figure 22 TDR plot comparing the deembedding of the open-short-DUT left-side model (100 ps/div)

Like the previous example, the deviation of the deembedded traces from the reference impedance of 100 Ω is less than 1%.

The last example (Figure 23) is again the same setup but with the open-short-DUT model.

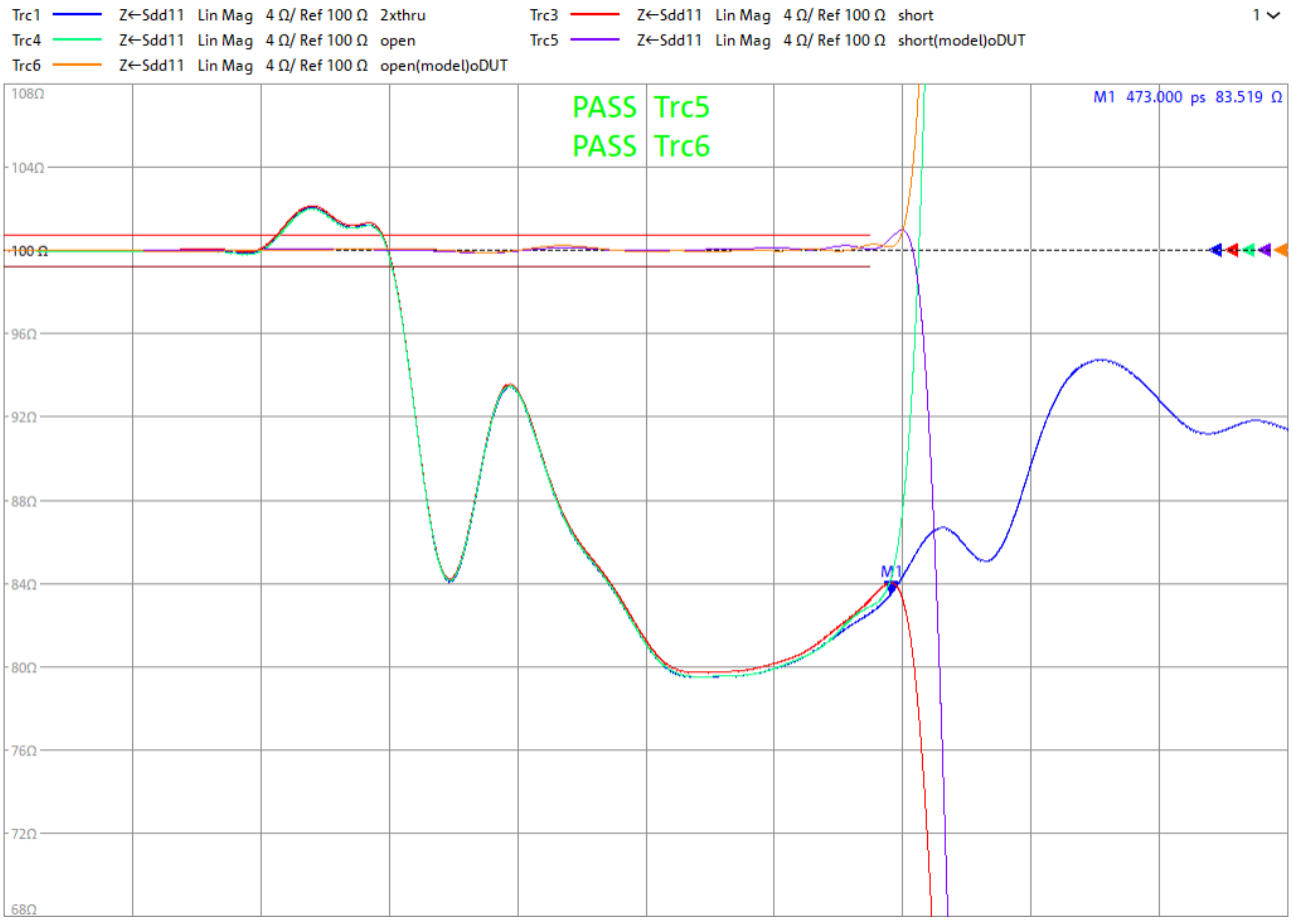


Figure 23 TDR plot comparing the deembedding of the open-DUT left-side model (100 ps/div)

3.3.4 Model Properties

The properties of all of the left-side models are displayed in Figure 24. Displayed are the magnitude of the insertion loss (S_{DD21}) (Trc{3*n+1} blue), the phase (Trc{3*n+2} red) and the delay (Trc{3*n} green) over frequency. The delay is the derivative of the phase to the frequency, and is part of the VNA measurements.

This analysis is also part of oscilloscope deembedding, and comparing both gives an indication as to whether something might go in the wrong direction or if the port assignment is correctly applied for the imported file.

In order to display the phase and delay in a meaningful way, the phase is unwrapped and both are delay compensated, so only the deviation from the linear phase and the propagation delay is displayed. This can be easily achieved by using the “Offset Embed” > “Auto Length” function. The linear delay for all models is 260.1 ps with a standard deviation of 1.4 ps.

Figure 24 The left column shows the models generated with the short measurement, and the right column shows the models without the short measurements. The top row uses the 2xthru measurement, whereas the bottom row uses the DUT measurement.

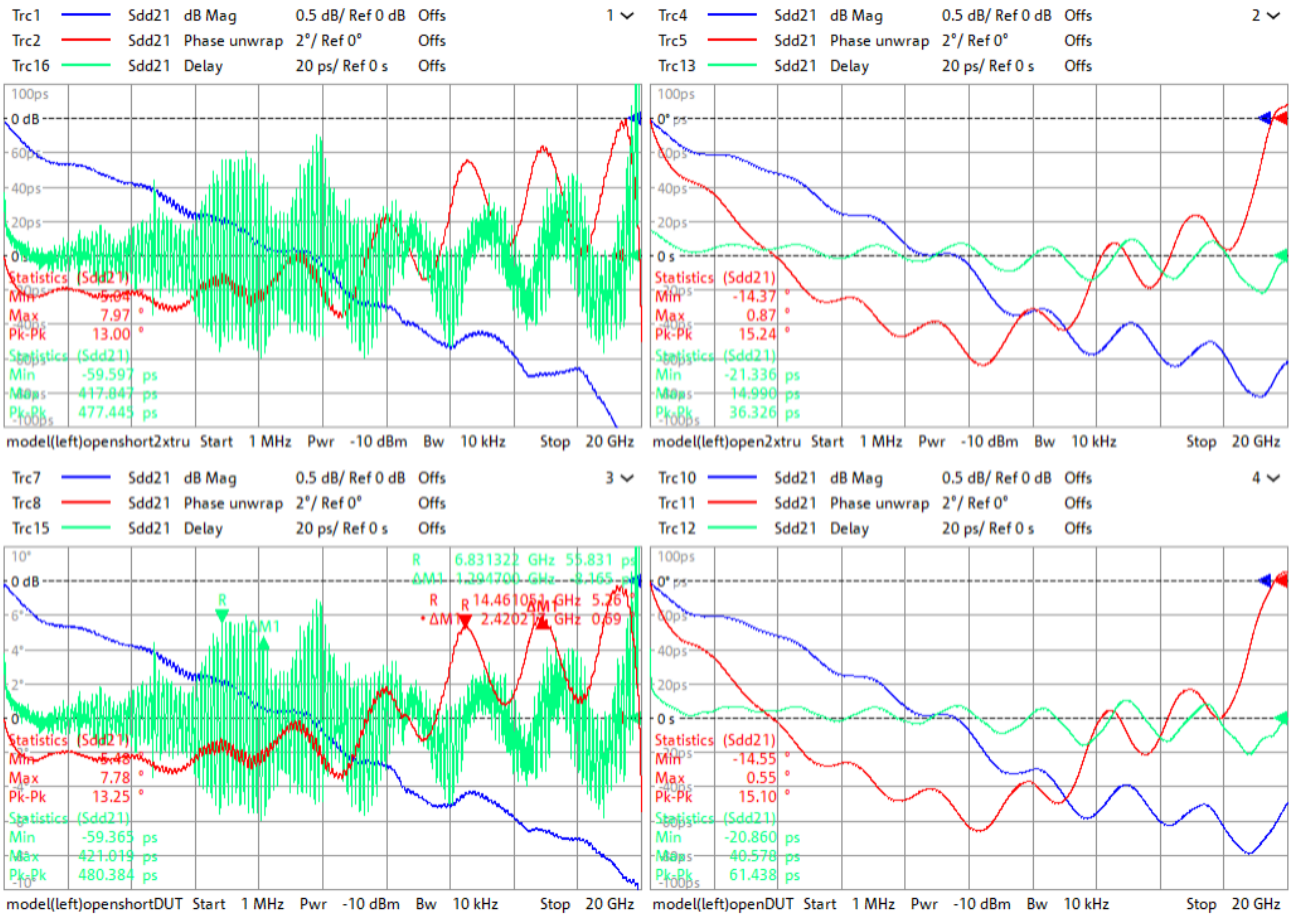


Figure 24 comparison of all model properties (2 GHz/div)

Comparing all generated models for the left-side, a few things seem to be apparent:

- The ripple on the delay measurement for the models created with a short. The phase vs. frequency plots share the same behavior.
- The phase variation of these measurements shows a smaller deviation from the linear phase, for measurements with a short compared to the measurement without a short.
- The magnitude shows a pretty linear trend, for the models created with a short

These ripples are measured with a delta marker (green) over 10 periods in the chart bottom left. The frequency is 129 MHz, which corresponds to a delay of 7.75 ns. The next chapter will look deeper into this behavior.

A second ripple is also measured with a delta marker (red) and the result is 2.42 GHz. Calculating the length of the underlying structure yields a length of ~ 30 mm. This is roughly the length of the test fixture, so it can be identified as multiple reflections between the SMA and the USB type-C connector of the fixture.

3.3.5 Model Adjustment

To find the root cause of the 129 MHz resonance, which indicates a signal shifted in time around 7.75 ns, the open-short-DUT model is further investigated. First the TDR (S_{DD11}) is analyzed in the range of [-8 to 2] ns (Figure 29) clearly shows a reflection of the TDR signal around -7.2 ns, indicated by the M1 marker.

Though the magnitude is very small (0.5 Ω), it means that the generated model behaves non-causally and that an output is issued before the input, which is impossible. One reason for this behavior is the non-infinite matching of the VNA input, which cannot be entirely removed by calibration. Other reasons are cable flexure, connector repeatability and of course calibration drift. It should be noted that the instrument has very good source matching (43 dB), comparable to other instruments on the market but technical constraints limit the ability to significantly improve this figure.

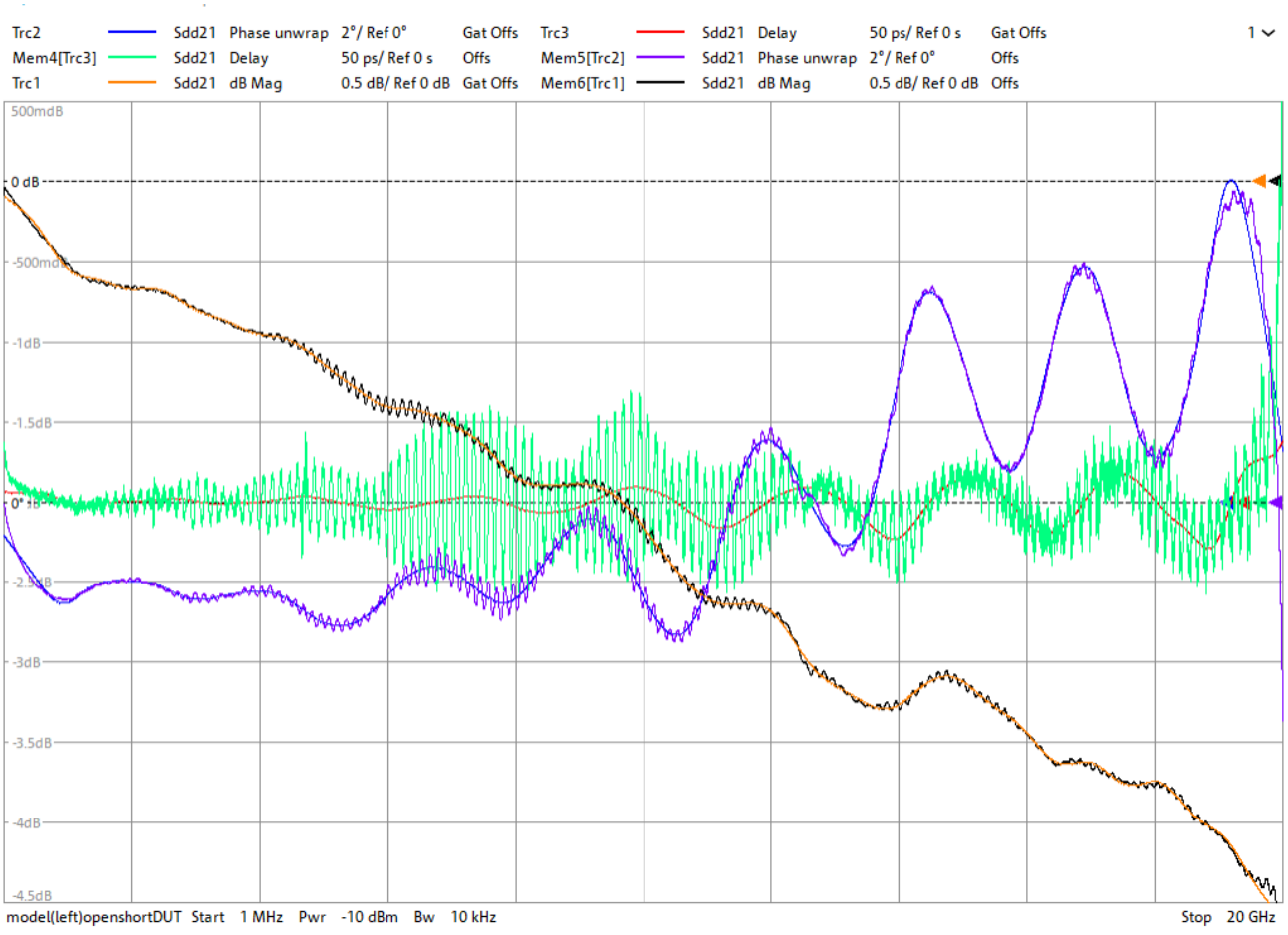


Figure 25 comparison of open-short-DUT model – original vs. time gated

This behavior in Figure 29 looks noncausal, and a quick sanity check confirms that this is the case (see Figure 25). To demonstrate this, the original data is stored as a memory trace (Mem4, Mem5, Mem6) and compared with the time gated traces (Trc1, Trc2, Trc3). The gate was set to [–1 - 1] ns. Comparing the corresponding trace magnitude, phase and delay it is obvious that the ringing is gone, though the gated traces show deviation from the original traces for low and high frequencies (0 and 20 GHz).

To mitigate this, two separate adjustments to the model can be carried out. The first is a correction based on the time gating of the TDR only, the second is a causal enforcement of the model. The explanation of these adjustments is beyond the scope of this app note. This model can be tested for causality based on the Kramer-Kronig relation [7] for causal systems, which relate the real and imaginary parts of transfer functions via the Hilbert transform [8].

$$H(\omega) = \frac{1}{\sqrt{2\pi}} \cdot \int_{-\infty}^{\infty} h(t) \cdot e^{-j\omega t} \cdot dt \wedge h(t<0) = 0 \Rightarrow \begin{cases} Re\{H(\omega)\} = \frac{2}{\pi} \cdot \int_{0}^{\infty} \frac{\omega' \cdot Im\{H(\omega')\}}{(\omega^2 - \omega'^2)} \cdot d\omega' \\ Im\{H(\omega)\} = -\frac{2}{\pi} \cdot \int_{0}^{\infty} \frac{\omega \cdot Re\{H(\omega')\}}{(\omega^2 - \omega'^2)} \cdot d\omega' \end{cases}$$

In the following four figures, four models are compared:

- The original open-short-DUT model labeled with *"no correction*"
- The TDR time gated model based on the original open-short-DUT model labeled with *"TDR gated"*
- The causality corrected model based on the original open-short-DUT model labeled with *"causality corrected"*
- The original open-DUT model labeled with *"without short"* for the purpose of comparison

Figure 26 shows the magnitude vs. frequency of the S_{DD21}. The original model (Trc1) shows the ringing with the measured 130 MHz frequency. The simple TDR gated trace (Trc2) is without ringing and looks fine so far. The trace of the causality corrected model (Trc9) is nearly coincident. Both show good coincidence at low and high frequencies (0 and 20 GHz). Only the model without short (Trc15) shows deviations at lower frequencies (< 5GHz), which is expected, and a ringing towards higher frequencies.

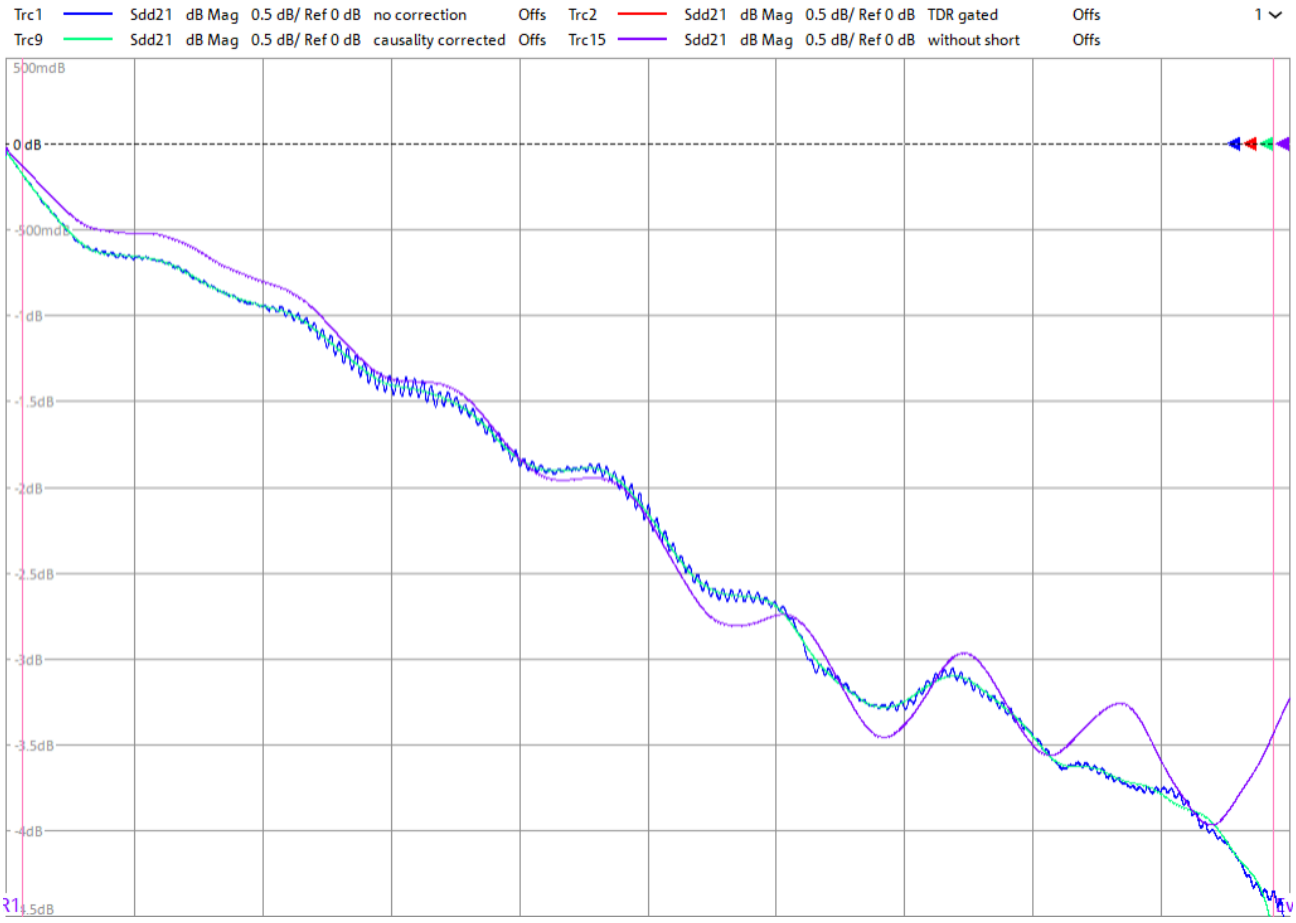


Figure 26 magnitude comparison of the adjusted models

Figure 27 compares the phase vs. frequency of the models. As already demonstrated, the original model (Trc4) shows ringing, but unlike the magnitude plot, the TDR gated model (Trc5) also shows ringing in phase. The causality corrected model (Trc10) has no ringing and also shows less deviation from the linear phase, unlike the model without short (Trc16).

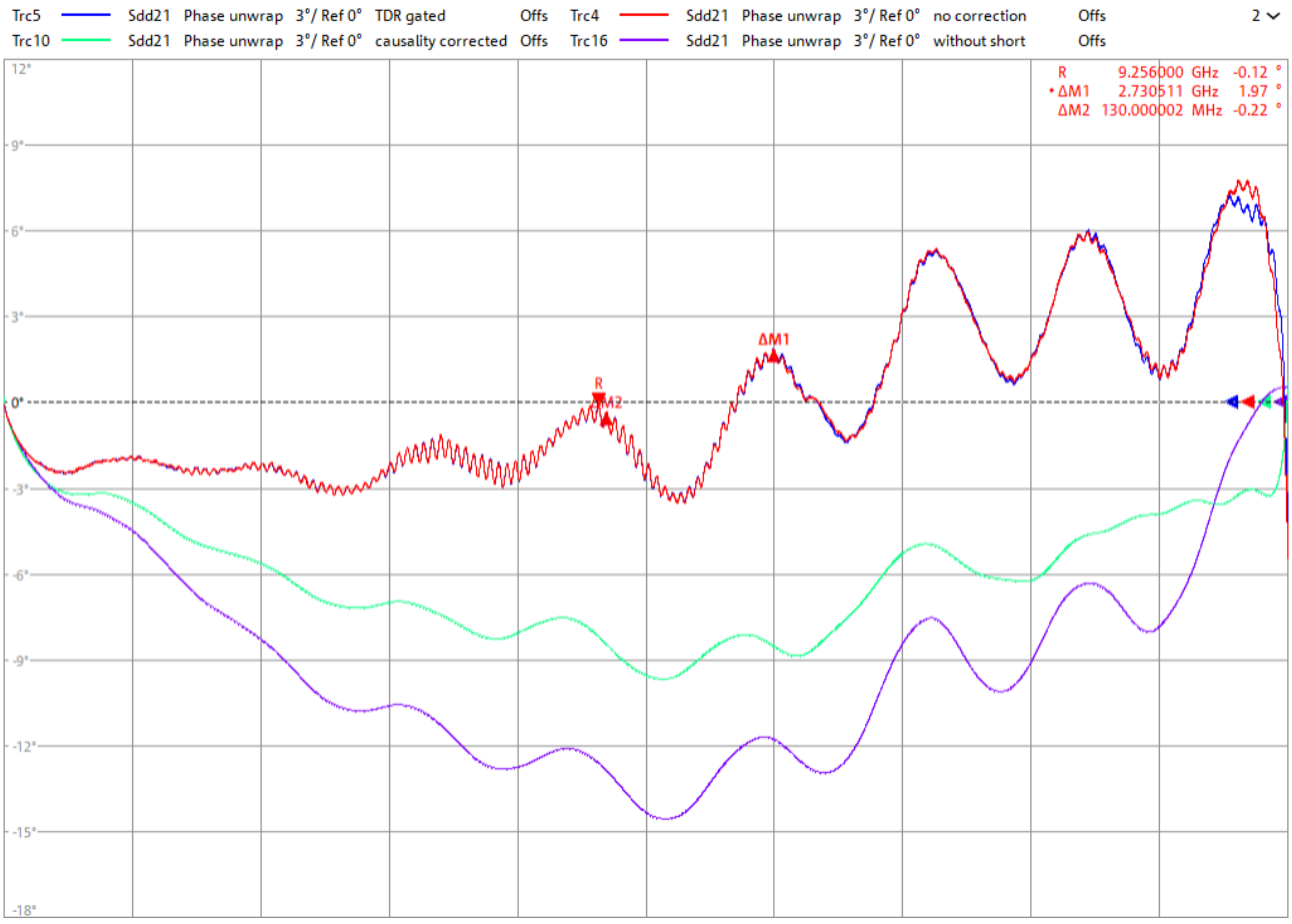


Figure 27 phase comparison of the adjusted models

Figure 28 displays the delay vs. frequency of the models, which has essentially the same message as the phase plot (see Figure 27). In this figure, it is also obvious that the delay variation of the causality corrected model (Trc11) is smaller than the model without short (Trc17), which can be read out from the Pk-Pk measurement (20 vs. 33 ps).

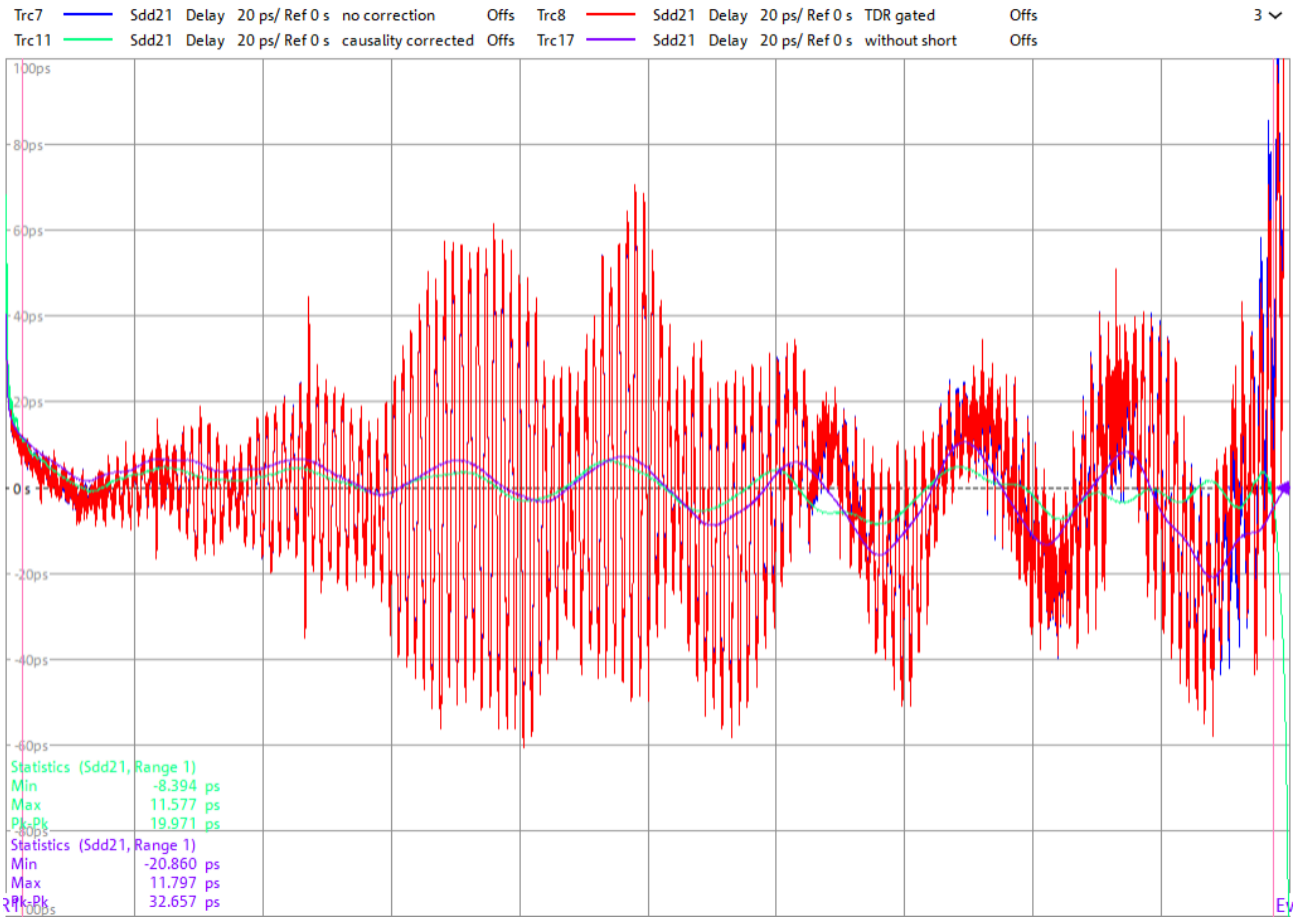


Figure 28 comparison delay of the adjusted models

As a final analysis, Figure 29 displays the TDR (time domain reflectometry) S_{DD11} and TDT (time domain transmissiometry) S_{DD21} of all models vs. time. Only the causality corrected model (Trc12, Trc20) shows no signal components before t=0. All of the other models have signal components in the negative time range. Particularly notable is the TDR gated model, which shows a signal component in the TDT (Trc13) indicated by the M2 marker. Both uncorrected models, with and without short, show larger signal components in the negative range.

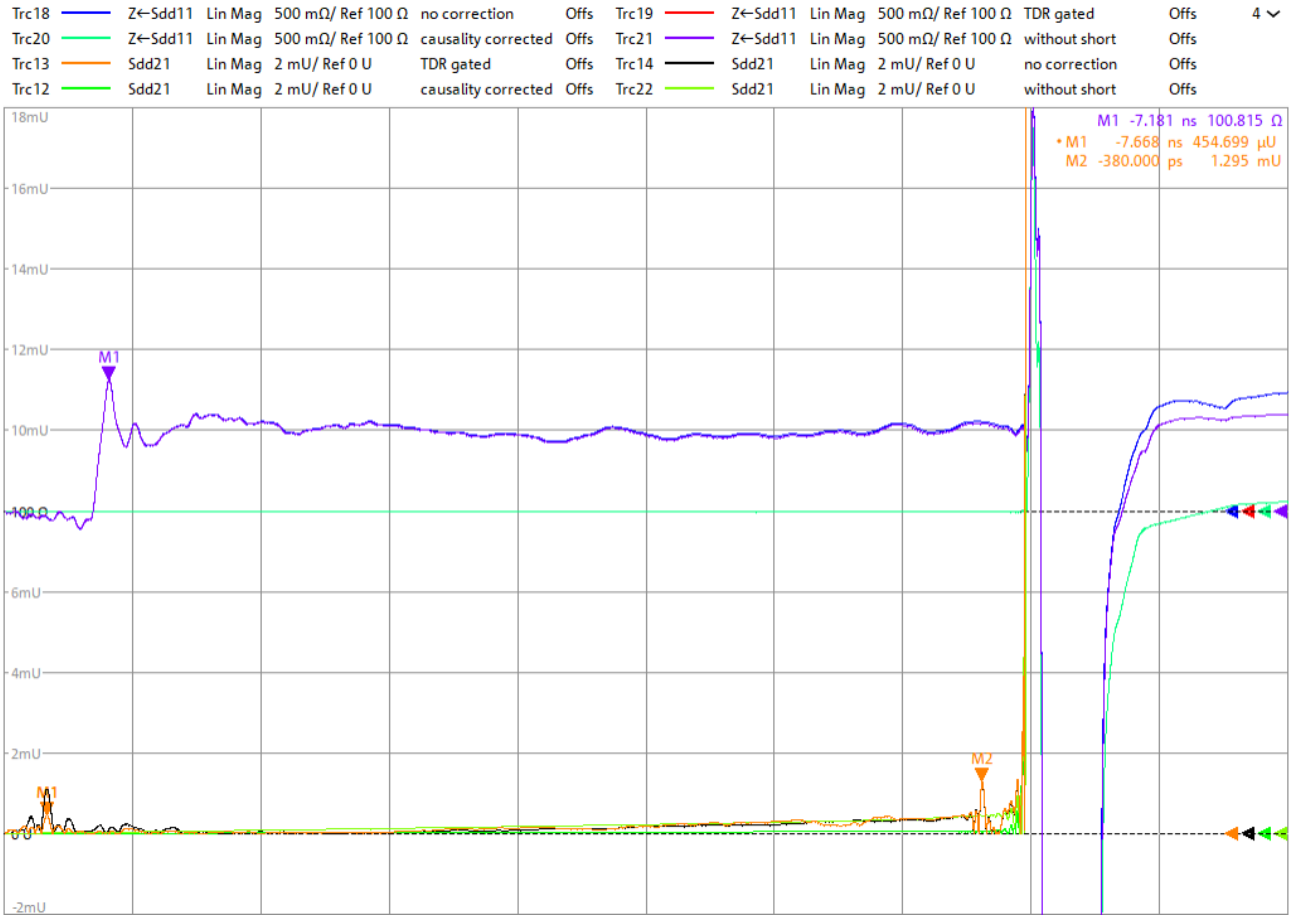


Figure 29 comparison of TDR and TDT of the adjusted models

In summary it can be stated that the model generation using a short improves the accuracy of the model, but only if causality correction is performed on the model in a subsequent step. A simple time gating of the model is insufficient.

Models without the short measurement are inaccurate at lower frequencies, and demonstrate a larger phase deviation from the linear phase. The next chapter shows the effects of the models when applied during measurements with an oscilloscope in the time domain.

4 Oscilloscope measurements

4.1 Setup

In order to analyze the USB signal on the oscilloscope, the following setup is necessary (see Figure 30). The TX side was chosen to enable the use of an oscilloscope for the time domain analysis. The RTP164 is connected via channels 1 & 3 to the TX1 port on the left-side of the test fixture (TF (1)). The ARB generator is connected via another test fixture (TF (2)) and a USB cable with a Type-C connector to apply the low frequency periodic signaling pattern (LFPS) in order to switch between various compliance patterns. The DUT is connected to the receptacle of the fixture (Type-C), as well as the power supply for the DUT.

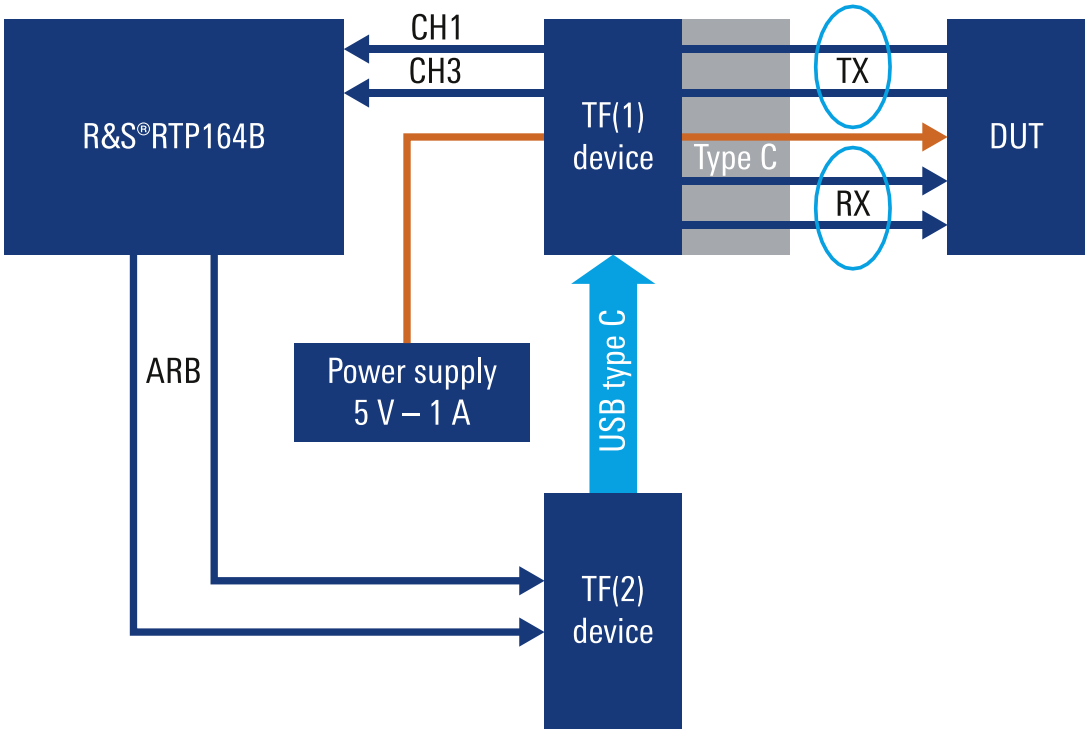


Figure 30 setup for the oscilloscope measurements

Two measurements were chosen in order to assess the impact of the deembedding on the oscilloscope measurements. First, the eye pattern is used to get statistical information, and then an advanced jitter analysis is performed.

The applied compliance test pattern for the analysis is based on the data rate. After power-up, the DUT starts with a CP0 pattern. This corresponds to a USB3.2 Gen 1 signal with a data rate of 5 Gbps. Using the ARB

generator, the applied LFPS pulse shifts the compliance pattern into the next state. After eight applied LFPS pulses, the DUT is in the CP9 state, and after a further three pulses, the CP12 state is reached. Both the CP9 and CP12 states issue a data pattern with a data rate of 10 Gbps (Table 4).

Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences.
CP9		Pseudo-random data pattern
CP12	LFSR15	Uncoded LFSR15 for PHY level testing and fault isolation. This is not 128b132b encoded. The polynomial is $x^{15}+x^{14}+1$

Table 4 excerpt from Compliance Pattern Sequences (Table 6-14) [6]

4.2 Oscilloscope setup

This section, describes the necessary setup for the oscilloscope. Starting from a PRESET state, always set the vertical scale to 80% of the full range, and if necessary due to the deembedding, adjust all of the settings The sampling rate is kept at the maximum of 40 GSa and the horizontal range is set to 200 µs range.

Channel 1 and channel 3 are combined into a differential channel. The common mode channel is additionally visible as a live icon. Skew adjustment is done on channel 3

To ensure reproducible results it is important to the setting of the trigger properly. An edge trigger will not generate the correct eye pattern as only transitions are visible, which is why the HW CDR trigger is chosen for the differential channel with the relative bandwidth set to 500 or 667 for a data rate of 5 or 10 Gbps, respectively.

, The RTP164B analysis tool is used in order to segment and display recorded data for the eye analysis.

Deembedding is set up with all of the necessary components because there are test fixtures, phase matched cables (RT-ZA17) and adapters (RT-ZA16), as shown in Figure 31. Due to the differential channel configuration, deembedding is also setup differentially.

Tip: It is important to model all of the components, even if the insertion loss is low. The phase still plays an important role in deembedding the complex S-parameters. Neglecting elements and their contribution to phase shifts will lead to *incorrect results*.

Figure 31 Deembedding setup with necessary components

If there is no deembedding, it is simply disabled in the dialog (Figure 31). For all other cases, deembedding is enabled and the open-DUT, open-short-DUT, open -2xthru, open-short-2xthru or sym-2xthru model is loaded as the appropriate touchstone file (*.s4p) in the component dialog for “Fixture 1” (Figure 32). Depending on the port configuration of the touchstone file (1,2,3,4, or 1,3,2,4), the port assignment can be adjusted, and the magnitude response of S_{21} or S_{31} will indicate the correct assignment. As a sanity check for a test fixture for the correct port assignment – like 1,3,2,4 – the insertion loss (magnitude S_{21}) of a single port limited by the PCB material should start at 0 dB and then decrease in a nearly linear fashion at higher frequencies.

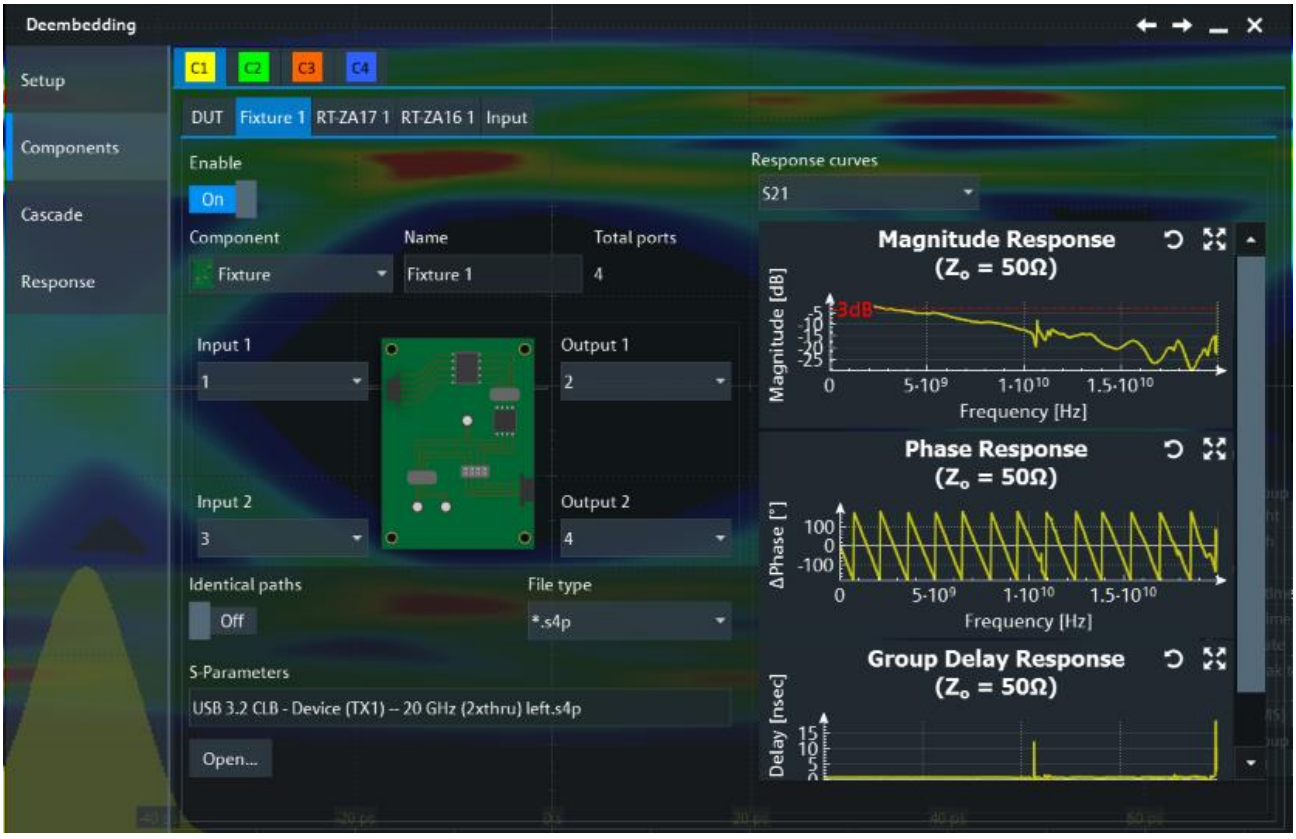


Figure 32 Configuring the fixture in the Deembedding dialog

Once deembedding is configured, a review of the overall calculated response (see Figure 33) is important for ensuring good or valid measurement results. The matters requiring attention are:

- ► The normalized magnitude should be flat up to the deembedding bandwidth
- ► The group delay response should not be excessively negative
- ► The normalized step response should not show significant ringing
- ► The attenuation Att_{max}, depending on the resolution of the scope, should not be so large that it unnecessarily magnifies the instrument's noise floor and causes a loss of the instrument's dynamic range.

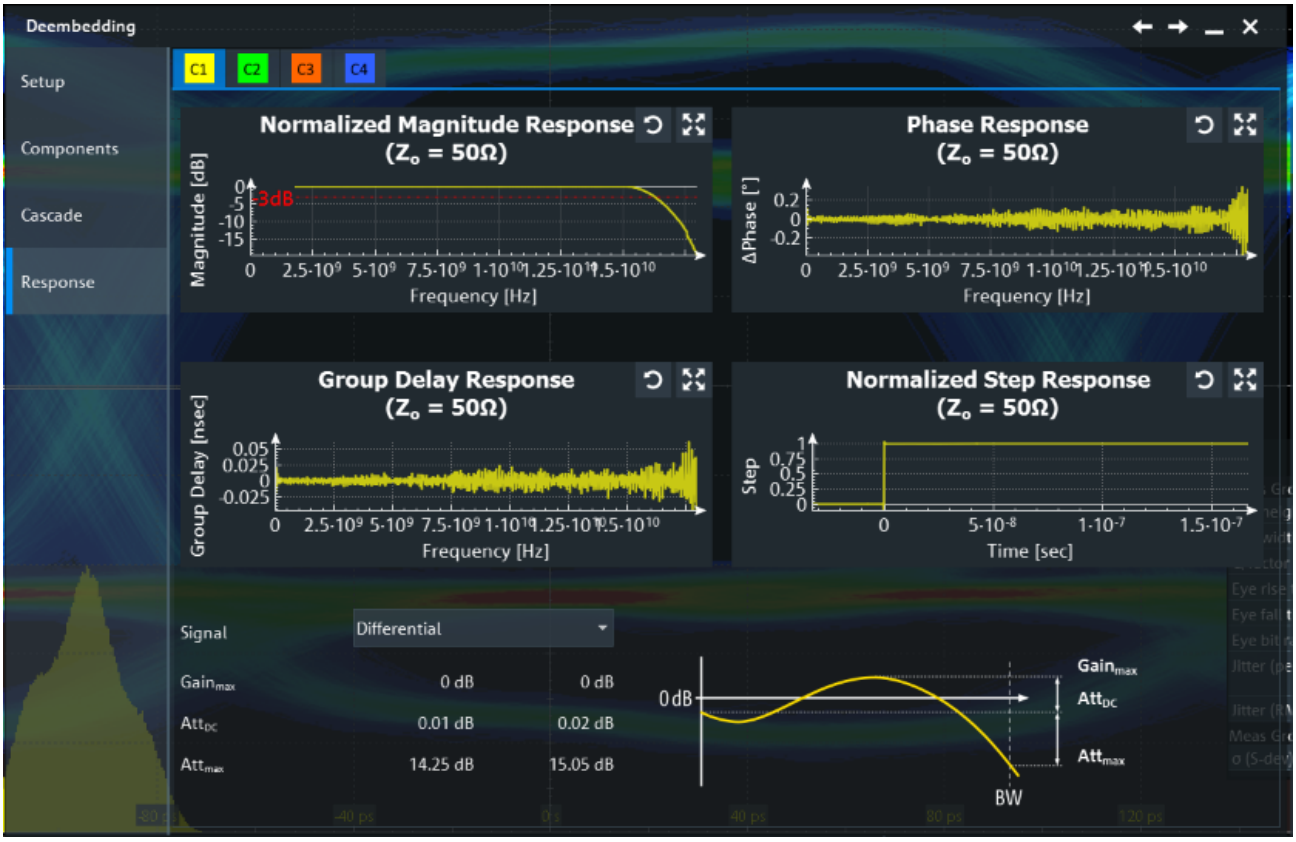


Figure 33 Quick check of the overall calculated Response of loaded Deembedding data

4.3 Eye pattern measurement

The eye pattern measurement was taken at 5 Gbps and 10 Gbps, or USB3.2 Gen 1 and Gen 2, respectively. The measurement of the setup without deembedding is compared to the four generated models. For reference, the 2xthru with a symmetrical split is also applied to show effects in the time domain.

The eye measurement shows what has changed, so that the effects of the deembedded model can be evaluated. The rise and fall time are measured with a 20% to 80% limit based on the high and low data levels, not on the preshoot and deemphasis levels.

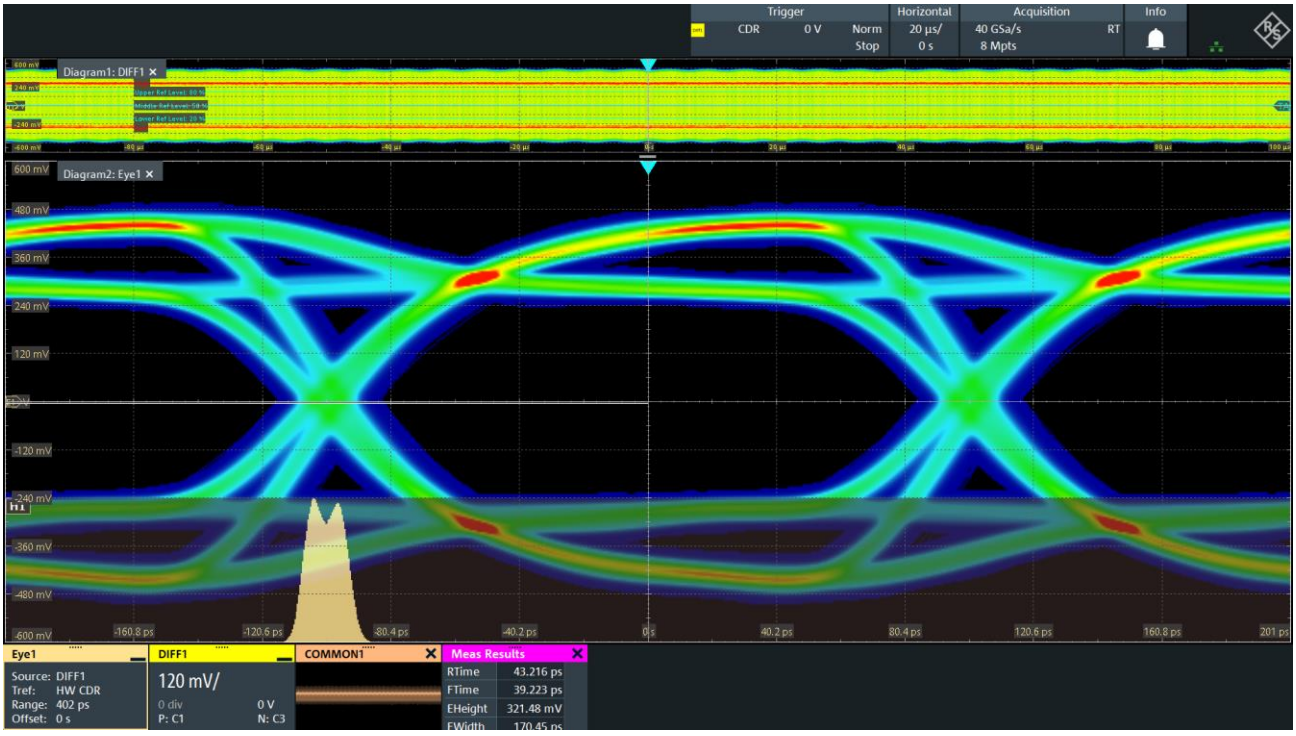


Figure 34 eye pattern of the USB3.2 Gen 1 data without deembedding

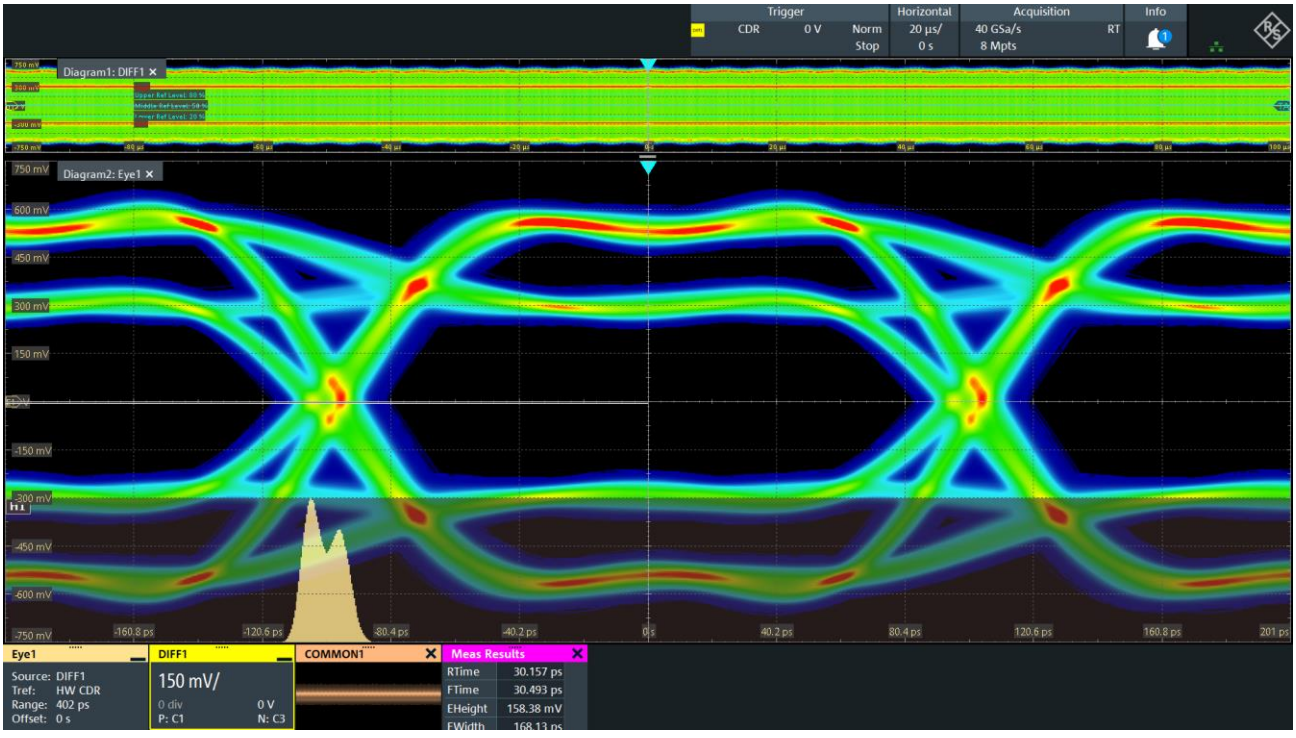


Figure 35 eye pattern of the USB3.2 Gen 1 data with deembedding via the sym-2xthru model

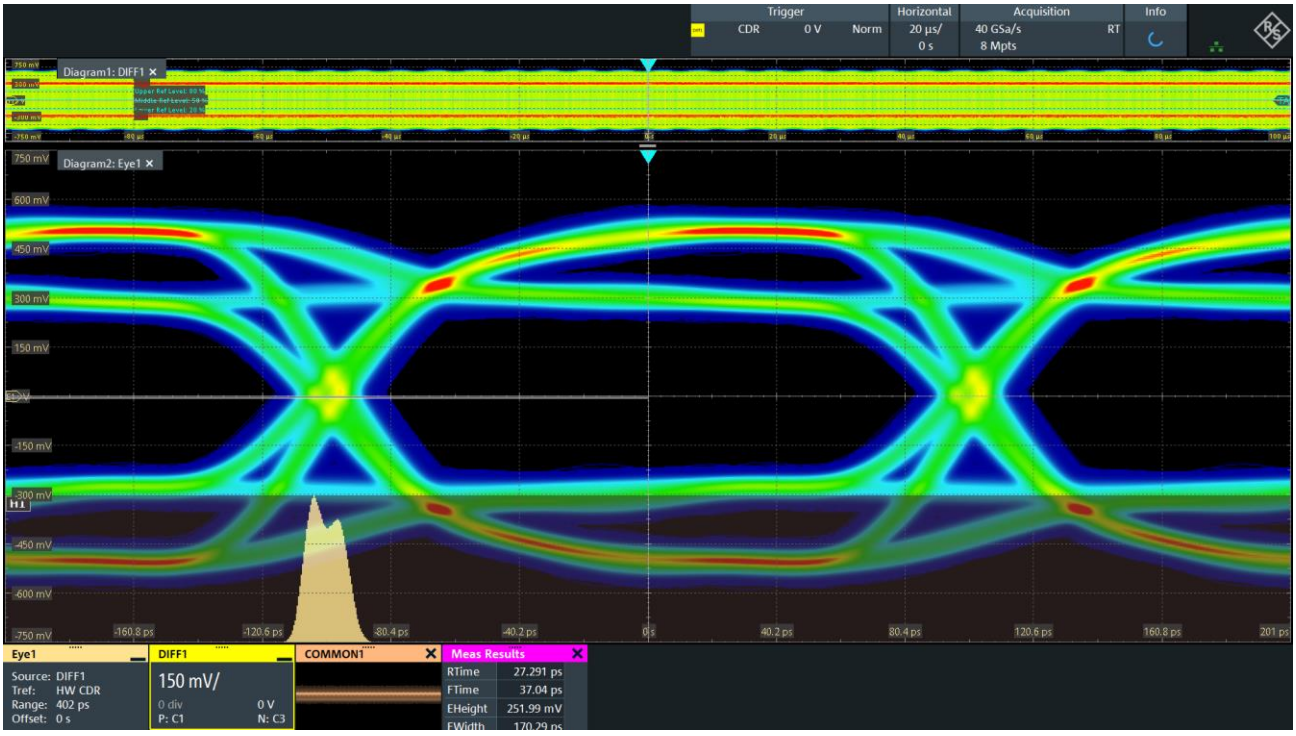


Figure 36 eye pattern of the USB3.2 Gen 1 data with deembedding via the open-short-DUT model

Comparing the eye patterns based on the deembedding, the most obvious change is preshoot / deemphasis. For the eye pattern without deembedding the preshoot / deemphasis shows a low pass filtered effect due to the insertion loss (Figure 34 – [-40 ps to 0 ps]). For the eye pattern with deembedding of the sym-2xthru model this effect seems to be overcompensated and an overshoot appears (Figure 35). Figure 36 illustrates the deembedding of the open-short-DUT model which shows the best behavior by compensating for insertion loss without any overshoot.

Configuration	Data rate [Gbps]	Measurement			
		t_r [ps]	t_f [ps]	j_{rms} [ps]	Q_f
Off	5	36.4	35.1	5.03	5.3
sym-2xthru		19.3	19.5	4.77	3.6
open-2xthru		29.8	29.319.5	4.97	4.4
open-short-2xthru		29.6	29.1	5.05	4.3
open-DUT		29.8	29.3	4.97	4.4
open-short-DUT		29.6	29.2	4.29	4.3
Off	10	45.5	43.4	3.21	10.8
sym-2xthru		24.4	24.7	3.52	7.0
open-2xthru		35.9	34.5	3.23	11.7
open-short-2xthru		36	34.6	3.34	11.4
open-DUT		35.8	29.234.6	3.25	11.8
open-short-DUT		36	34.6	3.36	11.4

Table 5 model configurations with selected signal parameters

Table 5 provides a complete comparison for eye pattern measurement. It is important to note that the rise and fall times in the table are the mean values for all transitions in the acquisition. These values do not match the

previous screenshots, as in the displayed, iconized measurements. Only the current value is shown and not the mean value.

The data show an improvement in the rise and fall time for the deembedding cases, but no significant improvement in rms jitter compared to the case without deembedding. This is interesting, because for a measured data signal, a decrease in rise and fall time reduces jitter. But in this case the decrease in rise and fall time results from deembedding. A further discussion about why this expectation is not fulfilled can be found in Chapter 4.4, which takes a closer look at the signal using advanced jitter separation methods.

In addition, the 2xthru model yields a very short rise and fall time, while the four other models have a fairly consistent variation of only 0.1 ps. Additionally, an unrealistic overshoot can be observed and measured for the 2xthru model, which adds to concerns about the validity of this model.

4.4 Advanced Jitter Analysis

Advanced jitter analysis is set up by changing the time base to 8 M samples, equivalent to 200 µs acquisition time with 25 ps resolution. This enables the capture of jitter residuals of the SSC (spread spectrum clocking) of approximately 33 kHz. It will be discovered as a periodic jitter and consequently not be considered as an effect of the deembedding. The analyzed trace is still the differential channel. In order to compare the eye measurement and the advanced jitter measurement, the rise and fall time is measured not only on the trace but also on the estimated step response.

To make the captured waveforms comparable, the serial pattern trigger is used to ensure that the same data is always captured for the analysis. The pattern for the 5 Gbps (CP0, see Table 4) mode will differ from the 10 Gbps (CP12) mode.

The specific advanced jitter separation setup on the NRZ data of the differential channel starts with a software based CDR (clock data recovery) analysis. This is set to PLL with either a 5 Gbps data rate and a relative bandwidth of 500, or a 10 Gbps data rate with a 667 relative bandwidth, respectively. The “Estimate Bit Rate” button helps to find the actual data rate of the investigated transmitted signal.

The “(Other) Bounded Uncorrelated *(OBUJ)* Estimation” option is enabled, to make sure that no crosstalk is present because this would increase the OBUJ significantly. The estimated step response is set to 20% step position with a length of 20 UI.

The results of interest are listed in Table 6 and additionally in the screenshots of the measured and calculated bathtub curves. The estimated step responses are also shown.

Component	Hist	Track	Spectrum	Comment
Event count				For a comparable statistic
TJ@BER				Supports the bathtub analysis
RJ + (O)BUJ	✓		✓	Non-uniform spectrum indicates issues in the separation
DJ (δ-δ)				

Component	Hist	Track	Spectrum	Comment
TJ	✓	✓	✓	Track indicates PLL locking problems, spectrum indicates potential issues in the separation
DDJ	✓			The assumption is that DDJ will be affected by deembedding
DCD				Indication of offset
PJ	✓			PJ histogram might have an impact on the TJ histogram
ISI				
(O)BUJ	✓			Small histogram indicates no crosstalk
RJ	✓			Should be gaussian and independent of the applied deembedding

Table 6 selected advanced jitter results for display

Figure 37 shows the advanced jitter results for the 5 Gbps mode without deembedding. On the upper left, all histograms of TJ[1], DDJ, PJ, RJ and OBUJ are shown. To the left, the measured and calculated bathtub curve is displayed, as is the list of periodic components.

The bottom row displays the estimated step response and the calculated values of the jitter separation.

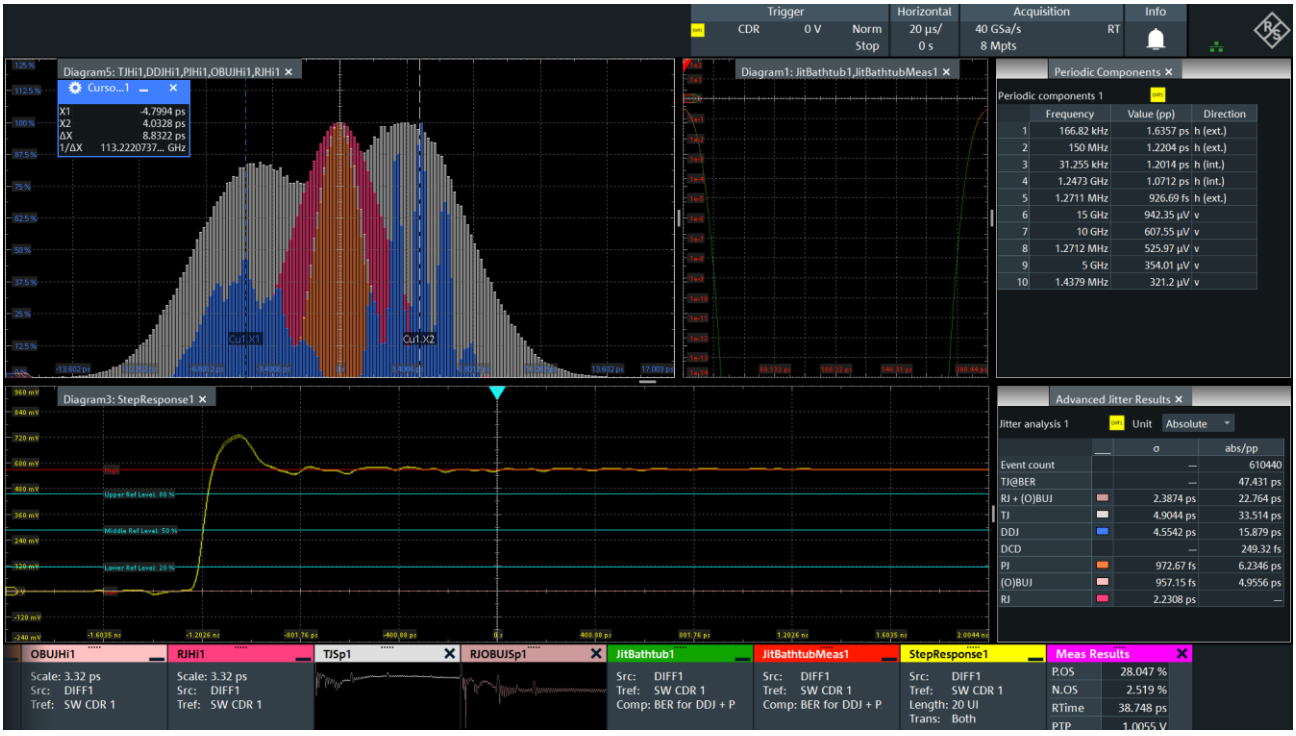


Figure 37 advanced jitter analysis of a USB3.2 Gen 1 signal with no deembedding

The screenshot also shows the spectrum of the TJ and RJ+OBUJ iconized. Here, the important fact is that the RJ spectrum is flat and consists of white noise. As a consequence, this is an indication that the separation is working well.

[1] TJ: total jitter; DDJ: data dependent jitter; PJ: periodic jitter; RJ: random jitter; OBUJ: other bounded uncorrelated jitter

The next step is to compare the results of the jitter separation in Table 7 across all of the models. In the results, it is important to distinguish between the 5 Gbps and the 10 Gbps modes because the results may differ depending on the mode.

Configuration	Data rate [Gbps]	Measurements on jitter separation							
		t_r [ps]	OV [%]	TJ [ps]	DDJ [ps]	DCD [ps]	PJ [ps]	OBUJ [ps]	RJ [ps]
Off	5	38.8	28.0	4.9	4.6	0.2	1.0	1.0	2.2
sym-2xthru		23.5	48.0	4.7	4.0	0.6	1.0	0.1	2.5
open-2xthru		30.4	37.9	4.9	4.5	0.0	1.0	0.9	2.3
open-short-2xthru		30.2	39.7	5.0	4.6	0.0	1.0	1.0	2.3
open-DUT		30.3	38.5	4.9	4.5	0.0	0.9	0.1	2.4
open-short-DUT		30.2	39.7	5.0	4.6	0.1	1.0	0.9	2.3
open-short-DUT (causal)		30.2	39.7	5.0	4.6	0.1	1.0	1.1	2.2
Off	10	49.3	35.3	3.3	2.2	0.7	0.8	0.1	1.9
sym-2xthru		24.2	19.7	3.6	2.8	1.3	0.7	0.1	2.0
open-2xthru		35.8		3.3	2.3	0.3	0.1	0.1	1.9
open-short-2xthru		35.7		3.4	2.5	0.3	0.8	0.7	1.9
open-DUT		35.8		3.3	2.3	0.6	0.7	0.7	1.9
open-short-DUT		35.7		3.4	2.5	0.6	0.7	0.1	1.9
open-short-DUT (causal)		34.8		3.5	2.7	2.0	0.7	0.1	2.0

Table 7 Advanced jitter results[2]

The rise time of the estimated step response coincides well with the measured rise time of the real signal (see Table 5). In this case, it also indicates that the rise time for the 2xthru model is too small compared to the other models.

Similar to the previous measurement, the relative overshoot voltage (OV) of the estimated step response in 5 Gbps mode – at 48% for the 2xthru model – is larger than the approx. 39% in the other models.

The total jitter (TJ) – at 4.9 ps for 5 Gbps and 3.3 ps for 10 Gbps – is quite consistent, though the DDJ appears lower for the sym-2xthru model. All other jitter contributions are within the same range and do not differ much.

The final step is to plot the DDJ distributions as histograms (see Figure 39 and Figure 40). Before analyzing them in detail, it is helpful to understand how the DDJ histogram should look. Figure 38 shows an ideal, symmetrical eye pattern for a data signal with preshoot and deemphasis. The horizontal axis is the time with the unit interval (UI) noted down. The vertical axis shows the signal level. As all rising transitions, as well as the falling ones, have two starting points, either with or without preshoot, this leads for this idealized eye to two different, distinct jitter values. As a consequence, the jitter histogram for the ideal signal with preshoot and deemphasis looks bimodal as opposed to a regular, ideal NRZ signal.

[2] t_r, OV, and DCD are absolute values, the remaining values are expressed as standard deviation

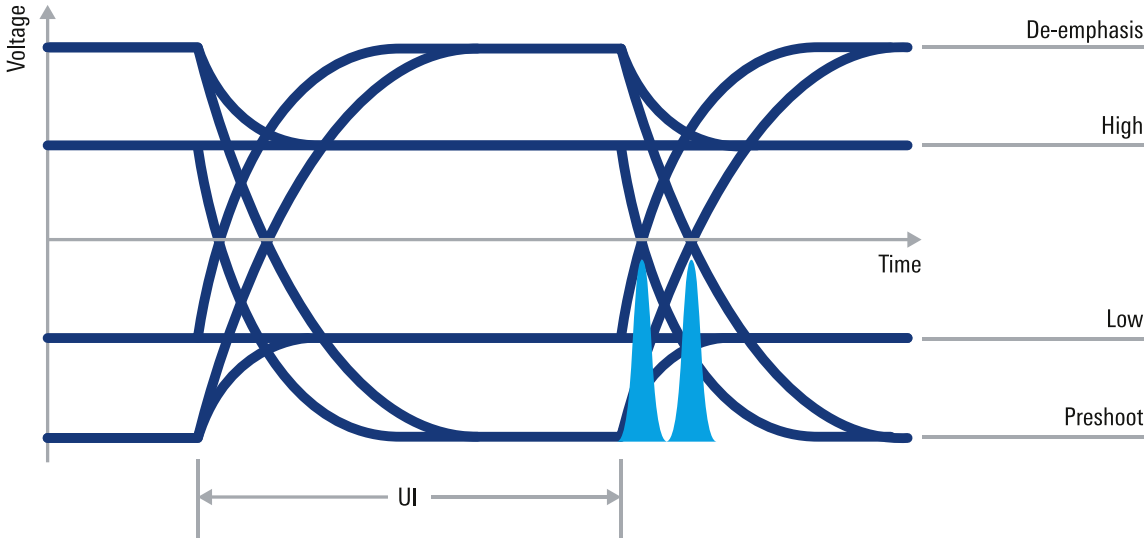


Figure 38 eye pattern with deemphasis and preshoot

For the acquired signal, this means that the histogram will approximately show a bimodal Gaussian distribution. For better readability, the histograms are plotted as lines, rather than bar charts and multiple DDJ are displayed in one diagram with the DDJ measurement without deembedding (off) serving as a reference.

Figure 39 shows that the 2xthru model pushes the DDJ distribution towards the center as opposed to the DDJ without deembedding. This behavior is an indication of a reduced channel BW.

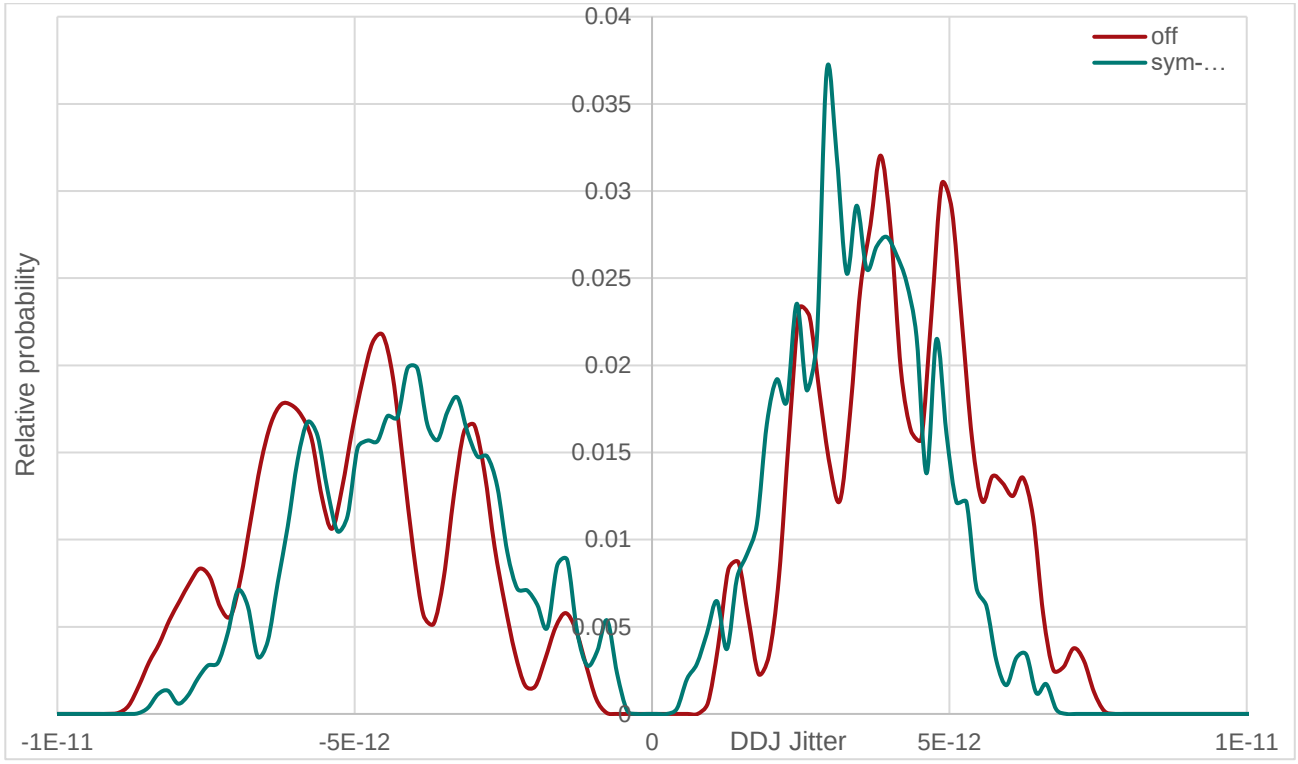


Figure 39 DDJ jitter histogram for no deembedding and 2xthru deembedding

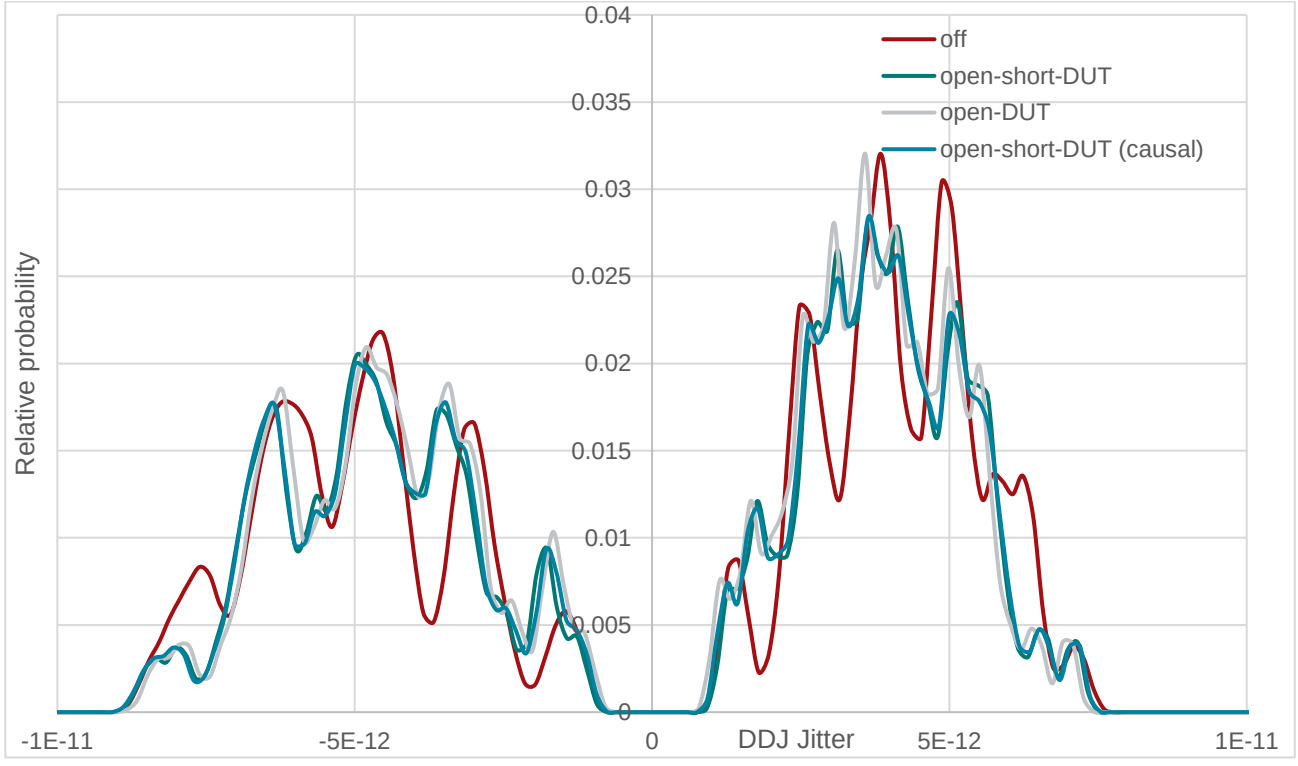


Figure 40 DDJ jitter histogram for no deembedding and DUT based deembedding

In contrast to this is Figure 40, which shows a plot of the DDJ histograms based on the other four DUT models plus the DDJ histogram without deembedding. The DUT based distributions occupy the same time range as

the distribution without deembedding, but the distributions based on the DUT deembedding appear smoother with smaller notches. This is in fact an indication for a successful deembedding, which results in an undisturbed channel.

The histogram for the open-2xthru and open-short-2xthru show a similar result, but for the 10 Gbps signal, the bandwidth of the scope is a limiting factor. The result is that the histogram converges to a Gaussian probability density distribution.

As a final comparison, the estimated step response of several models is correlated with each other and displayed in Figure 41. Again, the 5 Gbps data rate mode is used.

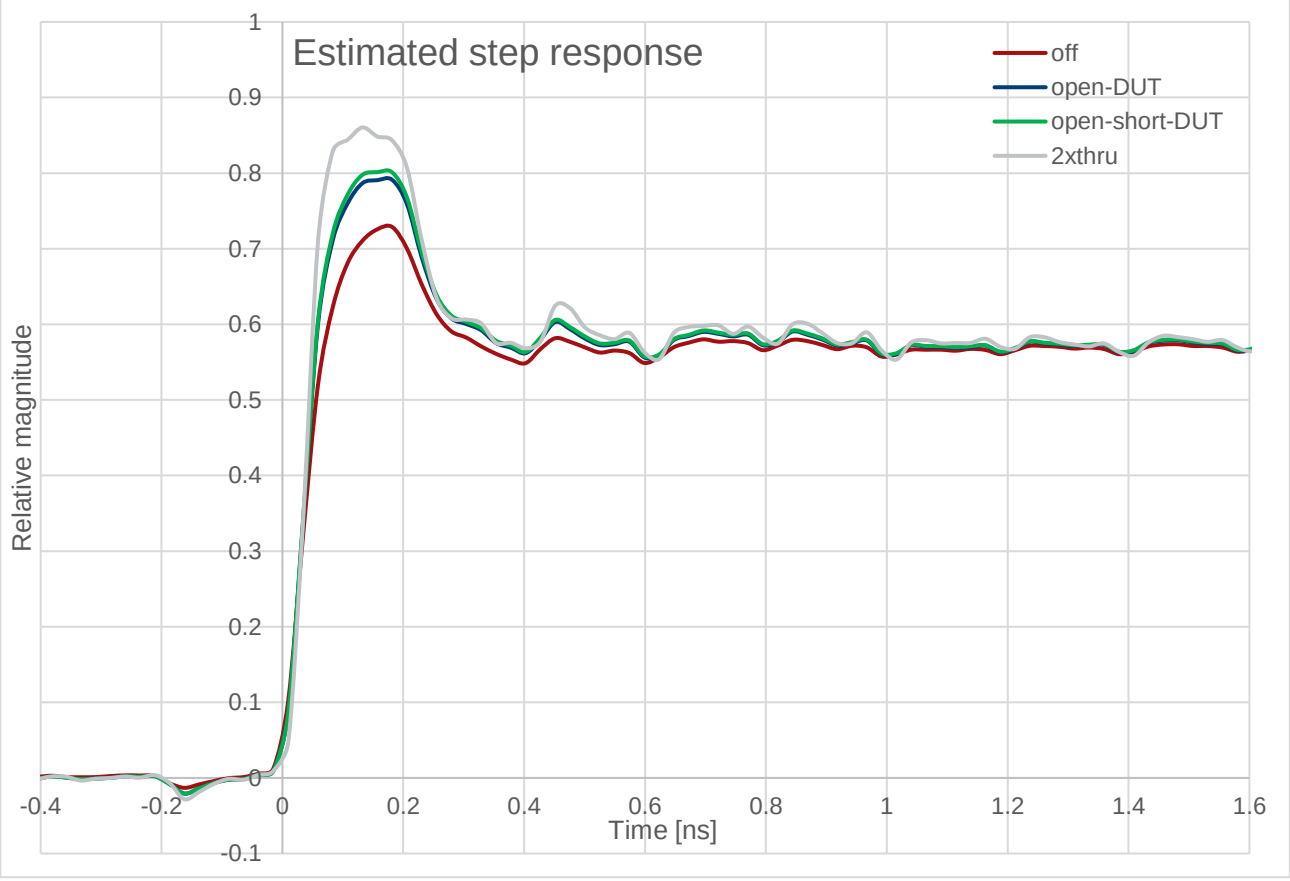


Figure 41 estimated step responses of the channel after deembedding for various models

The step response with no deembedding already shows quite a bit of frequency dependent attenuation, considering the short traces on the fixture. With deembedding the attenuation is gone and the level for the open-DUT and open-short-DUT model reach the compliant deemphasis $V_{TX\text{-}DE\text{-}RATIO}$ [3 to 4] dB [6]. Also in this comparison the 2xthru model shows a too high deemphasis and a distortion on the top level (150 ps). The ringing on the trace originates from the brick wall filter in the input channel. The effect can be mitigated by using a higher order Bessel filter in the deembedding processing chain.

Another important finding from this scenario is that the influence of a causal model is barely noticeable. This can be seen in Figure 40 and in Table 7, where the DDJ distributions between the open-short-DUT model and the open-short-DUT model (causal) are nearly identical, as are the parameters in the table.

Chapter 3.3.5 concluded that introducing a causal model significantly increases the quality of the resulting model, but using these models in real-world deembedding with a wideband oscilloscope seems to diminish the importance of these effects. An oscilloscope is affected by the wideband noise of the acquisition and is not able to resolve such fine phase resolutions. Nevertheless, the more trustworthy and causal the model is, the fewer restrictions will arise when using these models for real measurements with an oscilloscope, and the results of analysis performed in simulation tools will be numerically more precise.

5 Summary

This application note demonstrates the characterization of a widespread test fixture for data-com applications using a vector network analyzer, it creates a model based on the characterization and applies the model to an oscilloscope. All of this was done end-to-end with the R&S®ZBNB20 and the R&S®RTP164B. This document investigated several ways to create the model, in particular a method that does not require a mated pair of fixtures, which offers users flexibility in the selection of a suitable method.

The quality of the model was assessed through an analysis in the frequency domain before loading the model onto the oscilloscope. Similarly, the different fixture models were compared on the oscilloscope and the differences were explained.

Overall, this application note showcases the comprehensive offering from Rohde & Schwarz for a complete end-to-end solution to characterize test fixtures with a VNA and analyze signals for a USB3.2 application with an oscilloscope where the influence of the test fixture is deembedded. This solution can be easily ported to other high-speed digital technologies in the datacom world.

6 Literature

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7 Ordering Information

Designation	Type	Order No.
Vector signal analyzer (4-port)	R&S®ZNB20	1334.3330.64
Torque wrench	R&S®ZN-ZTW	1328.8534.35
VNA calibration kit	R&S®ZN-Z235	1336.8500.02
In-situ Deembedding	R&S®ZNB-K220	1328.8605.02
License dongle	R&S®ZNPC	1325.6601.02
16GHz oscilloscope	R&S®RTP164B	1803.7000.16
Precision BNC adapters	R&S®RT-ZA16	1320.7074.02
Pair of phase matched cables	R&S®RT-ZA17	1337.8991.02

Designation	Type	Order No.
Jitter separation	R&S® RTx-K133	1800.6860.02
Advanced eye analysis	R&S® RTx-K137	1800.6983.02
High-speed serial pattern trigger	R&S® RTx-K141	1326.4560.02

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