HOW TO DEBUG SIGNAL INTEGRITY WITH POWER INTEGRITY?

Pasi Suhonen
Application Engineer

ROHDE&SCHWARZ
Make ideas real

DEFINITIONS

Signal Integrity

- Signal Integrity describes the ability of a system, to transmit and receive (data-) signals properly.

Power Integrity

- Power Integrity groups several measurements to qualify the quality of a power supply and distribution network.

Electromagnetic Compatibility (short: EMC)

- EMC describes the ability of a system to operate in its electromagnetic environment without causing interference in its environment.

COMMON SIGNAL AND POWER INTEGRITY PROBLEMS

Signal Integrity

- Signal Integrity describes the ability of a system, to transmit and receive (data-) signals properly.

- Common measurements:
  - Eye diagram
  - Jitter/Phase Noise
  - Crosstalk
  - Noise
  - Timing e.g. Skew, TIE, …

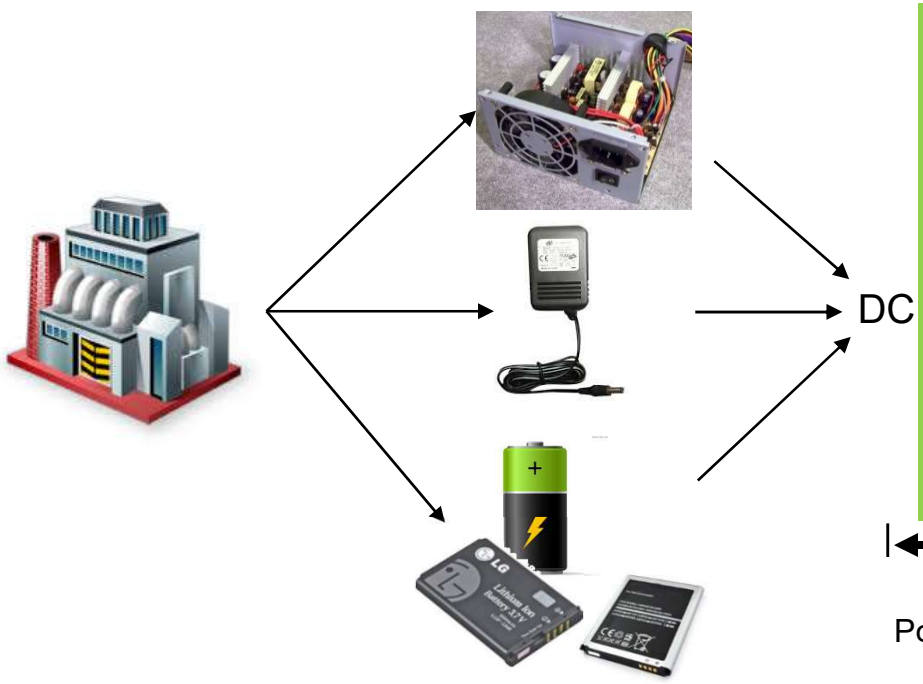
Power Integrity

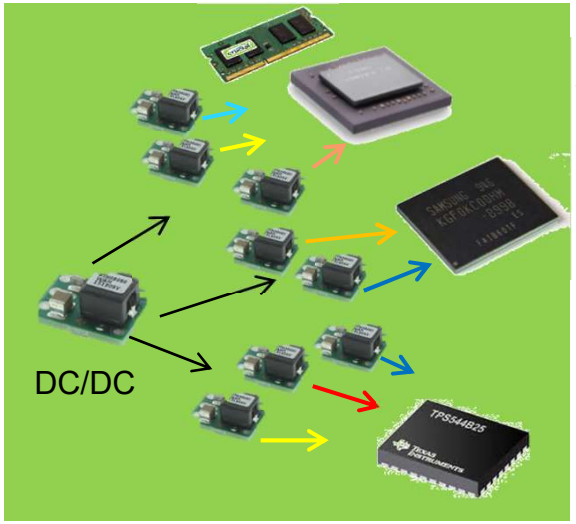
- Power Integrity groups several measurements to qualify the quality of a power supply and distribution network.
- Common measurements:
  - Voltage level and offset,
  - AC ripple / harmonics
  - Droops / distortions
  - Long term stability

Electromagnetic Compatibility (short: EMC)

- EMC describes the ability of a system to operate in its electromagnetic environment without causing interference in its environment.

WHAT DOES POWER INTEGRITY MEAN?

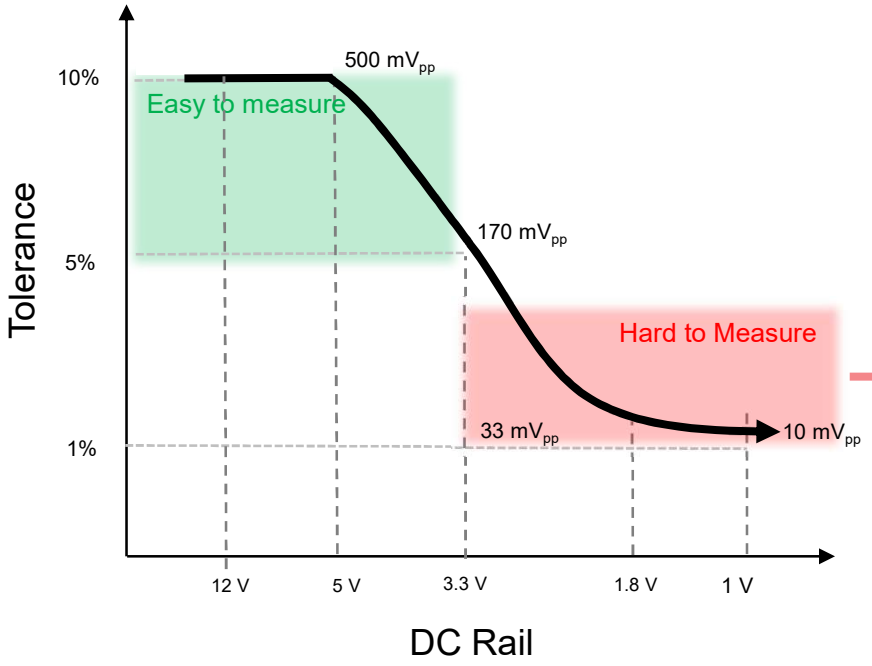




Typical Power Rail Quantities
- SSD: 12+
- RTO2K: 20+
- Tablet: 24+
- Network switch: ~56
- Next gen mobile: ~100

Power Integrity:
Analysis to determine quality of DC power from the output of the DC converter to ICs. Includes chip, board, & system.

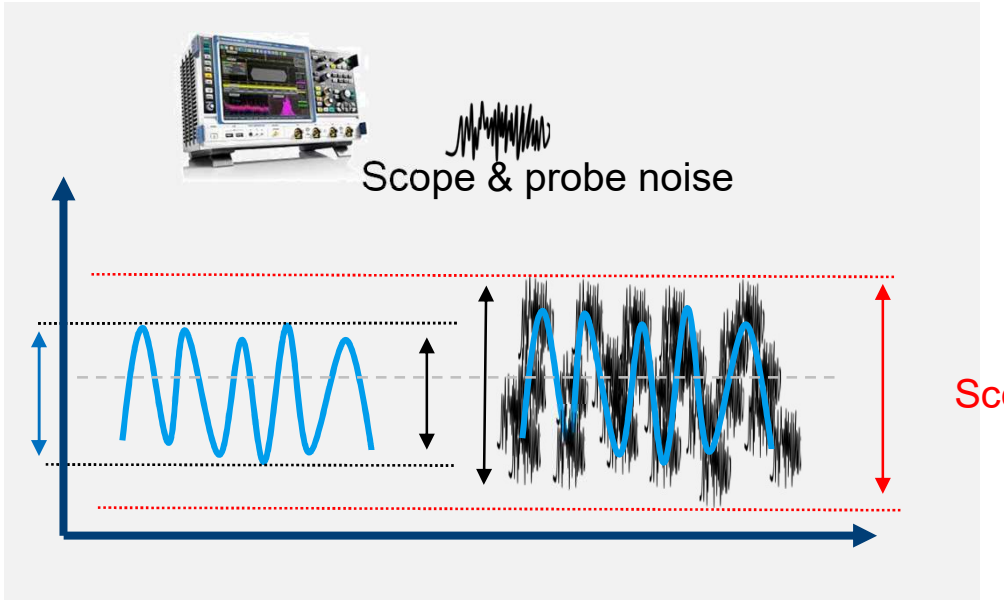
POWER RAIL MEASUREMENT CHALLENGES
LOWER RAIL VOLTAGES AND SMALLER TOLERANCES



Examples

Rail Value	Tolerance	Need to measure
3.3 V	1%	33 mV_{pp}
1.8 V	2 %	36 mV_{pp}
1.2 V	2 %	24 mV_{pp}
1 V	1 %	10 mV_{pp}

SEVERAL FACTORS MAKE IT DIFFICULT TO MEASURE SMALL SIGNALS

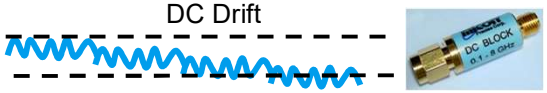


CHOOSE THE RIGHT PROBE

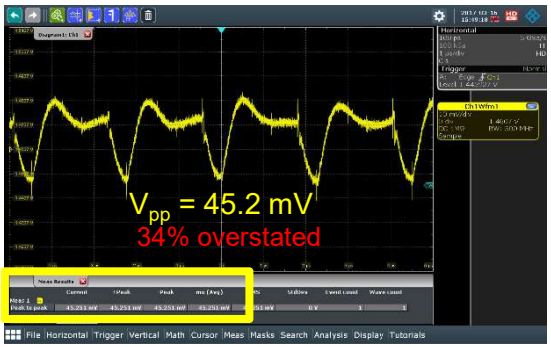
10:1 ZP10 passive 500 MHz BW

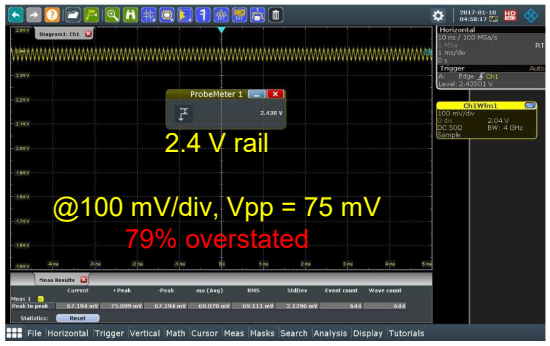
- Advantages
  - 500MHz Bandwidth with 10:1 attenuation
  - Good dynamic range
  - Readily available and low cost
- Disadvantages

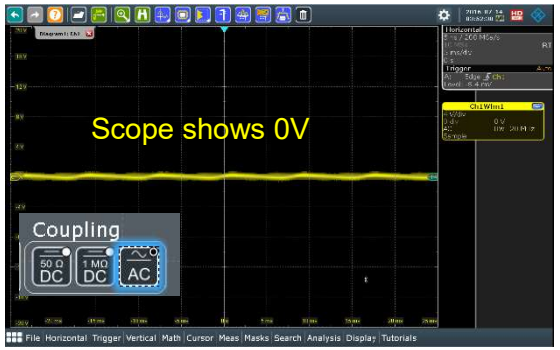
DC Drift



Using max built-in scope offset





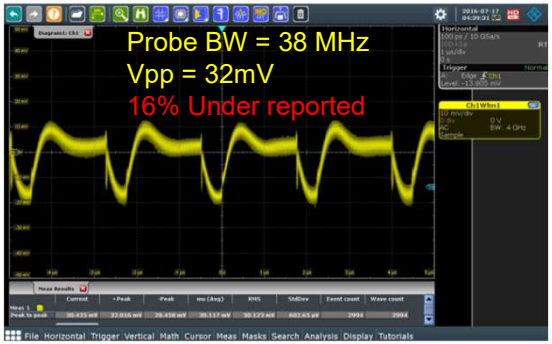


Can bring to center screen and zoom in / User can't tell absolute vertical value / User can't see DC offset issues

CHOOSE THE RIGHT PROBE

1:1 ZP1X passive 38 MHz BW

- Advantages
  - 1:1 attenuation
  - Good dynamic range with low noise
  - Very low cost
- Disadvantages



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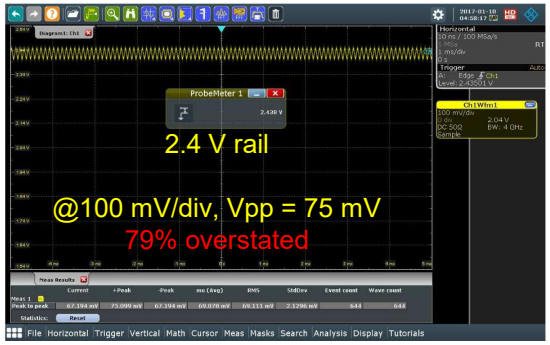
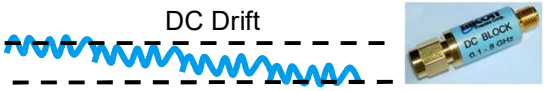
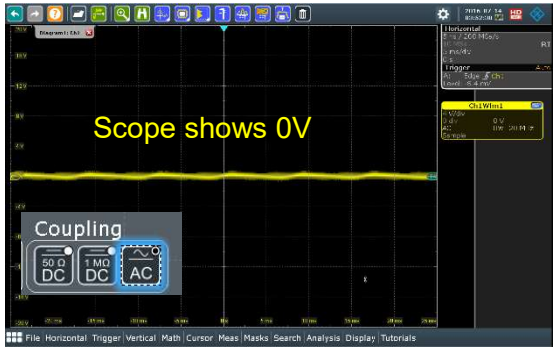


DC Drift



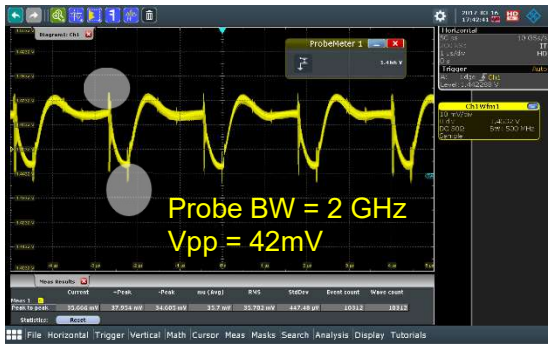


Can bring to center screen and zoom in / User can't tell absolute vertical value / User can't see DC offset issues

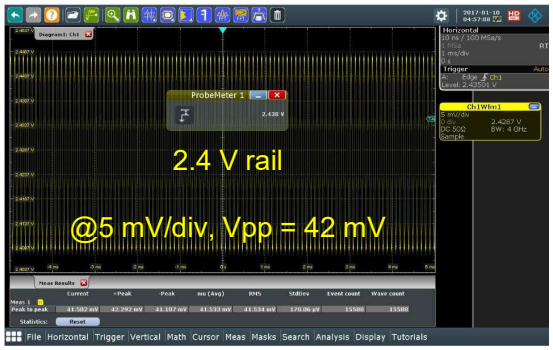
CHOOSE THE RIGHT PROBE

1:1 ZPR active 2 / 4 GHz BW

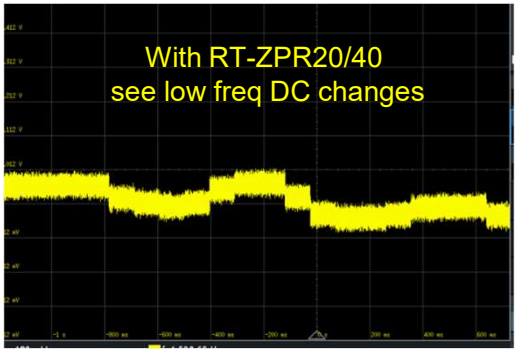
- Advantages
  - 1:1 attenuation with 2 / 4 GHz bandwidth
  - Very low noise
  - Built in offset compensation of ±60V
  - AC or DC coupling, 50kΩ resistance



Using built-in probe offset



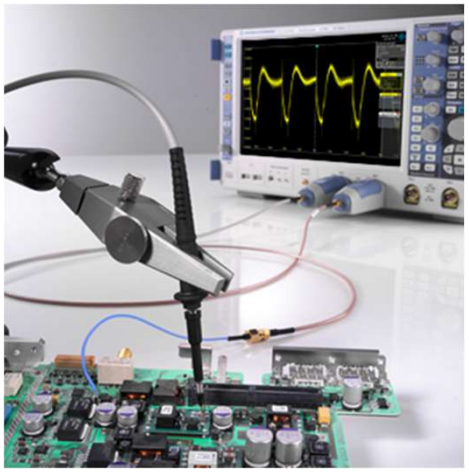
DC Drift



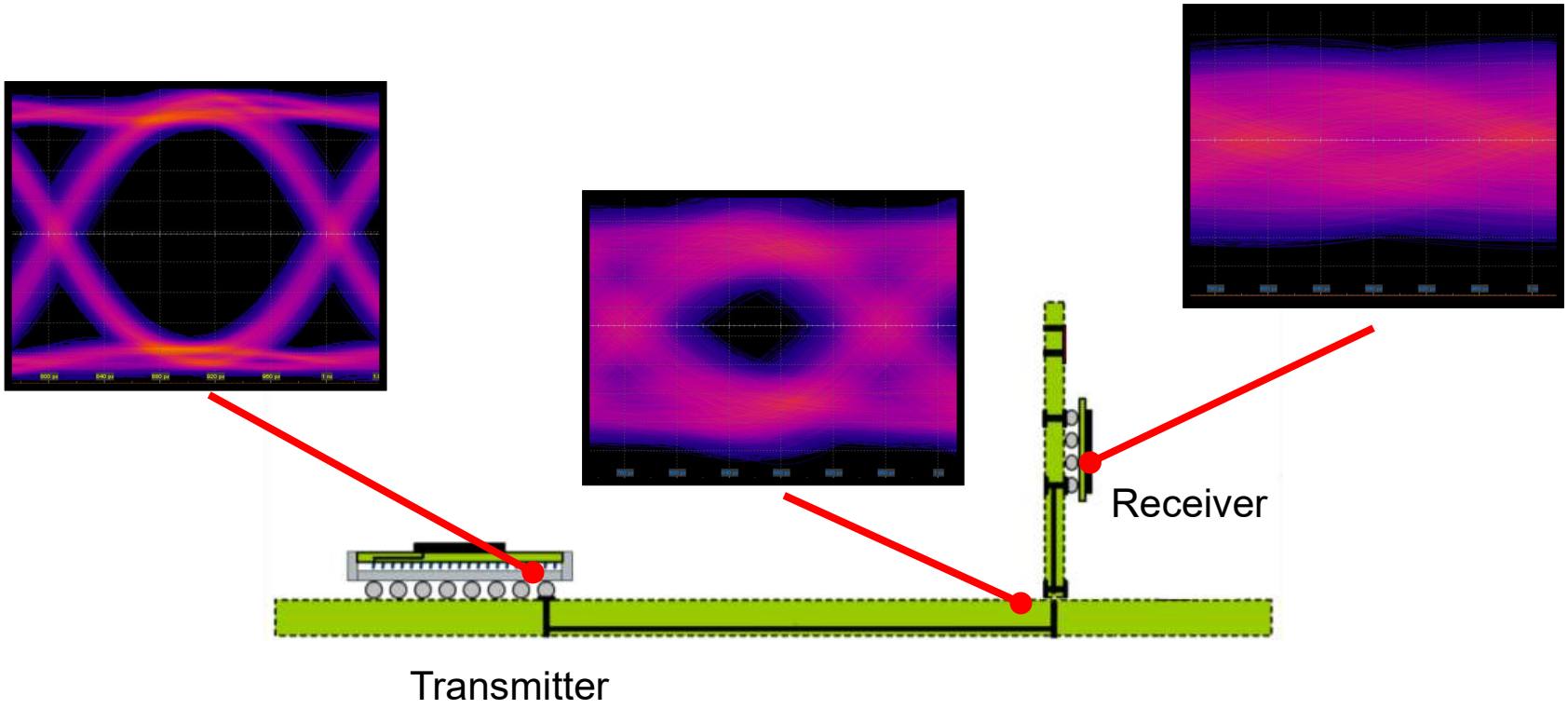
RT-ZPR20/40 – 2GHZ AND 4 GHZ POWER RAIL PROBES

- Designed uniquely for measuring small perturbations on power rails
- Active, single-ended probe
- Low noise with 1:1 attenuation
- Best in class offset compensation capability

Key Specifications	
Attenuation	**1:1**
Probe BW	**2 GHz / 4 GHz**
Browser BW	350 MHz
Dynamic Range	±850 mV
Offset Range	**> ±60 V**
Noise Scope (RTO) standalone Scope + Probe Noise (at 1 GHz, 1mV/div)	 107 µV AC_{rms} **120 µV AC_{rms}**
Input Resistance	**50 kΩ** @ DC
R&S ProbeMeter	Integrated
Coupling	DC or AC



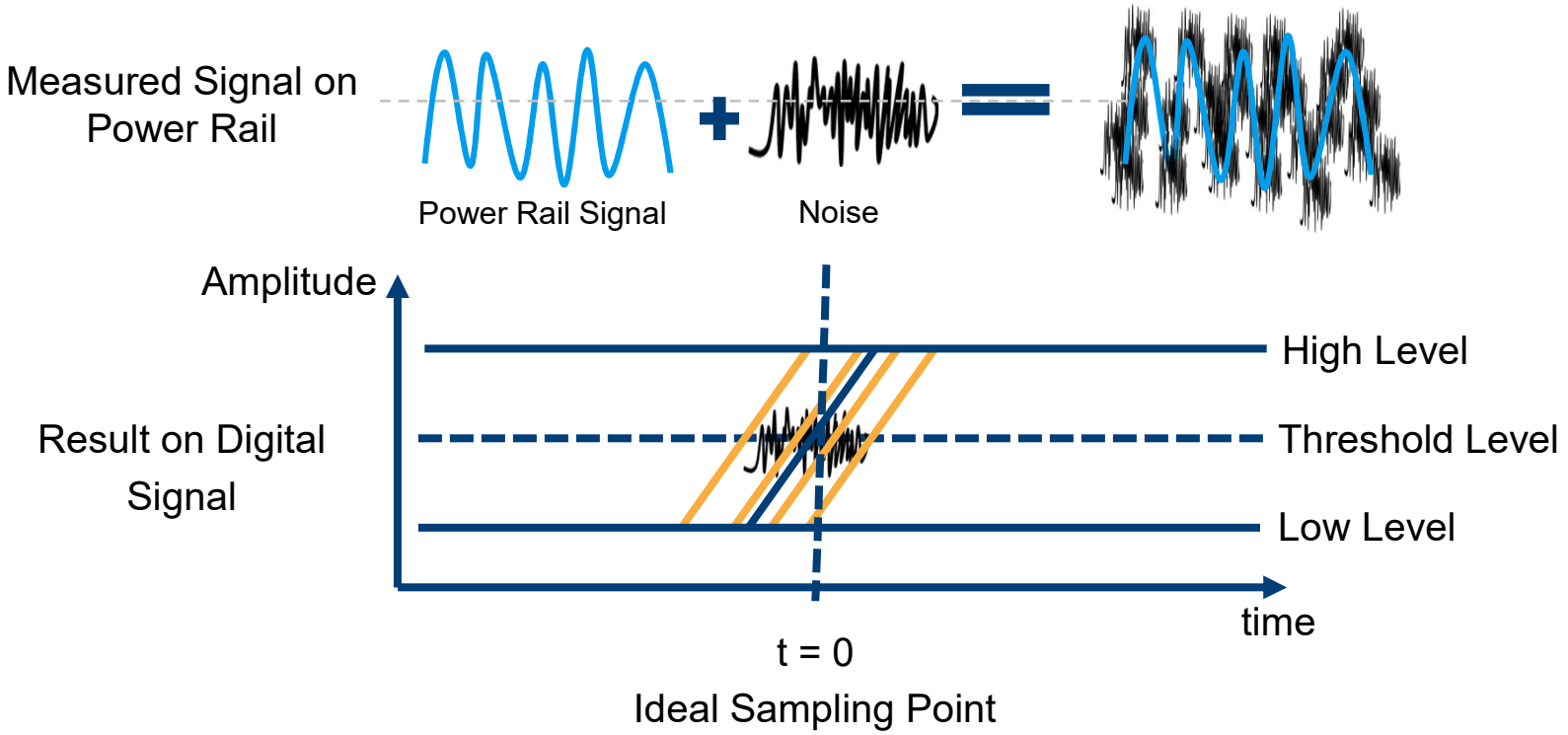
WHAT COULD POSSIBLY GO WRONG?



COMMON SIGNAL INTEGRITY PROBLEMS

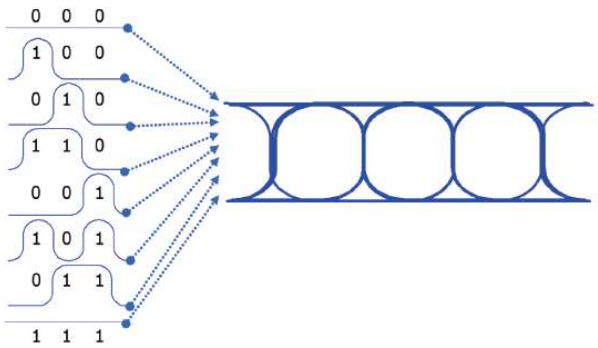
- Ringing (overshoot/undershoot)
- Signal loss/attenuation
- Crosstalk
- Reflections due to impedance mismatches
- EMI within or from outside the components in the system
- Noise from power and distribution networks

HOW ARE SIGNAL AND POWER INTEGRITY LINKED TOGETHER?

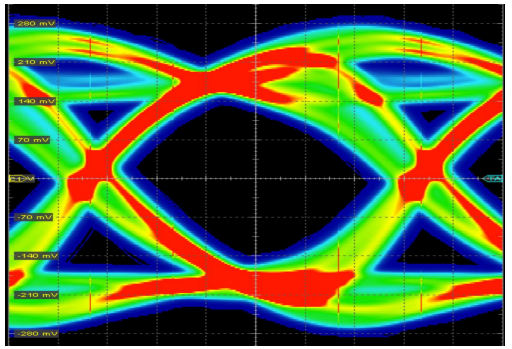


EYE DIAGRAM
INTRODUCTION

- Intuitive graphical tool for the evaluation of the quality and integrity of data signals
- Generated by superposition of multiple signal waveform segments aligned to well-defined reference time instants
  - Waveform segments commonly correspond to a data symbol
  - Reference clock provides timing information for alignment (e.g. symbol start instant)

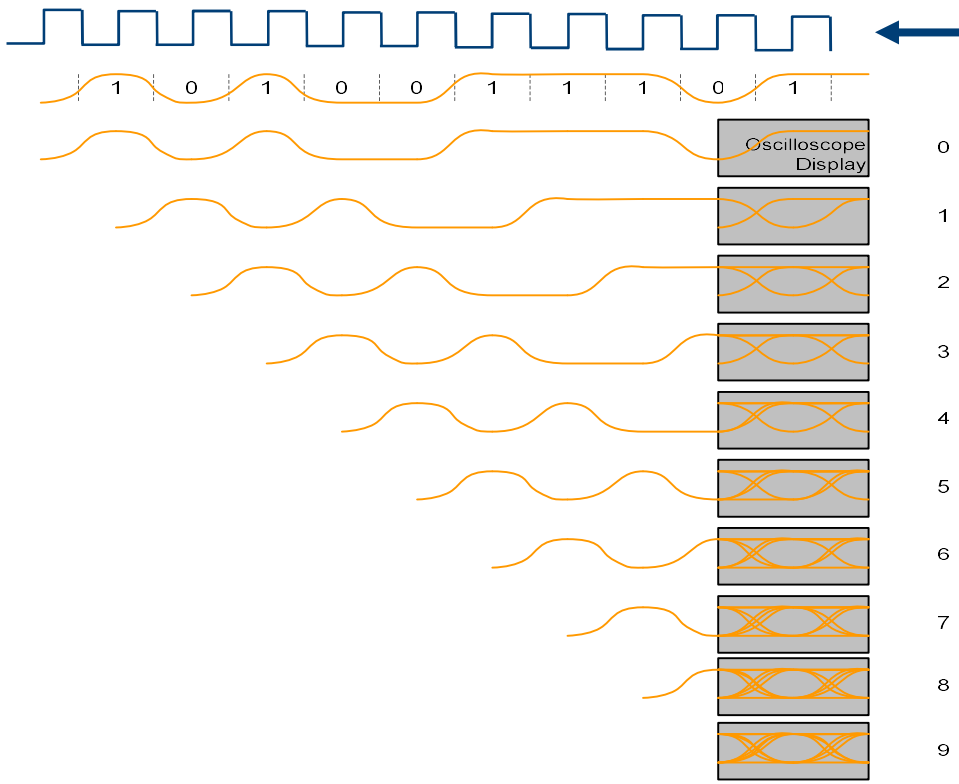


Superposition of bit sequences form the eye diagram



Eye diagram with color-coded frequency

GENERATING EYE DIAGRAMS

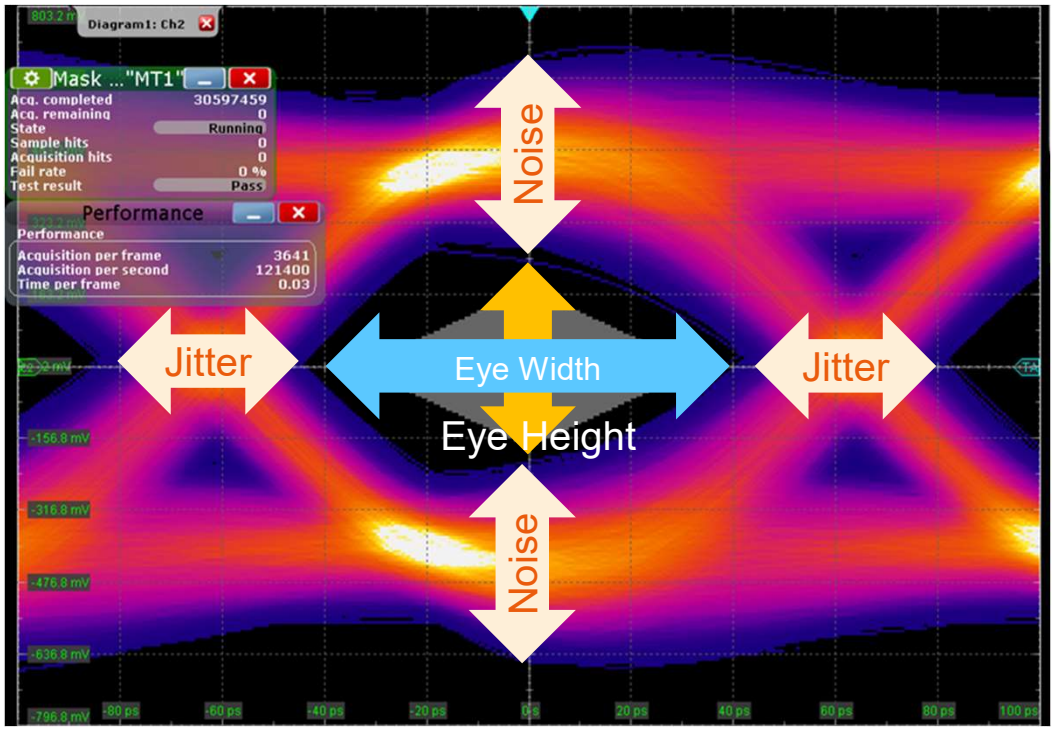


Reference clock
Triggers oscilloscope

Waveform is sampled synchronous with the bit rate of the signal and randomly over time

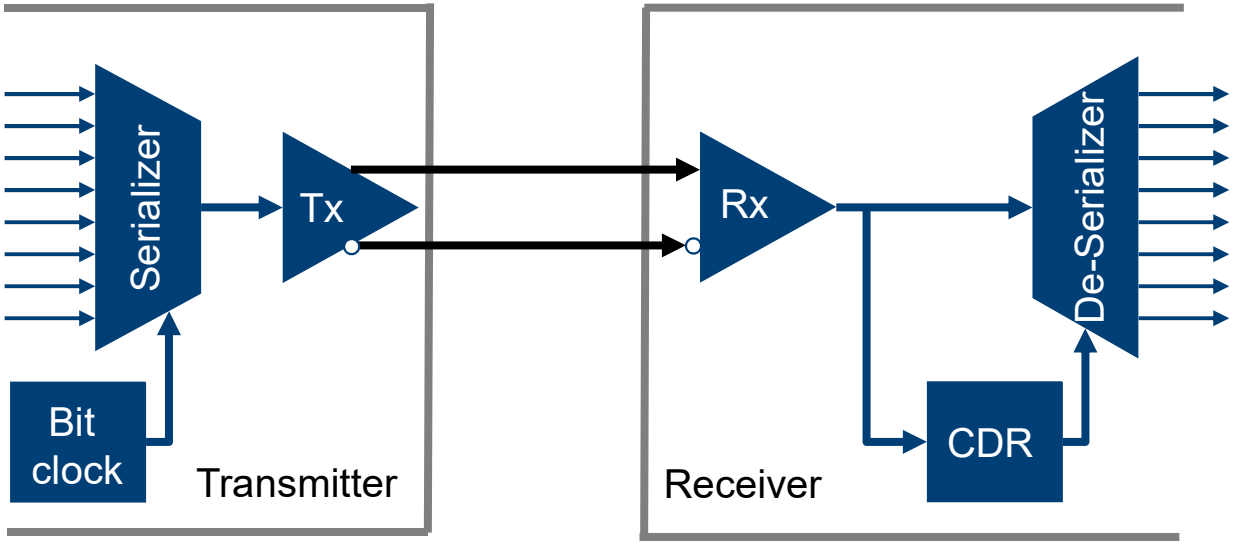
INFORMATION CONTAINED IN AN EYE DIAGRAM

- Timing jitter: peak to peak, standard deviation
- Noise: peak to peak, standard deviation
- Eye width: the minimum time interval over which no signal transition will occur
- Eye height: the minimum amplitude over which the signal level occur
- Eye parameters are based on statistics and require large sample size for repeatable measurements



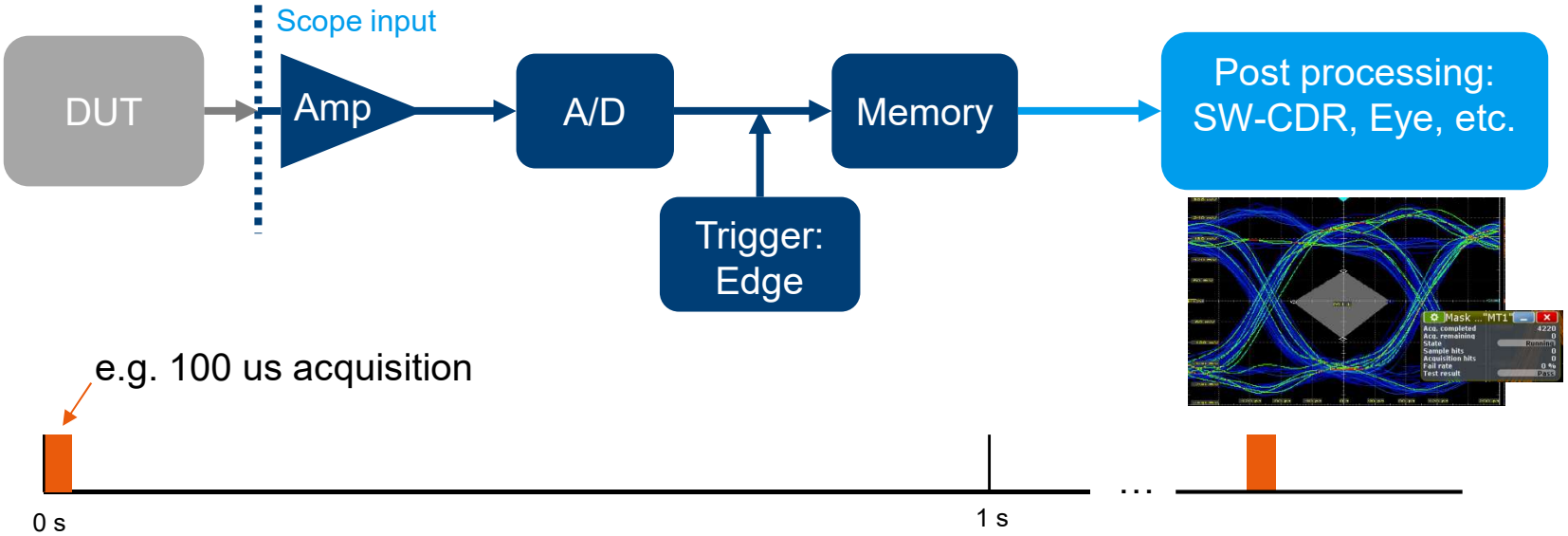
REFERENCE CLOCK GENERATION FOR EYE DIAGRAMS
CLOCK-DATA-RECOVERY

- Timing Reference can be from a reference clock (parallel clock signal) or from the data signal itself (embedded clock signal)
- Clock data recovery is typically uses a Phase Locked Loop (PLL) or Delay Looked Loop (DLL)



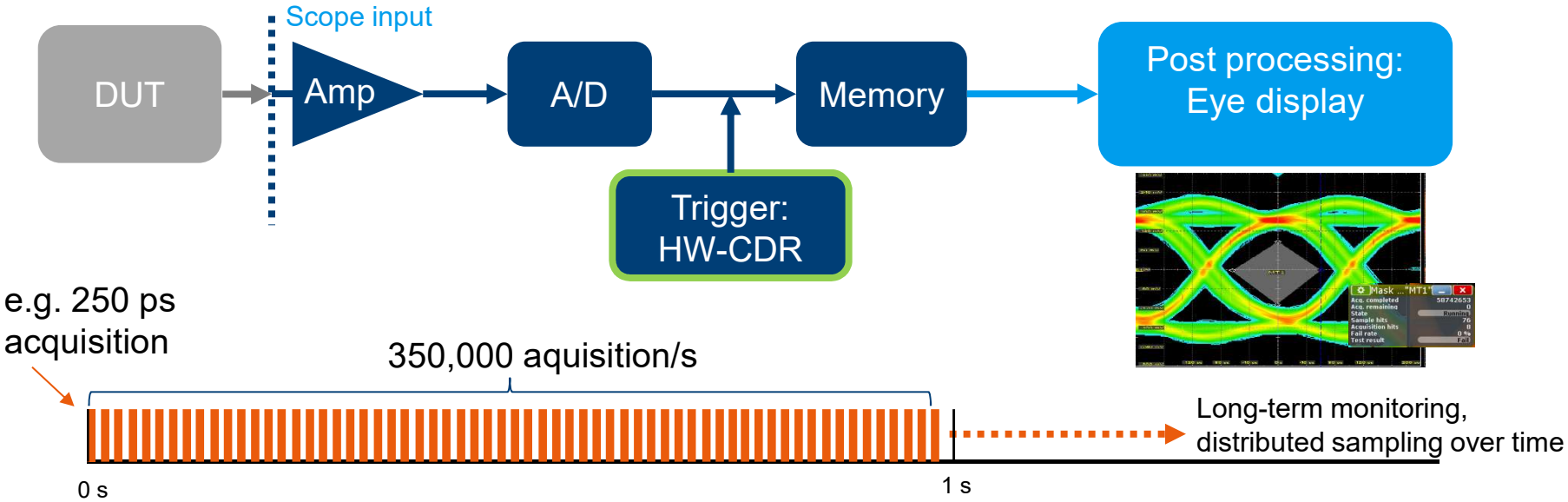
Eye Diagram in Post-Processing

- Analysis based on a single acquisition with long Record length and SW-CDR in post processing
  - Acquired waveform is “folded” over into an eye based on software recovered clock
  - CDR – settling time (typ. >10us) and new synchronization for every new acquisition

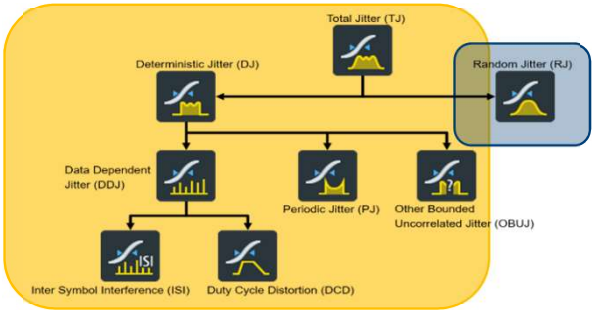


Realtime Eye Diagram

- Analysis based on a multiple acquisition, short Record Length and CDR in Hardware
  - Acquired bits are overlaid to an eye based on HW-CDR timing
  - CDR – looked once and runs continuously



JITTER CAUSES



Data Dependent Jitter

- Transmission Losses
- Circuit Bandwidth
- Frequency dependent Losses
- Dielectric Absorption
- Dispersion – esp. Optical Fiber
- Reflections, Impedance mismatch

Duty Cycle Distortion

- Offset error in receiver or transmitter
- Rise/fall times mismatch

Random Jitter

- Thermal noise
- Shot noise (semiconductor dev)
- External radiation sources
- Oscillator instabilities

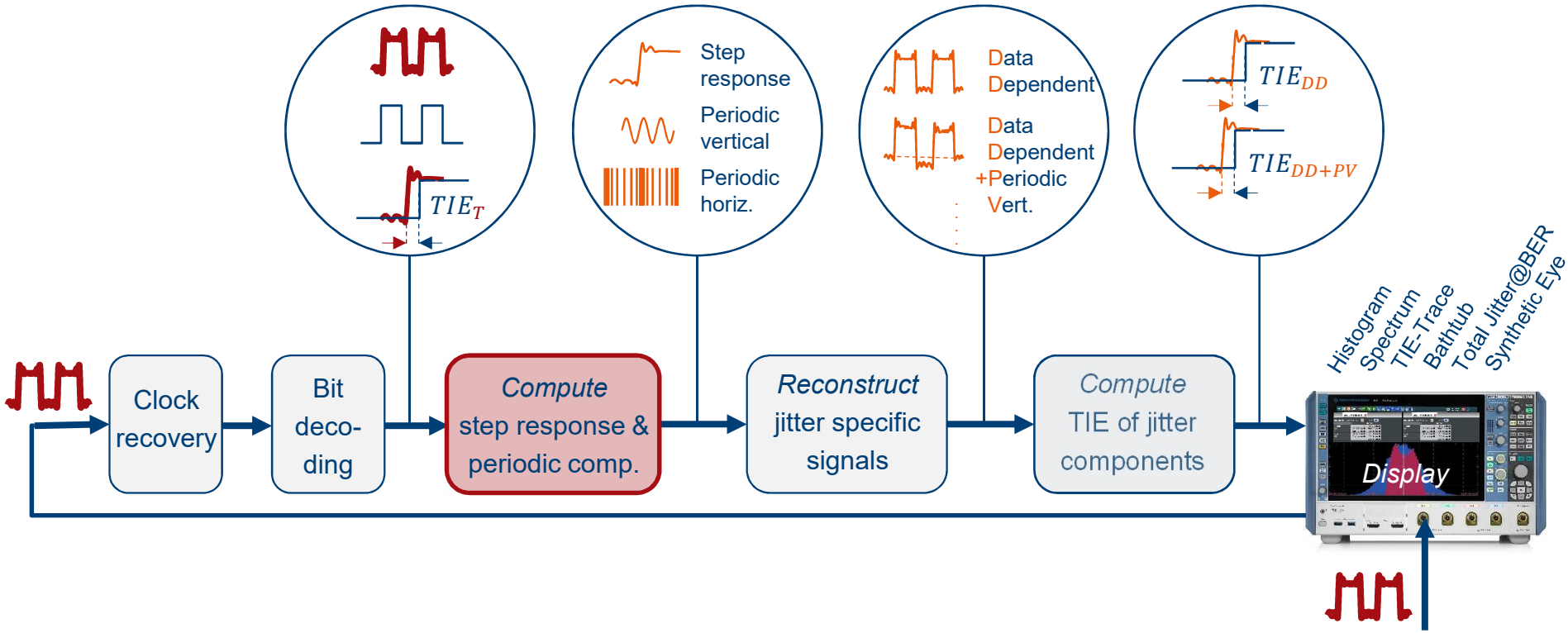
Periodic Jitter

- Injected noise & Circuit instabilities
- SMPS and oscillators plus harmonic content
- PLL's stability problems
- Loop bandwidth (tracking & overshoot)

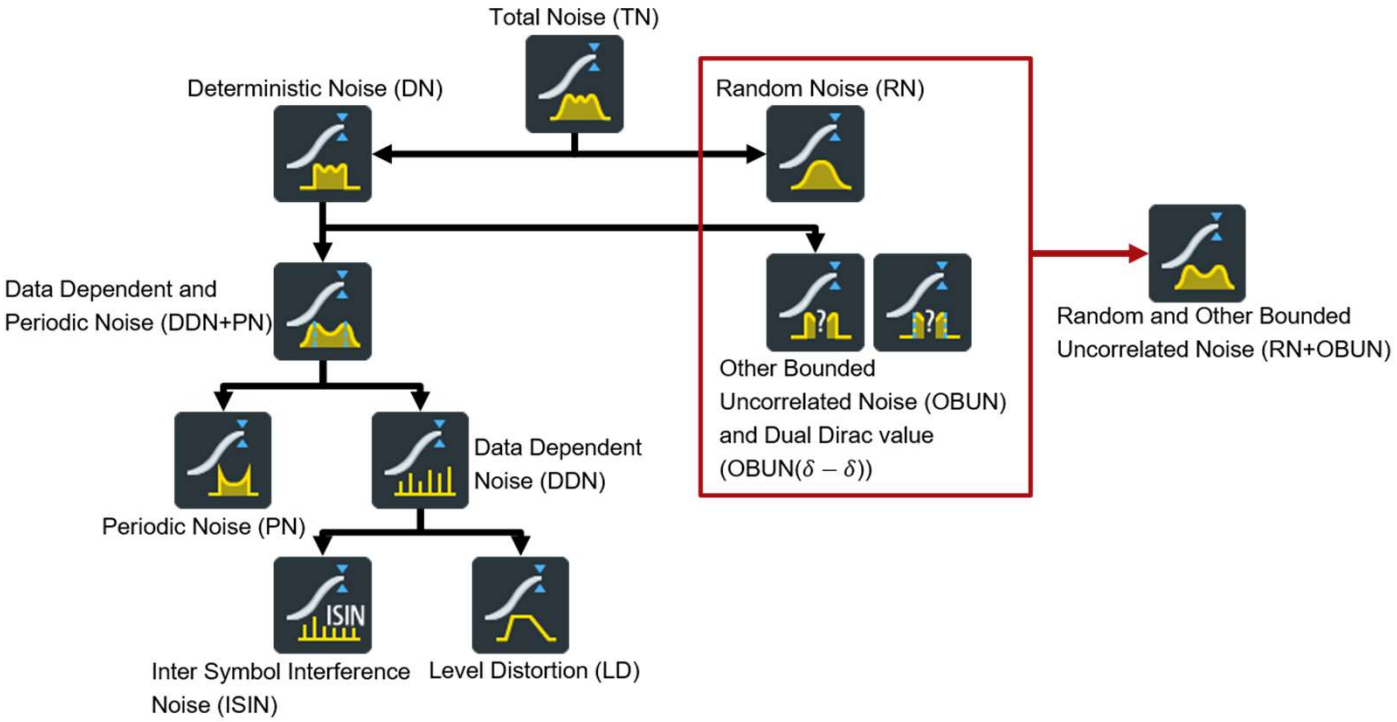
Bounded Uncorrelated Jitter (BUJ)

- X-talk from adjacent lanes (example PCIe*x)
- Appears typically as RJ without spec analysis

R&S ADVANCED JITTER DECOMPOSITION ALGORITHM DETERMINISTIC COMPONENT



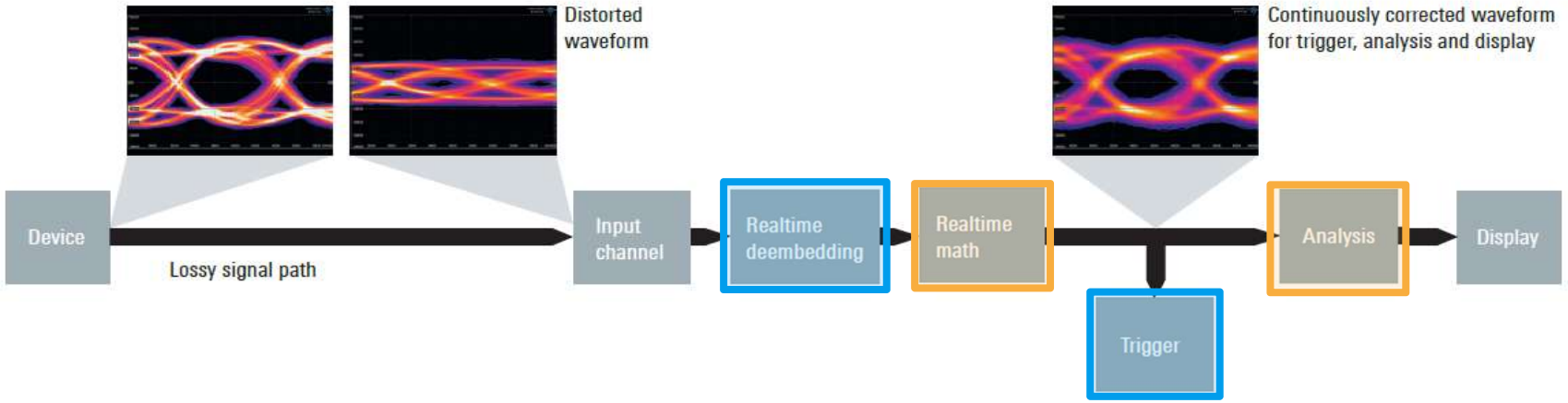
Noise Decomposition



Advanced Jitter Analysis

REALTIME SIGNAL INTEGRITY UP TO 16 GHZ

Realtime Deembedding Architecture



Fast debugging
- ► 20 GSa/s: 750k wfm/s
- ► 40 GSa/s: 300k wfm/s

RT-Deembedding:
- ► Realtime transmission loss compensation

Realtime Math:
- ► V_{Diff} signal
- ► V_{CM} signal

Digital Trigger System:
- ► 16 Gbps Serial Trigger/CDR
- ► 25 ps glitch trigger

HW accelerated analysis:
- ► Mask Test
- ► Histogram

No time consuming post-processing

HOW TO CHECK FOR SI ISSUES?

1) Eye Diagram with high update rate

- Utilizes HW-CDR as Trigger Source and captures up to 400.000 UI/s
- Search for short term events that might corrupt the eye.
- Using Histogramms first analysis on shape and width possible

2) Eye Diagram on long acquistion

- Uses longer acquisition thus longterm stability is investigated.
- SW-CDR is used to slice the acquired data and display the Eye-Diagram
- Comparison of Histograms to step 1) possible.

3) Jitter separation

- If the eye diagram does not give sufficient details Jitter separation can be activated on the same acquired signal.
- Jitter separation unreviels the sources of signal distortions by displaying:
  - Selected Jitter Terms.
  - all major PJ contributors.
  - An calculated step response which represents a channel estimation.

LIVE DEMO

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Make ideas real

THANK YOU
QUESTIONS!

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Make ideas real