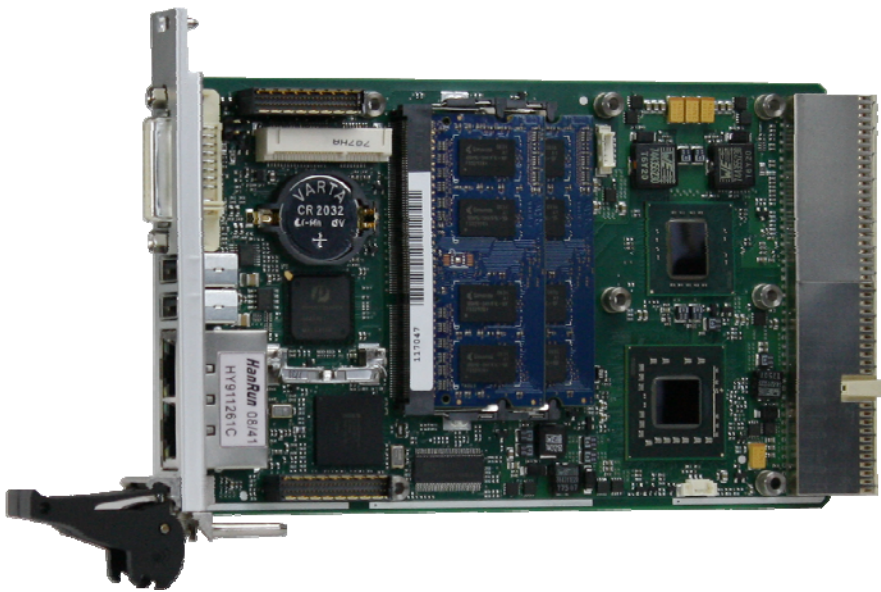


CP75X
3U CompactPCI CPU Board
Hardware Revision 3
User Manual - Version 1.0



Made in Germany
By
EMTrust GmbH

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Preface

Read This First

About this guide This manual describes the 3U CompactPCI CPU Board, its goal is to describe the CP75X, how it works, how to integrate it and how to use it.

Safety First

<p>Danger</p> 	<p>The red Danger sign warns you when a wrong or missing action dramatically endangers your life or health. The used components as well as the peripheral components could be destroyed.</p>
<p>Warning</p> 	<p>The orange Warning sign warns you when a wrong or missing action could seriously harm your health or destroy the used components.</p>
<p>Caution</p> 	<p>The yellow Caution sign warns you when a wrong or missing action could damage the component.</p>

	<p>The yellow ESD sign draws your attention that static-sensitive parts of the component could be destroyed. Unpack shielded components only with ESD protections like an ESD wrist strap.</p>
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The EMTrust Note gives you more information and advice for optimal use of this product.

For example it helps you to purchase necessary or optional accessories.

1 Product Description

In the first chapter you will get a glance of all the integrated features. For further information and a brief description of all the possible changes and extensions please refer to the corresponding chapter.

1.1 General Features

Processor Support

Intel® Core™ 2 Duo

Standard:

SP9300 (2x 2.26 GHz/1066 MHz/6 MB cache/25 W TDP)

Optional:

SL9400 (2x 1.86 GHz/1066 MHz/6 MB cache/17 W TDP)

SU9300 (2x 1.2 GHz/800 MHz/3 MB cache/10 W TDP)

Intel® Celeron® M

Standard:

C723 (1.2 GHz/800 MHz/1 MB cache/10 W TDP)

Optional:

C722 (1.2 GHz/800 MHz/1 MB cache/5.5 W TDP)

Chipset

Mobile Intel® GS45 Express Chipset with Intel® ICH9M

Integrated Bios

SPI-Flash-BIOS using Award BIOS from Phoenix

Ram Support

The Intel® Mobile GS45 Express Chipset supports 800 and 1066 MHz SO-DIMM DDR3 modules. In dual channel mode up to 8GB.

Video Interfaces

Intel Chipset Graphic Media Accelerator Gen. 5

DVI-I

Analog up to QXGA (2048px × 1536px)

Digital up to UXGA (1600px × 1200px)

Ethernet Controller

Intel® 82567 Family Gigabit Ethernet Controller (ETH 1)
Intel® 82574 Family Gigabit Ethernet Controller (ETH 2)
Intel® 82574 Family Gigabit Ethernet Controller (ETH 3)
for Rear I/O (order option)
Intel® 82574 Family Gigabit Ethernet Controller (ETH 4)
only on 8 HP version

USB Support

8 USB ports compliant to USB-Specification 1.1/2.0 with over-current control allocated as

- 2 USB ports on the board provided as 2 single connectors
- 4 USB ports to Board-to-Board connector
- 1 USB port routed to PCI Express Mini Card (self powered)
- 1 USB port routed to Rear I/O (order option)

PCI Express Mini Card socket

PCI Express Mini Card socket with additional SATA and USB 2.0 support.

Bus Support

CompactPCI according to PICMG 2.0 R3.0
Universal (3.3V/5V) PCI VI/O voltage
Rear I/O “E” interface (order option)
Support for 7 PCI REQ/GNT pairs
Supports PCI Rev 2.3 Specification at 33 MHz / 32bit

Storage Support

4 SATA ports with data throughput up to 300MB/s divided into

- 2 SATA ports to Rear I/O (order option)
- 1 SATA port routed to PCI Express Mini Card
- 1 SATA port to Board-to-Board connector

Cooling

4HP version: passive cooled (additional forced air-flow required to comply with specified temperature range)

8HP version: active cooled

Power Supply

Supplied via CompactPCI bus
3.3 V, 5 V and PCI VI/O voltage

1.2 Additional Feature for 8HP Version

The 8HP version uses the Board-to-Board connector to enhance the board capabilities.

3 USB ports compliant to USB-Specification 1.1/2.0 with over-current control for 3 single front connectors

1 SATA port on SATA host receptacle

Intel® 82574 Family Gigabit Ethernet Controller (ETH 4) for Gigabit Ethernet front connector

2 COM ports for 1 single front connector and internal extension header

1 LPT port for internal extension header

PS/2 support*

***Please note:**



For PS/2 support the CP75 needs an appropriate BIOS version with Keyboard Controller Support (KBC-support).

The BIOS version with KBC-support will only boot-up with a present Keyboard Controller. Please ensure for a successful boot-up that the Extension Board of 8HP variant or the Rear I/O module is connected.

1.3 Additional Feature for Versions with Rear I/O

The Rear I/O “E” interface is an order option for the 4HP and 8HP version.

1 USB port compliant to USB-Specification 1.1/2.0 with over-current control for Rear I/O module

2 SATA ports for Rear I/O module

Intel® 82574 Family Gigabit Ethernet Controller (ETH 3) for Gigabit Ethernet connector on Rear I/O module

Analog VGA (shared with front-panel VGA)

PS/2 support via Rear I/O module*

***Please note:**



For PS/2 support the CP75 needs an appropriate BIOS version with Keyboard Controller Support (KBC-support).

The BIOS version with KBC-support will only boot-up with a present Keyboard Controller. Please ensure for a successful boot-up that the Extension Board of 8HP variant or the Rear I/O module is connected.

1.4 Mechanical Dimensions

Size

213 mm × 129 mm overall

Max. Height

4HP: 20.32 mm

8HP: 40.64 mm

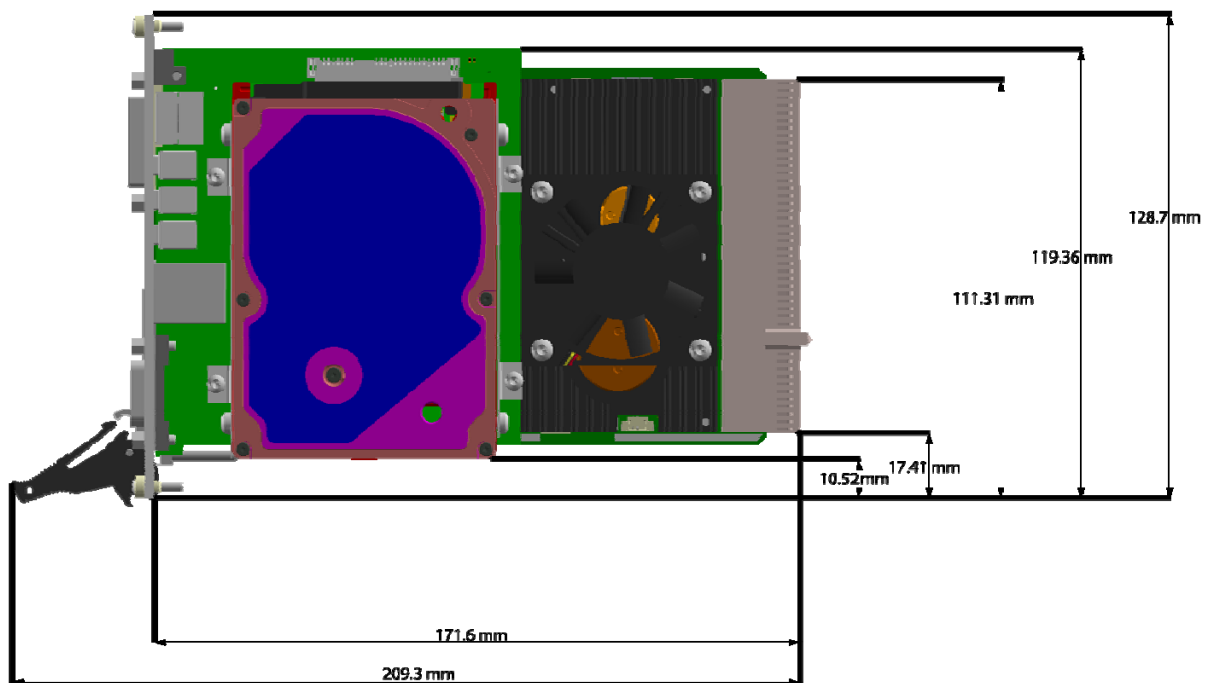


Fig. 1:Dimensions of CPU Board

1.5 Environmental Specification

Max. Operating Temperature

0°C to 55°C ambient or

0°C to 70°C at any point on the modules surface with adequate airflow



Other Operating Temperature Ranges upon request

Max. Storage Temperature

-20°C to +100°C

Max. Humidity


Non-condensing

Working 80% / Storage 95%

2 Assembly

The sockets and connectors you can use to build up our system are specified in chapter 4.

The needs of your peripheral hardware can be fitted by the BIOS Configuration described in chapter 5.

<p>CAUTION</p> 	<p>Please note to prevent loss of warranty:</p> <p>Do not remove the Heatsink, the 8HP daughter board or break any seal.</p>
---	--

4HP Front View

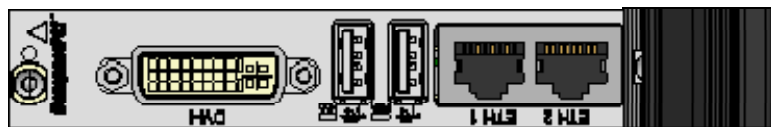


Fig. 2:4HP Front View

4HP Top View

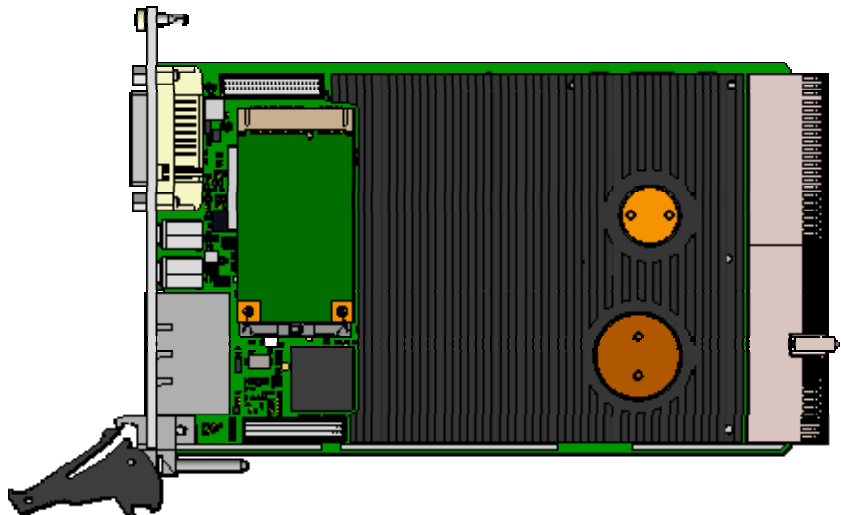


Fig. 3:4HP Top View

4HP Side View



Fig. 4:4HP Side View

4HP Rear View



Fig. 5:4HP Rear View

4HP Bottom View

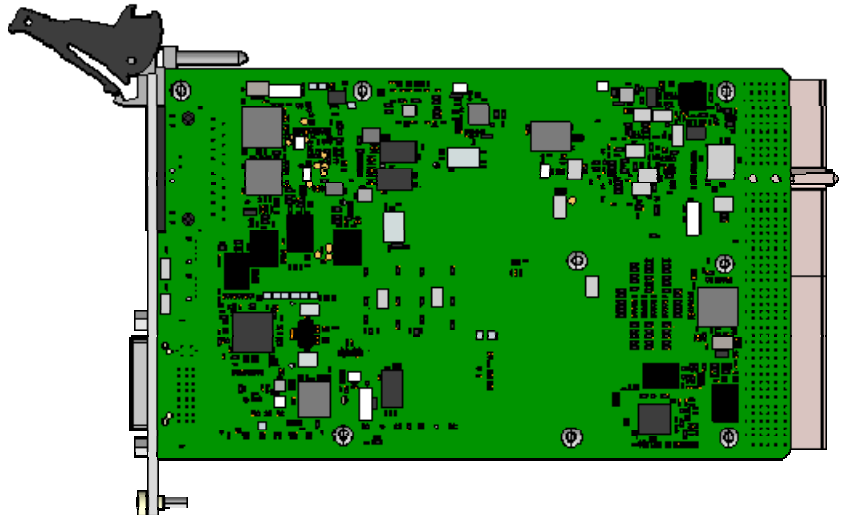


Fig. 6:4HP Bottom View

8HP Front View

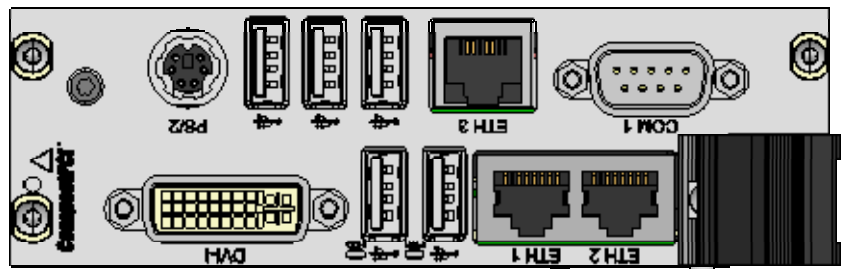


Fig. 7:8HP Front View

8HP Top View

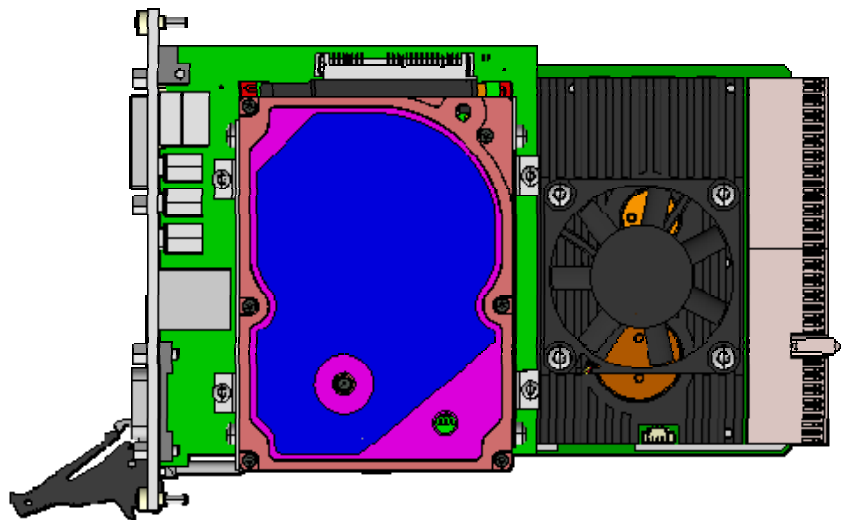


Fig. 8:8HP Top View

8HP Side View



Fig. 9:8HP Side View

8HP Rear View

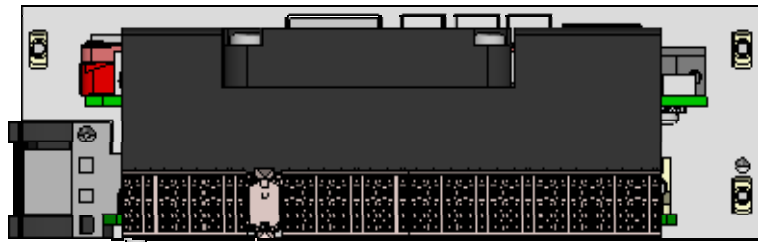


Fig. 10:8HP Rear View

8HP Bottom View

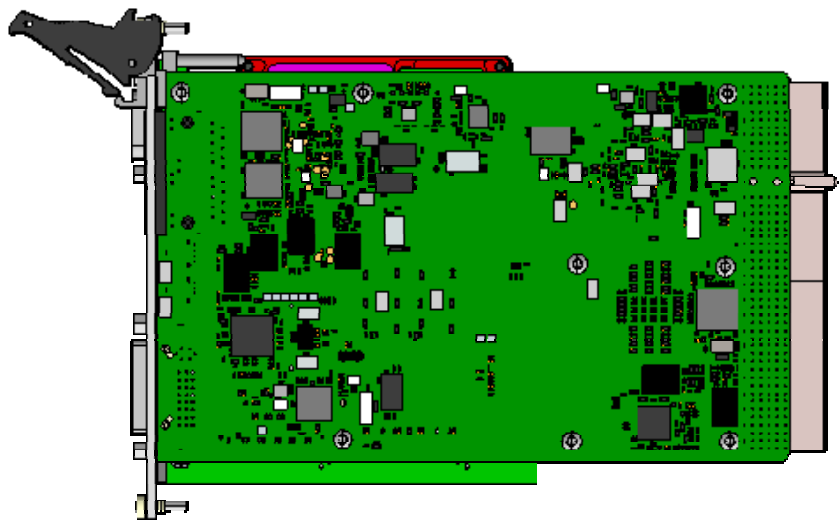


Fig. 11:8HP Bottom View

2.1 Mechanical Mounting

For further information please consult the PICMG CompactPCI Specifications.



Please use only 3U System Slots (marked with the triangle and red guide rails).

The CPU board should slide smooth into the housing.

Rear I/O functionality is only appropriate with a suitable Backplane.

CAUTION



Please power off system before installing or replacing of the CPU board.

Assembly: First slide CPU board in the System Slot and pull the In/Ejector handle upwards.

Then tighten the screw according to the position numbers.

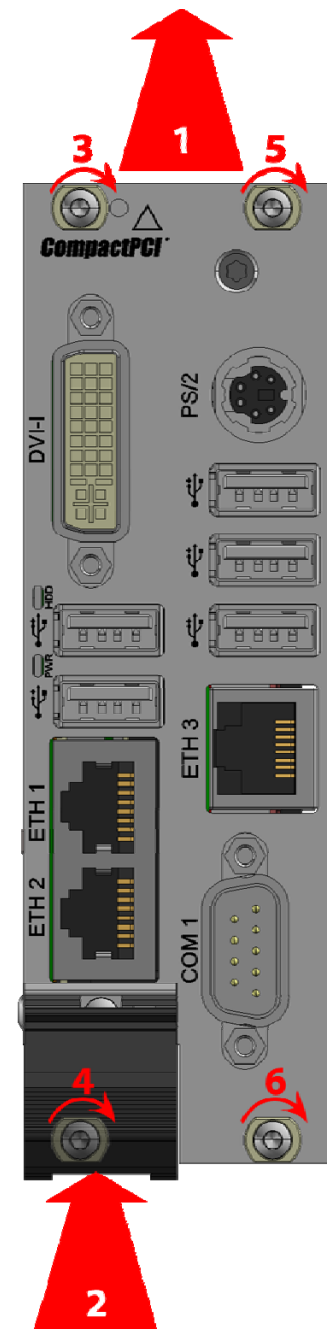


Fig. 12: Insert CPU Board

Release: First loosen the screw according to the position numbers.

Then press the In/Ejector handle down and the CPU board will be released automatically.

Remove the board from the System Slot.

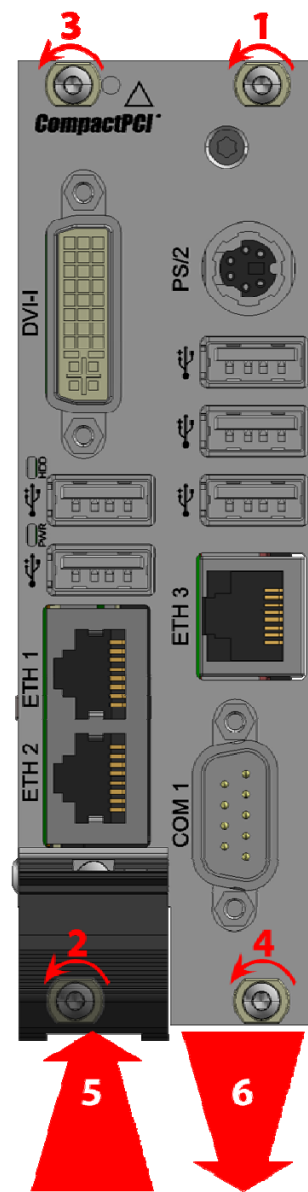


Fig. 13: Remove CPU Board

3 Sockets, Jumper and Features of 4HP Version

The following schedule contains all the necessary information to integrate the CPU board into your system housing.

On the left side of the page you will see the position on the board (red mark) and on the right side a magnified image of the explained item.

The explanation supplies you with general information, electrical specifications and a pin allocation table.

3.1 DVI-I Connector

The DVI-I delivers analog and digital signals.

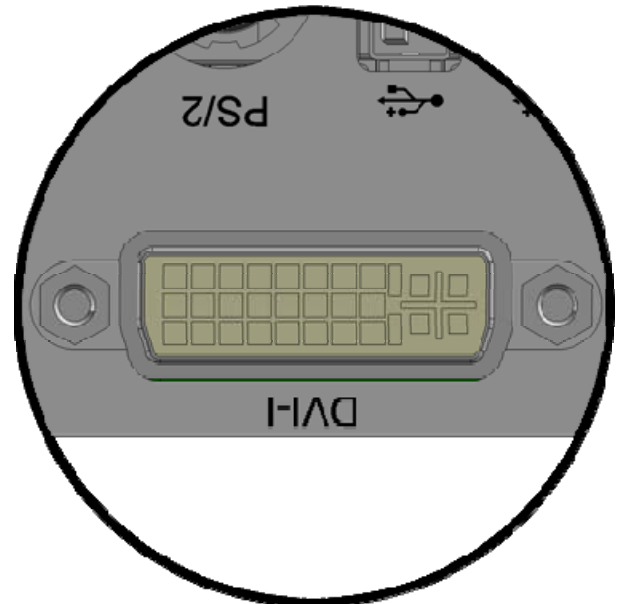
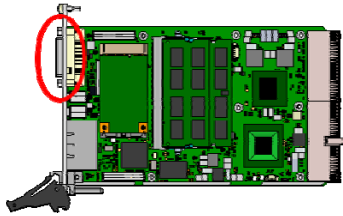


Fig. 14: DVI-I Detail

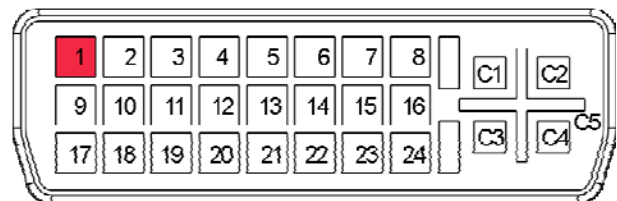


Fig. 15: DVI-I Schematic

Pin	DVI Signal
1	TX2-
2	TX2+
3	GND
4	NC
5	NC
6	DDC-CLK
7	DDC-DATA
8	VSYNC
9	TX1-
10	TX1+
11	GND
12	NC
13	NC
14	5V (Fuse)

15	GND
16	HOTPLUG
17	TX0-
18	TX0+
19	GND
20	NC
21	NC
22	GND
23	CLK+
24	CLK-
C1	RED
C2	GREEN
C3	BLUE
C4	HSYNC
C5	GND

Tab. 1:DVI-I

**Note: DDC-CLK and DDC-DATA should be connected to DVI-Displays only.
VGA monitors are not connect to DDC-CLK or DDC-DATA!**

3.2 System LEDs

The System LEDs show the system status and the HDD activity.

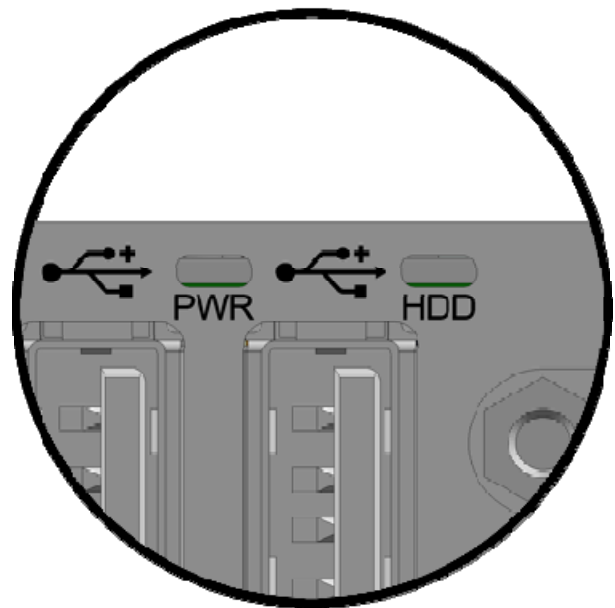
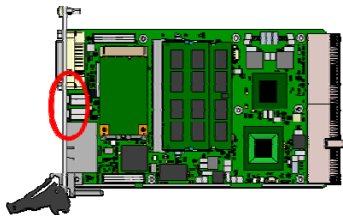


Fig. 16: System LEDs Detail

PWR	Green	Red
Off	CP75X off	No Error
On	CP75X on	Error

Tab. 2: PWR LED

HDD	Green
Off	No Serial ATA drive activity
Blink	At least one drive active
On	Heavy drive activity

Tab. 3: HDD LED

3.3 USB Sockets

The USB Sockets are compliant to the USB 1.1 and USB 2.0 specification.

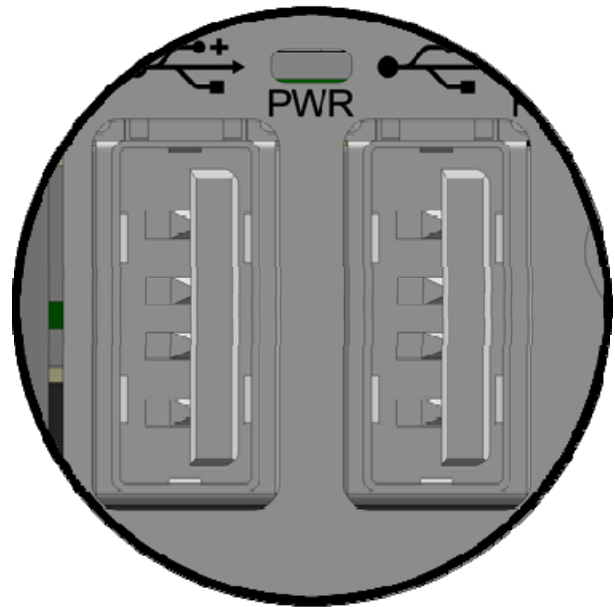
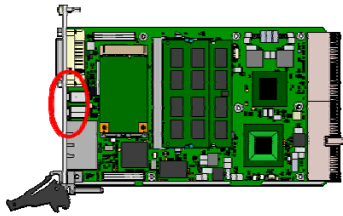


Fig. 17:USB Sockets Detail

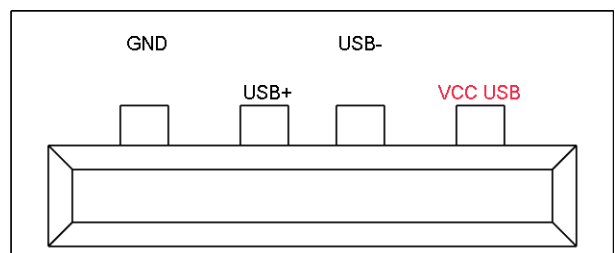


Fig. 18:USB Socket Schematic

3.4 Ethernet Sockets

Ethernet socket ETH1 is connected to an Intel 82567LM Gigabit Ethernet Controller.

Ethernet socket ETH2 is connected to an Intel 82574IT Gigabit Ethernet Controller.

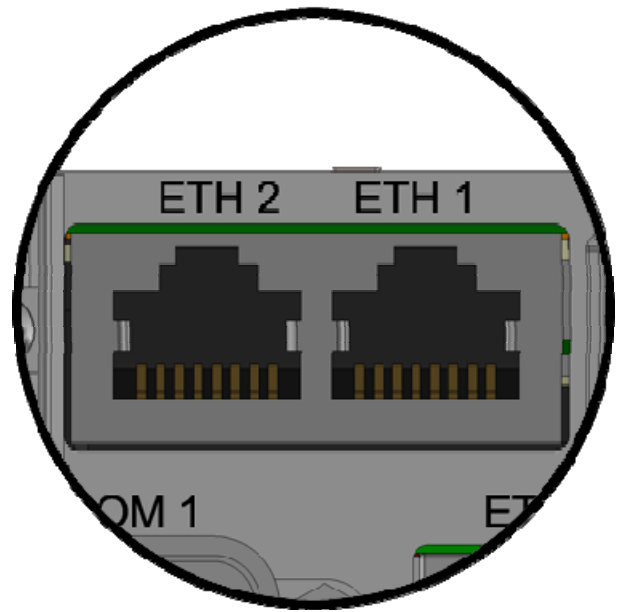
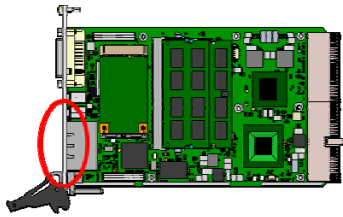


Fig. 19: Ethernet Sockets Detail

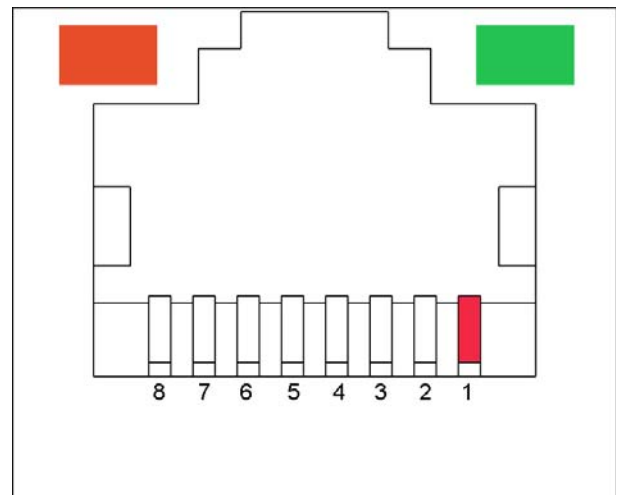


Fig. 20: Ethernet Socket Schematic

Pin	Signal
1	TXD0+
2	TXD0-
3	TXD1+
4	TXD2+
5	TXD2-

6	TXD1-
7	TXD3+
8	TXD3-

Tab. 4:Ethernet

Orange LED

Speed LED is on during 1 Gbit transmission and switched off during 10 / 100 Mbit transmission.

Green LED

Link / Activity LED is permanently on to indicate that there is an active connection on the Ethernet port. LED flashes during communication with Ethernet networks.

3.5 Battery Socket

The battery buffers the Real Time Clock and the BIOS settings.

WARNING



DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED.

Use only Lithium cells CR2032.

Assure right polarity according to the figure 32 below.

For proper function of the board change the battery every five years.

CAUTION



Please note to prevent loss of warranty:

Do not remove the Heatsink, the 8HP daughter board or break any seal.

For the battery replacement use RMA procedure.

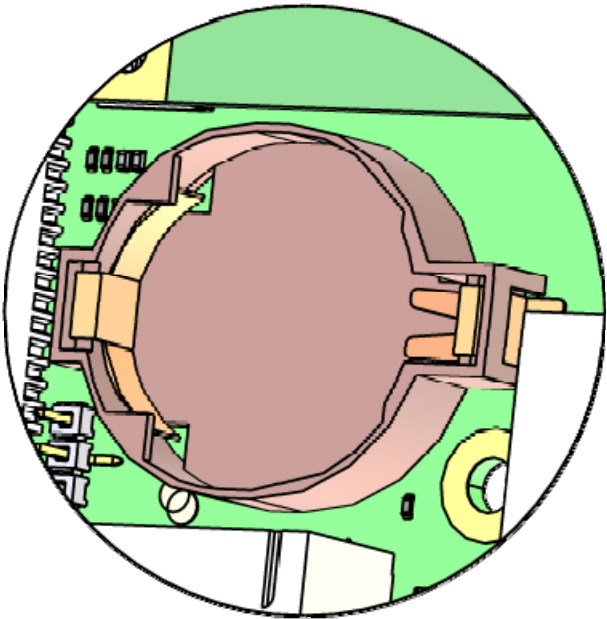
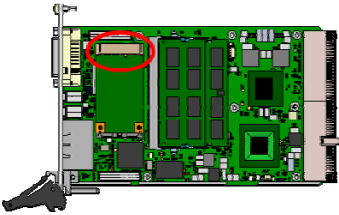


Fig. 21:Battery Socket Detail

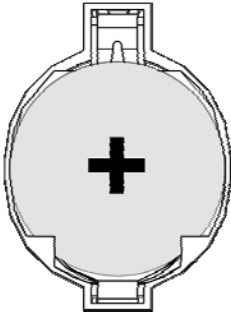


Fig. 22:Battery Socket Schematic

3.6 PCI Express Mini Card Socket

As default one PCI Express lane, a USB port and a SATA port are routed to the Mini Card Socket.

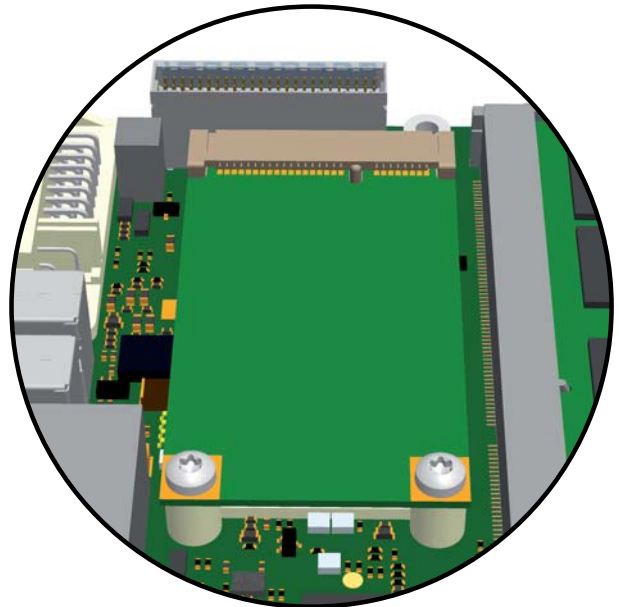
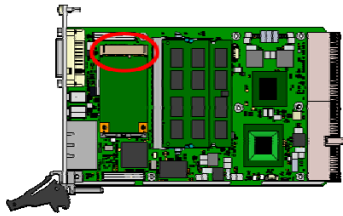


Fig. 23:PCI Express Mini Card Socket Detail

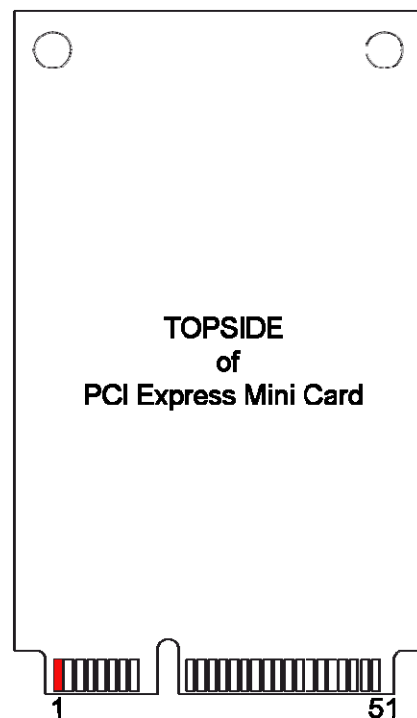


Fig. 24:PCI Express Mini Card Socket Schematic

CAUTION

Never insert PCI Express Mini Cards which connect 3.3V with 3.3Vaux.

This may damage the CPU Board.

CAUTION

Never insert PCI Express Mini Cards where Pin´s 39, 41, 47 or 49 are connected. These pin´s must be unconnected. If you need to use a PCI Express Mini Card where these pin´s are connected, please contact EMTrust for further instructions.

This may damage the CPU Board.



EMTrust recommends M2.5 Torx Screws with a screw locking and a maximum tightening torque of 0.5 Nm.

Assembly: First slide Mini Card in the socket.

Then press the card in direction to the board.

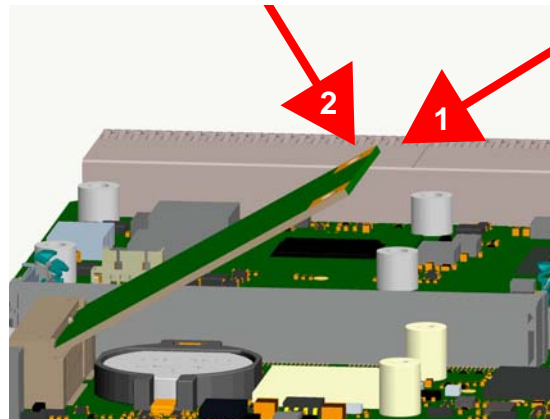


Fig. 25: Insert PCI Express Mini Card

Then tighten the screw according to the position numbers.

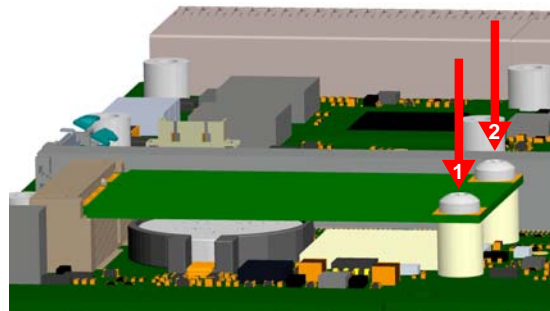


Fig. 26: Remove PCI Express Mini Card

Release: First remove both screws (1/2).

Then the Mini Card will set upright automatically (3).

Remove the card form the socket.

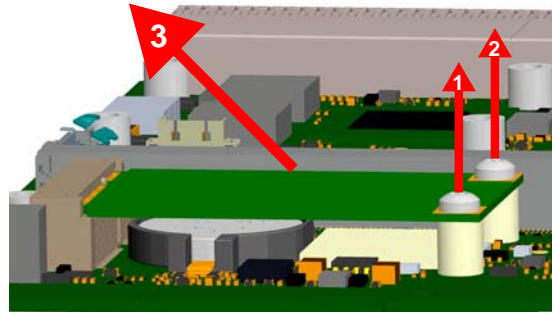


Fig. 27: Remove PCI Express Mini Card

Pin	Signal
1	WAKE#
2	3.3V
3	N.C.
4	GND
5	N.C.
6	1.5V
7	CLKREQ#
8	N.C.
9	GND
10	N.C.
11	PCIE_CLK_0-
12	N.C.
13	PCIE_CLK_0+
14	N.C.
15	GND
16	N.C.
17	N.C.

18	GND
19	N.C.
20	Reserved
21	GND
22	PERST#
23	PCIE3_RX-
24	3.3Vaux
25	PCIE3_RX+
26	GND
27	GND
28	1.5V
29	GND
30	SMB_CLK
31	PCIE3_TX-
32	SMB_DATA
33	PCIE3_TX+
34	GND
35	GND
36	USB_D-*
37	GND*
38	USB_D+*
39	SATA_RXN1*
40	GND
41	SATA_RXP1*
42	N.C.
43	GND*
44	N.C.
45	GND*
46	N.C.
47	SATA_TXN1*
48	1.5V
49	SATA_TXP1*
50	GND
51	GND*
52	3.3V

Tab. 5:PCI Express Mini Card Socket

* **Additional signals divergent to the
PCI Express Mini Card specification.**

3.7 CompactPCI System Connector

The pin assignment of the CompactPCI System connector without Rear I/O feature.

The System connector consists of two single connectors J1 and J2.



The CP75X does not support the following signals:

TCK, TMS, TRST#, TDO, TDI, INTP, INTS,
IPMB_PWR, REQ64#, ENUM#, ACK64#, M66EN and
HEALTHY#

3.7.1 System Connector J1

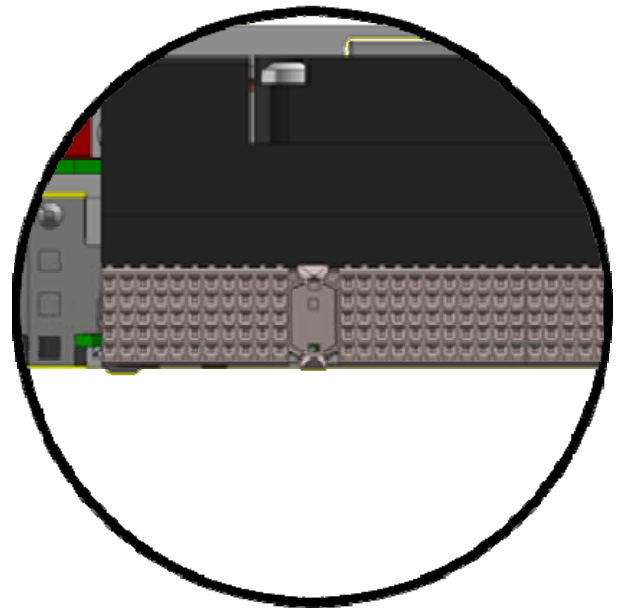
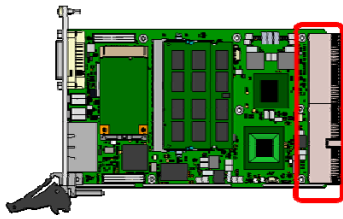


Fig. 28:J1 Detail

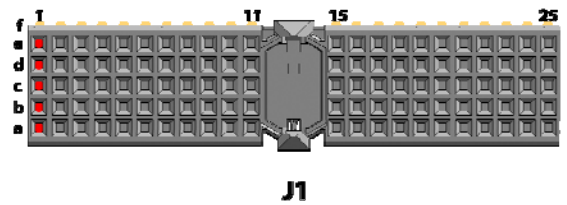


Fig. 29:J1 Schematic

Pin	Row A	Row B	Row C	Row D	Row E	Row F
J1-25	+5V	REQ64#	ENUM#	+3.3V	+5V	Shield
J1-24	AD[1]	+5V	V(I/O)	AD[0]	ACK64#	Shield
J1-23	+3.3V	AD[4]	AD[3]	+5V	AD[2]	Shield
J1-22	AD[7]	GND	+3.3V	AD[6]	AD[5]	Shield
J1-21	+3.3V	AD[9]	AD[8]	M66EN	C / BE[0]#	Shield
J1-20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	Shield
J1-19	+3.3V	AD[15]	AD[14]	GND	AD[13]	Shield
J1-18	SERR#	GND	+3.3V	PAR	C / BE[1]#	Shield
J1-17	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	Shield
J1-16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	Shield
J1-15	+3.3V	FRAME#	IRDY#	GND	TRDY#	Shield
J1-14	KEY AREA					
J1-13						
J1-12						
J1-11	AD[18]	AD[17]	AD[16]	GND	C / BE[2]#	Shield
J1-10	AD[21]	GND	+3.3V	AD[20]	AD[19]	Shield
J1-09	C / BE[3]	GND	AD[23]	GND	AD[22]	Shield
J1-08	AD[26]	GND	V(I/O)	AD[25]	AD[24]	Shield
J1-07	AD[30]	AD[29]	AD[28]	GND	AD[27]	Shield
J1-06	REQ0#	GND	+3.3V	CLK0	AD[31]	Shield
J1-05	NC	NC	RST#	GND	GNT0#	Shield
J1-04	NC	NC	V(I/O)	INTP	INTS	Shield
J1-03	INTA#	INTB#	INTC#	+5V	INTD#	Shield
J1-02	TCK	+5V	TMS	TDO	TDI	Shield
J1-01	+5V	-12V	TRST#	+12V	+5V	Shield

Tab. 6:J1

3.7.2 System Connector J2

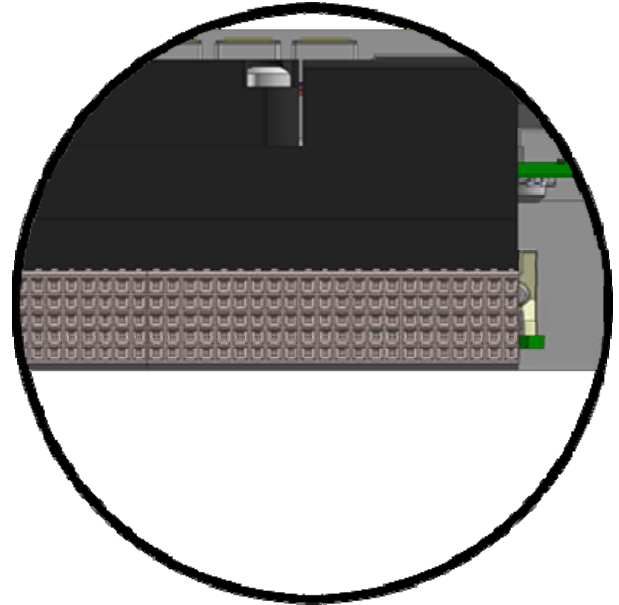
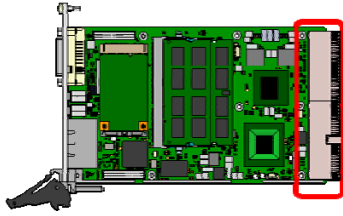
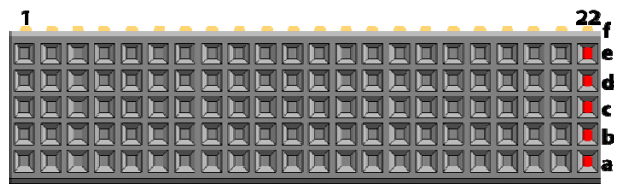


Fig. 30:J2 Detail



J2

Fig. 31:J2 Schematic

Pin	Row A	Row	Row C	Row D	Row E	Row F
J2-22	(GA4)	(GA3)	(GA2)	(GA1)	(GA0)	Shield
J2-21	CLK6	GND	N.C.*	N.C.*	N.C.*	Shield
J2-20	CLK5	GND	N.C.*	GND	N.C.*	Shield
J2-19	GND	GND	N.C.*	N.C.*	N.C.*	Shield
J2-18	N.C.*	N.C.*	N.C.*	GND	N.C.*	Shield
J2-17	N.C.*	GND	PRST_m	REQ6_m	GNT6_m	Shield
J2-16	N.C.*	N.C.*	DEG_m	GND	N.C.*	Shield
J2-15	N.C.*	GND	FAL_m	REQ5_m	GNT5_m	Shield
J2-14	N.C.*	N.C.*	N.C.*	GND	N.C.*	Shield
J2-13	N.C.*	GND	V(I/O)	N.C.*	N.C.*	Shield
J2-12	+3V3SB	N.C.*	N.C.*	GND	+5V	Shield
J2-11	N.C.*	GND	V(I/O)	N.C.*	N.C.*	Shield
J2-10	N.C.*	N.C.*	N.C.*	GND	+5V	Shield
J2-09	N.C.*	GND	V(I/O)	N.C.*	N.C.*	Shield
J2-08	N.C.*	N.C.*	N.C.*	GND	+3V3	Shield
J2-07	N.C.*	GND	V(I/O)	N.C.*	N.C.*	Shield
J2-06	N.C.*	N.C.*	N.C.*	GND	N.C.*	Shield
J2-05	N.C.*	GND	V(I/O)	N.C.*	N.C.*	Shield
J2-04	V(I/O)	N.C.*	N.C.*	GND	N.C.*	Shield
J2-03	CLK4	GND	GNT3_m	REQ4_m	GNT4_m	Shield
J2-02	CLK2	CLK3	SYSEN_m	GNT2_m	REQ3_m	Shield
J2-01	CLK1	GND	REQ1_m	GNT1_m	REQ2_m	Shield

Tab. 7:J2 without Rear I/O

* Not connected in Non-Rear I/O versions



For more information about the additional signals of the Rear I/O versions, please contact EMTrust sales department.

4 Additional Features of 8HP Version

This chapter describes the additional features of the 8HP version.

4.1 Internal Extension Header COM2 (8HP)

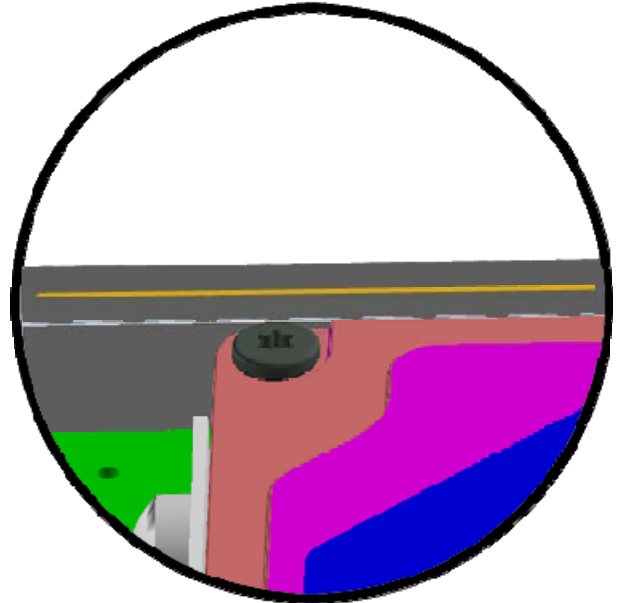
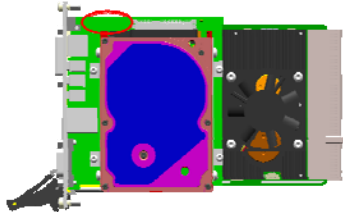


Fig. 32: Internal Extension Header Detail



Fig. 33: Internal Extension Header Schematic

Pin	Signal
1	DCD
2	DSR
3	RxD
4	RTS
5	TxD
6	CTS
7	DTR
8	RI
9	+5V
10	GND
11	LPT_AFD_m
12	LPT_INIT_m
13	LPT_SLIN_m
14	LPT_STB_m
15	LPT_BUSY

16	LPT_ACK_m
17	LPT_PE
18	LPT_SLCT
19	LPT_ERR_m
20	LPT_PD0
21	LPT_PD1
22	LPT_PD2
23	LPT_PD3
24	LPT_PD4
25	LPT_PD5
26	LPT_PD6
27	LPT_PD7

Tab. 8: Internal Extension Header



It is recommended to use the IPS-PPE12-C.

4.2 PS/2 Connector (8HP)

The PS/2 connector for mouse and keyboard.

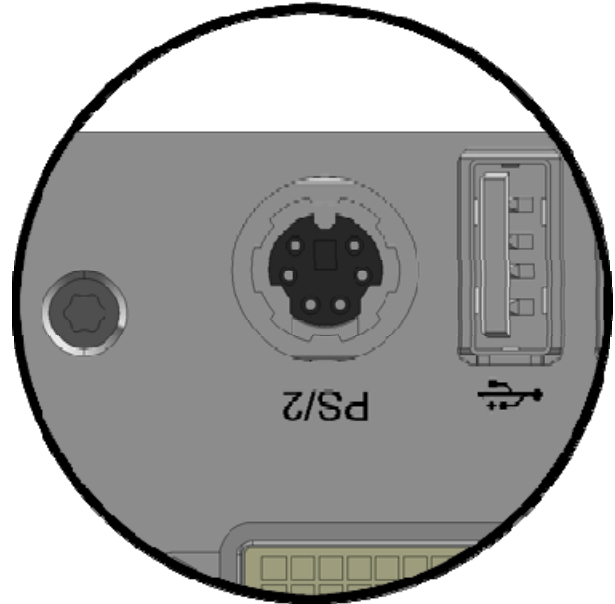
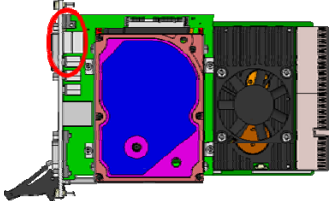


Fig. 34:PS/2 Detail

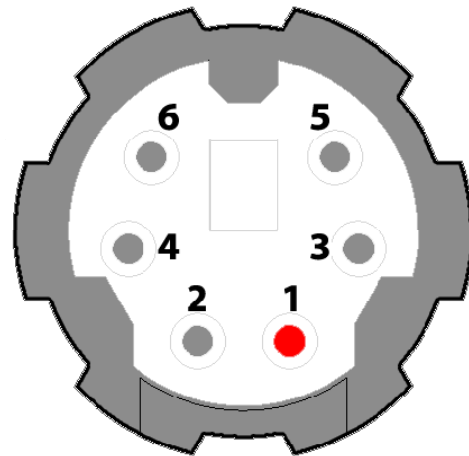


Fig. 35:PS/2 Schematic

Pin	Signal
1	KBDATA
2	MSDATA
3	GND
4	VCC_KB
5	KBCLK
6	MSCLK

Tab. 9:PS/2



***Please note:**

For PS/2 support the CP75 needs an appropriate BIOS version with Keyboard Controller Support (KBC-support).

4.3 USB Sockets II (8HP)

The USB Sockets are compliant to the USB 1.1 and USB 2.0 specification.

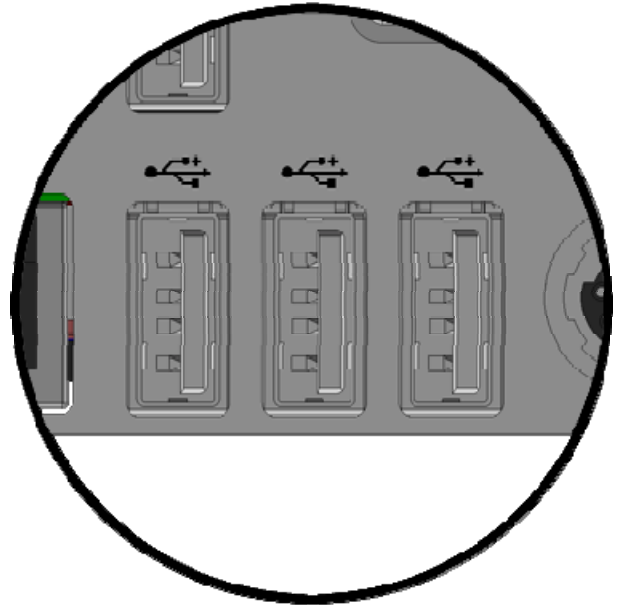
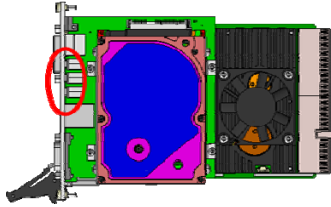


Fig. 36:USB Socket 8HP Detail

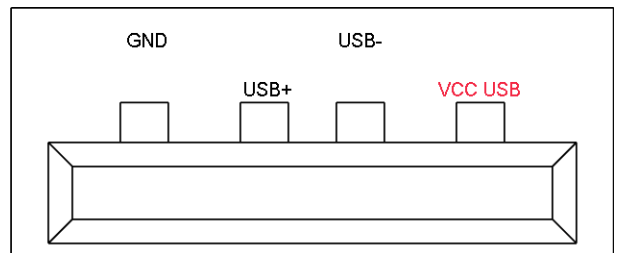


Fig. 37:USB Socket Detail

4.4 Ethernet Socket (8HP)

The Ethernet socket ETH3 uses a Gigabit Ethernet Controller Intel 82574IT.

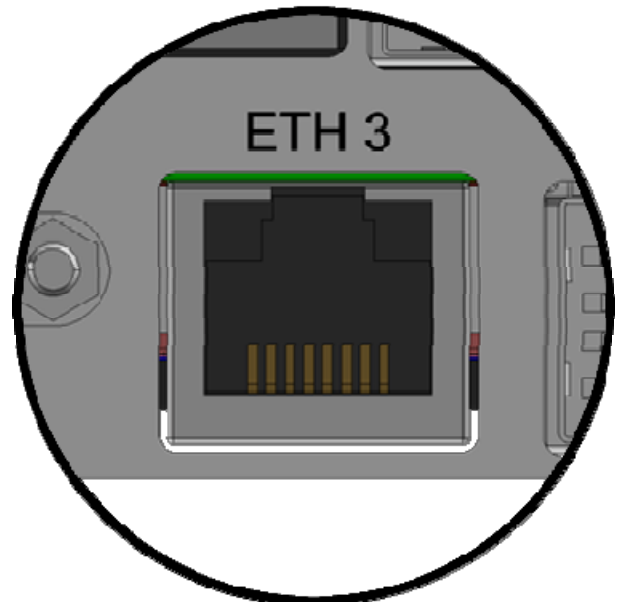
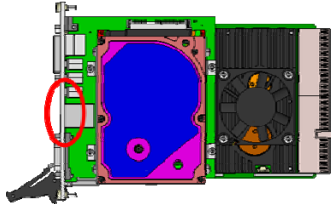


Fig. 38: Ethernet Socket 8HP Detail

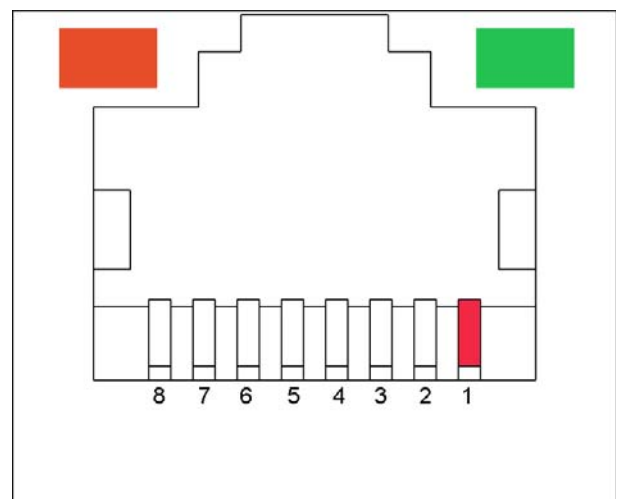


Fig. 39: Ethernet Socket Schematic

Orange LED

Speed LED is on during 1 Gbit transmission and switched off during 10 / 100 Mbit transmission.

Green LED

Link / Activity LED is permanently on to indicate that there is an active connection on the Ethernet port. LED flashes during communication with Ethernet networks.

Pin	Signal
1	TXD0+
2	TXD0-
3	TXD1+
4	TXD2+
5	TXD2-
6	TXD1-
7	TXD3+
8	TXD3-

Tab. 10: Ethernet Socket

4.5 COM1 Connector (8HP)

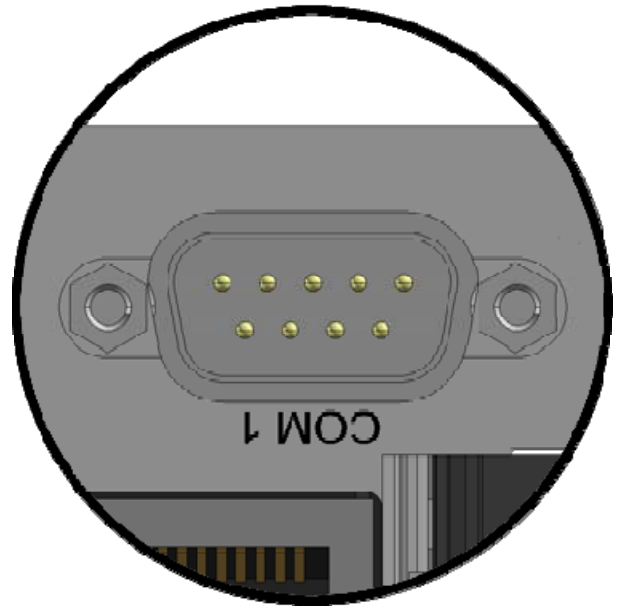
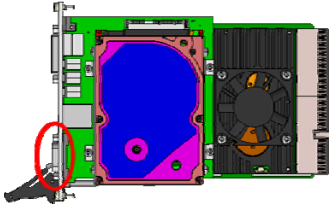


Fig. 40:COM1 Connector 8HP Detail

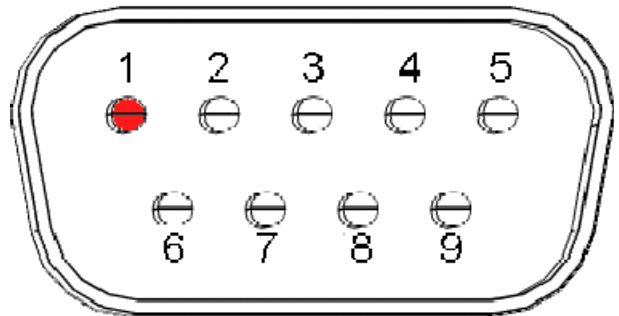


Fig. 41:COM Connector Schematic

Pin	Signal
1	DCD
2	RxD
3	TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

Tab. 11:COM

4.6 SATA Host Receptacle (8HP)

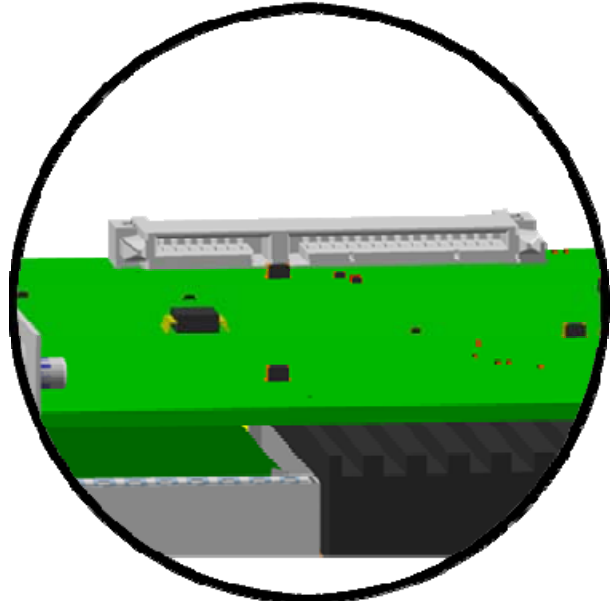
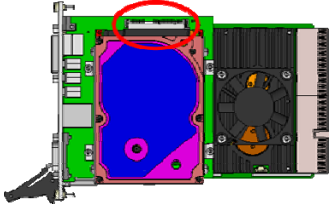


Fig. 42: SATA Host Receptacle Detail




Fig. 43: SATA Host Receptacle Schematic

Pin	Signal
1	GND
2	DATATX0+
3	DATA0TX0-
4	GND
5	DATARX0-
6	DATARX0+
7	GND
11	3.3V
12	3.3V
13	3.3V
14	GND
15	GND
16	GND
17	5V
18	5V
19	5V

20	GND
21	Staggered Spin-up/Activity LED
22	GND
23	12V
24	12V
25	12V

Tab. 12:SATA Host Receptacle

CAUTION



EMTrust recommends M3x4 Torx Screws with a screw locking and a maximum tightening torque of 0.5 Nm.

Please ensure that the bottom side of the hard disk is electrically insulated.

In order to insulate the bottom side of the hard disk use only non-electrostatic foil.

Assembly: First preassemble the HDD.

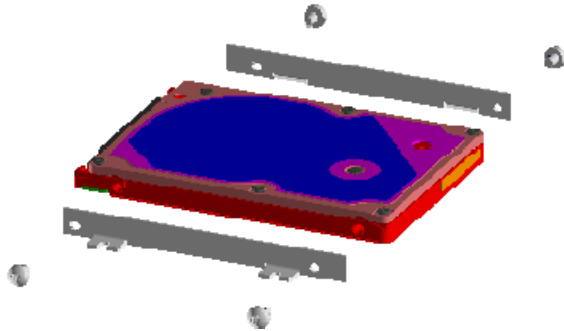


Fig. 44:Preassemble HDD

Then lower the preassembled HDD onto the carrier board and carefully slide the HDD towards the host receptacle to connect the HDD.

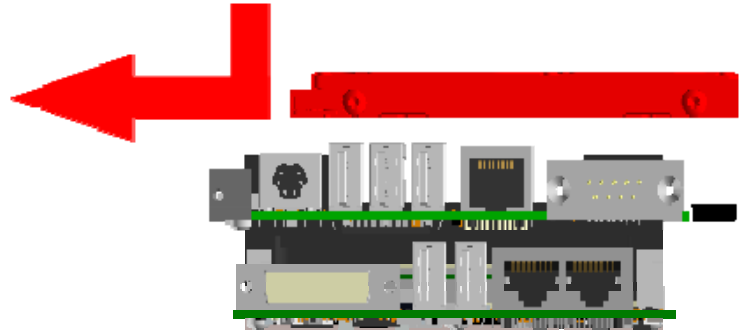


Fig. 45:Connect HDD

Then tighten the screw crosswise.

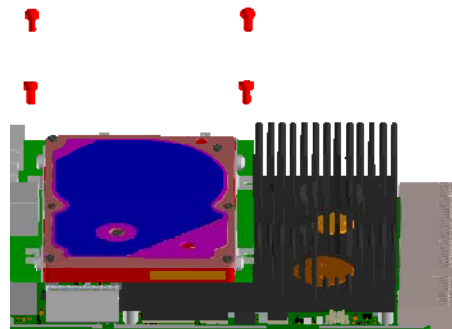


Fig. 46:Mount HDD

Release: First release the screws crosswise.

Then slide the HDD carefully away.

5 Additional Features with Rear I/O Interface

This chapter describes the additional features of the Rear I/O interface.

The additional features:

- 1 USB ports compliant to USB-Specification 1.1/2.0 with over-current control
- 2 SATA ports
- Gigabit Ethernet port (ETH 3)
- Analog VGA (shared with front-panel VGA) without DDC-Support
- SM bus support
- 1 PCI Express lane (x1)



To use all the Rear I/O features you need to order a EMTrust Rear I/O Extension Card.

6 Configuration

This Chapter explains the BIOS settings to configure your Panel Board.

Enter the BIOS

During the boot procedure you can enter the BIOS menu while pressing the key.



Please note the BIOS feature set will vary using different CPUs and used Extensions e.g. Virtualization, multi core and interface functions.

6.1 The Main Page

Award BIOS ROM has a built-in Setup program that allows users to modify the basic system configurations. This type of information is stored in battery-backed CMOS RAM, so that Setup information is retained when the power is turned off.

Once you enter Award® BIOS CMOS Setup Utility, the Main Menu (Fig. 47:Main BIOS Page) will appear on the screen. The Main Menu allows you to select from thirteen different setup functions. Two of these functions are to be used to exit the BIOS (F10 key save and exit, or ESC key exit without saving).

The Main BIOS setup screen is shown below.

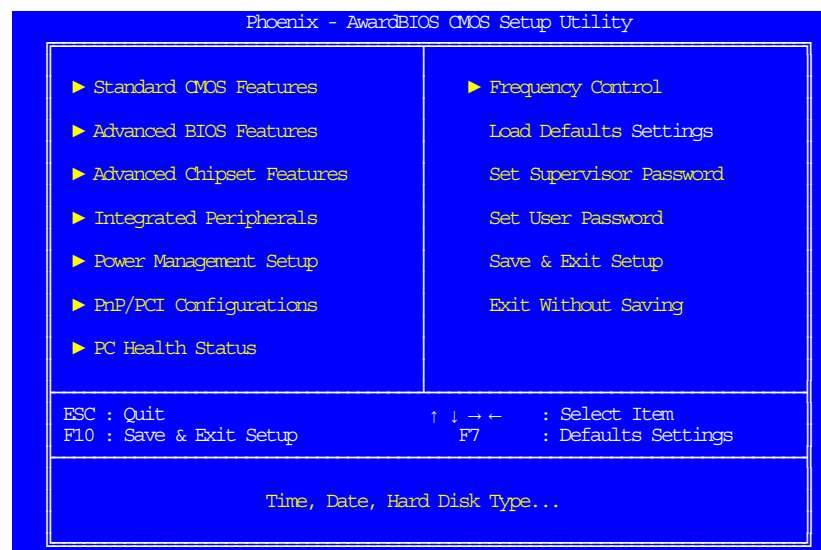


Fig. 47:Main BIOS Page

Use arrow keys to select any item and press [Enter] to accept or to enter a submenu for detail settings.

<F7>

<F7> key can be used in any Setup page to restore the Defaults Settings.

6.2 Standard CMOS Features

Use this Menu for basic system configurations.

Use the <Arrow> keys to highlight a Standard CMOS Features option.

The Standard CMOS Features Screen is shown below.

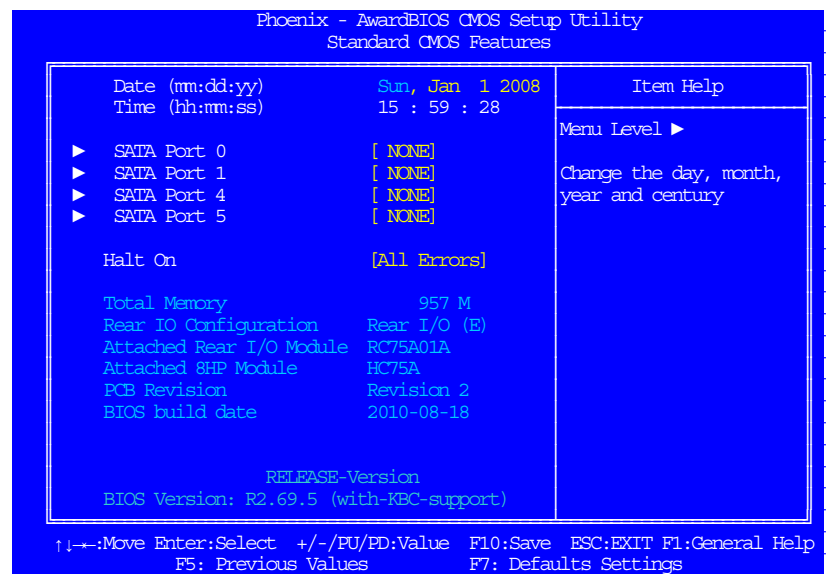


Fig. 48: Standard CMOS Features Page

Date

The date format is [Weekday] [Month] [Day] [Year].
Change the day, month and year to the actual date.

Time

The time format is [Hour] [Minute] [Second]. (Format: 24 hours)
Change the hour, minute and second to the actual time.

SATA Port X

For the description of SATA Port X refer to chapter 6.2.1.

Halt On

During POST, the computer stops if the BIOS has detected a hardware error. You can set the BIOS to ignore certain errors during POST and continue the boot-up process.

The following options are available:

[No Errors]

POST does not stop for any error.

[All Errors]

If the BIOS detect any non-fatal error, POST will stop and prompts you to take corrective action.

[All, But Keyboard]

POST does not stop if a keyboard error occurs, but stops for all other errors.

Total Memory

Total Memory

Shows the amount of available system memory.

RearIO Configuration

Shows the used RearIO Configuration.

Attached Rear I/O Module

Shows the version of the used REARI/O Module.

Attached 8HP Module

Shows the version of the used 8HP Module.

PCB Revision

Shows the used PCB Revision.

BIOS build date

Shows the build date of the used BIOS.

RELEASE-Version*

Shows the used BIOS Version and if it supports a Keyboard Controller (KBC-support).

***Please note:**



For PS/2 support the CP75 needs an appropriate BIOS version with Keyboard Controller Support (KBC-support).

The BIOS version with KBC-support will only boot-up with a present Keyboard Controller. Please ensure for a successful boot-up that the Extension Board of 8HP variant or the Rear I/O module is connected.

6.2.1 SATA Port X

Enter the next page for detailed hard drive settings.

The BIOS supports up to four SATA drives. The BIOS can automatically detect the parameters of the drive and will set the optimum operating conditions of almost all SATA drives. The BIOS will detect the drive parameters during power-on self-test (POST), every time the system boots. By pressing [ENTER], the BIOS will show the SATA channel submenu. It shows the respective SATA device information except for e.g. CD ROM or similar devices.

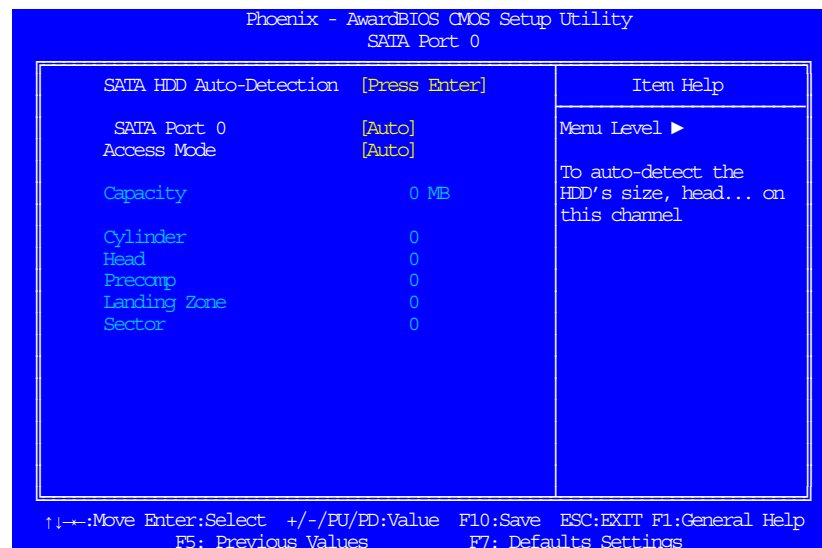


Fig. 49:SATA Channel Master Page

SATA HDD Auto-Detection

This command reads and displays the respective disk information and parameters again.

SATA Port X

The CP75 Board supports only SATA drives.

The default setting is [Auto].

Choose [None] to deactivate or [Manual] for manual setting of the SATA Port.

Access Mode

The default setting of Access Mode is [Auto].

Choose [CHS], [LBA] or [Large] when needed for your drive. If the Access Mode is set to [CHS] and the SATA Port is set to [Manual] you can set the harddisk settings by hand.



We recommend to set [AUTO] for all drives.

6.3 Advanced BIOS Features

Use this menu to set the Advanced BIOS Features available on your system.

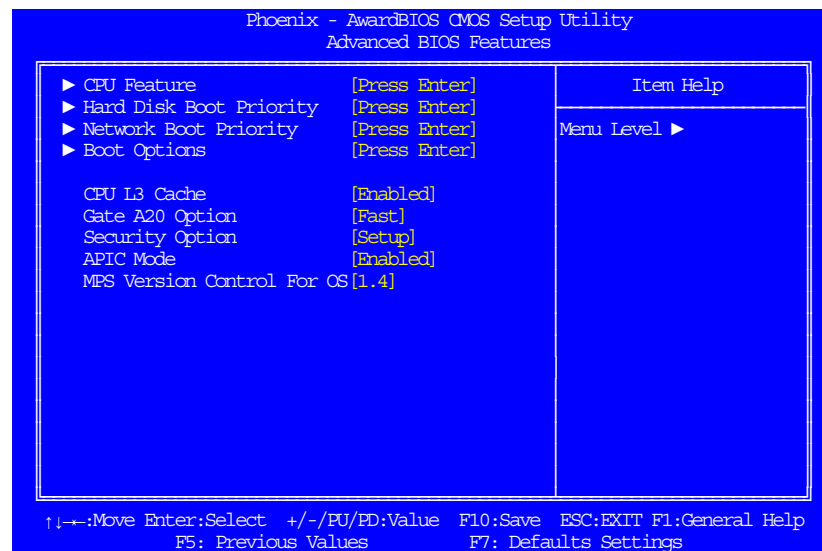


Fig. 50:Advanced BIOS Features Page

CPU Feature

For the description of the CPU Feature refer to chapter 6.3.1.

Hard Disk Boot Priority

For the description of the Hard Disk Boot Priority refer to chapter 6.3.2.

Network Boot Priority

For the description of the Network Boot Priority refer to chapter 6.3.3.

Boot Options

For the description of the Boot Options refer to chapter 6.3.4.

CPU L3 Cache

The default value is [Enabled]. When [Disabled] is chosen it forces the L3 cache in off-state.

Gate A20 Option (Only available with KBC supporting BIOS)

The default value is [Fast]. When [Normal], it forces the system to use the slower keyboard controller for the memory handling.

Security Option

The default value is [Setup].

When [System] is chosen the set BIOS password is needed for boot up and to enter Setup.

When [Setup] is chosen the set BIOS password is needed to enter Setup.

APIC Mode

The default is [Enable].

When [Disabled], it deactivates the APIC (Advanced Programmable Interrupt Controller) functions.

MPS Version Control For OS

The default is [1.4].

If your OS needs version 1.1, change the setting to [1.1].

6.3.1 CPU Feature

Displays a menu to set the CPU Features.

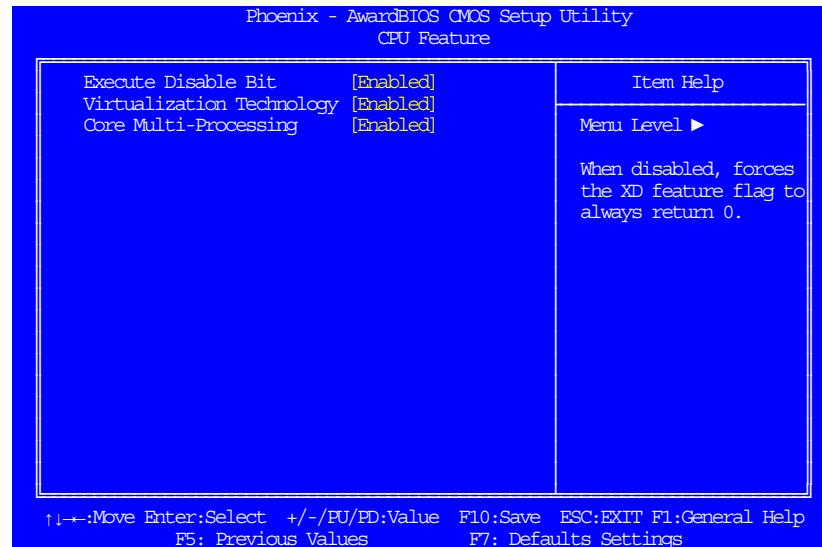


Fig. 51:CPU Feature Page

Execute Disable Bit

The default value is [Enabled]

When [Disabled], it forces the XD feature flag to always return 0.

Virtualization Technology (depends on processor support)

The default value is [Enabled].

The second setting is [Disabled], if function is not needed.

Core Multicore-Processing (depends on processor support)

The default value is [Enabled].

The second setting is [Disabled], if function is not needed.

6.3.2 Hard Disk Boot Priority

This option allows the user to control the order of the boot devices.

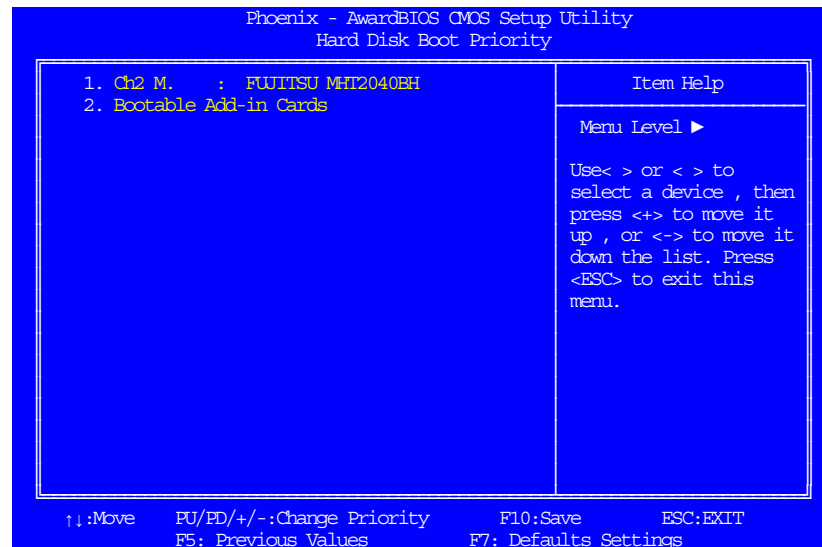


Fig. 52: Hard Disk Boot Priority Page

Use <UP> or <DOWN> to select a device, then change priority by pressing <+> to move it up, or <-> to move it down the list. Press <ESC> to exit this menu.

6.3.3 Network Boot Priority

This option allows the user to control the order of the network boot devices.

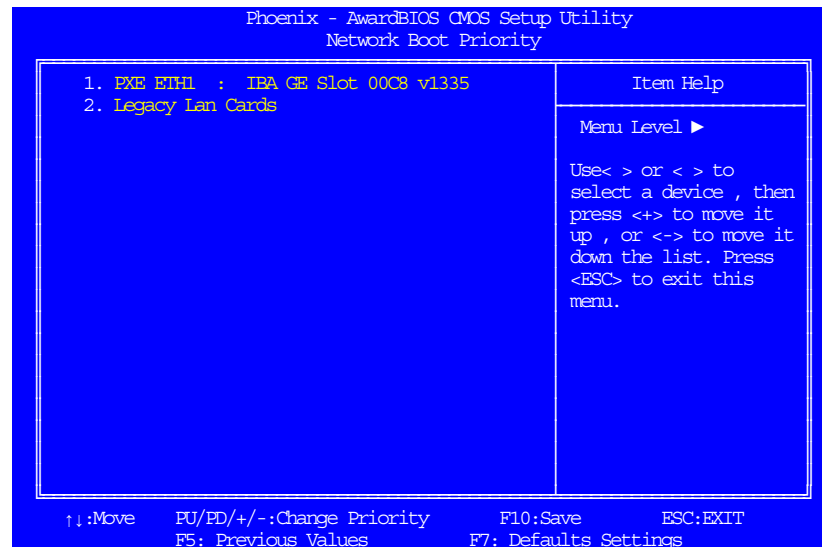


Fig. 53:Hard Disk Boot Priority Page

Use <UP>or <DOWN> to select a device, then change priority by pressing <+> to move it up, or <-> to move it down the list. Press <ESC> to exit this menu.

6.3.4 Boot Options

Displays a menu to set the order in which devices are checked for boot capabilities.

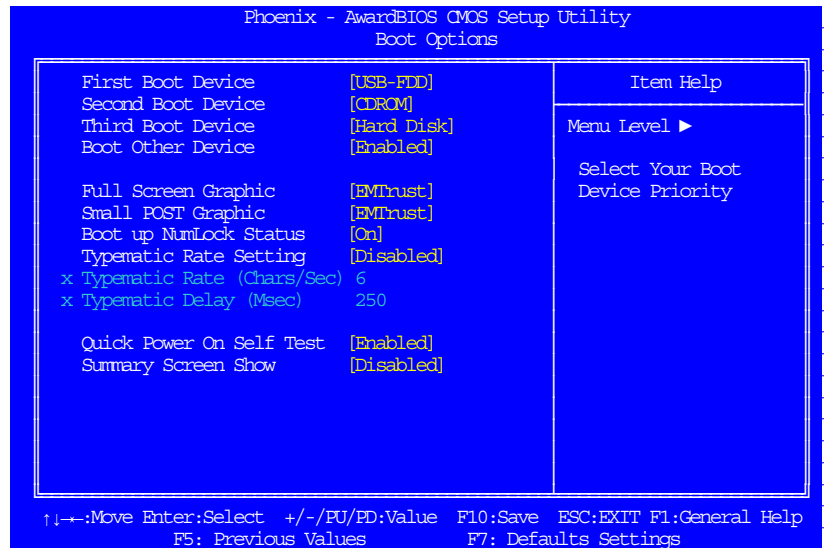


Fig. 54: Boot Options Page

For Example:

When [Floppy] is selected, the BIOS attempt to load the Operating System from a Floppy.

When [CDROM] is selected, the Operating System will be loaded from the CDROM; all other bootable add-in cards are displayed in numerical order.

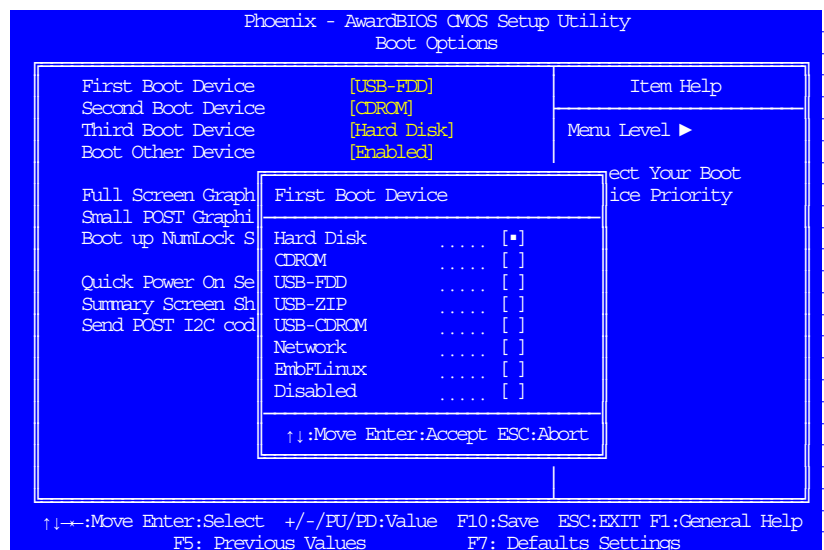


Fig. 55: Boot Options Detail

First Boot Device

This item [Fig. 54:Boot Options Page] allows you to set the sequence of boot devices where BIOS attempt to load the OS.



If the first boot-up device should be changed for the next boot-up, the boot menu can be used.

Press <ESC> at the beginning of the boot-up sequence and change the Boot First device in the boot menu.

Second Boot Device

Select the device that is checked second for boot.

Third Boot Device

Select the device that is checked third for boot.

Boot Other Device

The default value is [Enabled].

Two options are available: [Enabled] and [Disabled].

Full Screen Graphic

Select the full-screen graphic to be displayed during system starts up instead of text messages.

The default value is [EMTrust]. Choose [None] to display the messages during system start up.

Small POST Graphic

This item enables you to show the company logo on the boot up screen if option Full screen graphic [NONE] is selected.

The default value is [EMTrust]. Choose [None] to boot without POST graphic.

Boot up NumLock Status

When is [On] – At boot up, the Numeric Keypad is in numeric mode.

When is [Off] – At boot up, the Numeric Keypad is in cursor control mode.

The default setting is [On].

Typematic Rate Setting (Only available with KBC supporting BIOS)

When enabled, the typematic rate and typematic delay can be selected. The default setting is [Disabled].

Quick Power On Self Test

When enabled certain tests during the system boot up are skipped. This will decrease the boot-time of the system.

The default setting is [Enabled].

Summary Screen Show

When enabled, a summary of the configuration detected through the BIOS POST, is shown before the OS is loaded.

The default setting is [Disabled].

6.4 Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize the system performance.

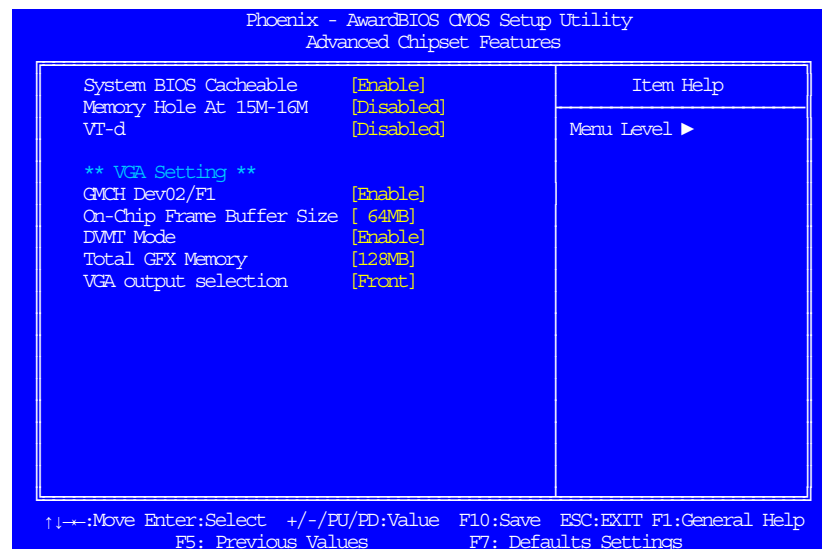


Fig. 56: Advanced Chipset Features Page

System BIOS Cacheable

You can select [Enabled] or [Disabled]. Selecting [Enabled] allows caching of the video BIOS, resulting in better system performance. However, if any program writes to this memory area, a system error may result. The default setting is [Enabled].

Memory Hole AT 15M-16M

Two options are available: [Enabled] or [Disabled]. This option is used to reserve the memory blocks 15 - 16M for ISA adapter ROM. Some special peripherals need to use a memory block located between 15M and 16M, and this memory block has a size of 1M. We recommend that you disable this option if not required.

The default setting is [Disabled].

VT-d

The default value is [Disabled]. The second setting is [Enabled], this activates the Intel® Virtualization Technology for Directed I/O.

GMCH Dev02/F1

The default value is [Enabled]

When [Disabled], it forces the GMCH to disable the 2nd onboard Video Function (Dev02/F1).

On-Chip Frame Buffer Size

Alternatively [32MB], [64MB] or [128MB] setting is available. This setting enhances the VGA parameters for high resolution application.

The default setting is [64MB].

DVMT Mode

Intel® DVMT (Dynamic Video Memory Technology) 3.0

If [Enable] is selected, the select the memory amount, it will no longer be available for system memory.

Default setting is [Enable].

Total GFX Memory

You can select the fixed memory amount for the video memory to [128MB] or [256MB]. If [MAX.] is chosen the video memory size will be maximized according to the available memory size.

Default setting is [128MB].

VGA output selection (Only available with present REAR I/O module)

If a Rear I/O module is connected the VGA output can be switched from [Front] to [RearIO].

Default setting is [Front].

6.5 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

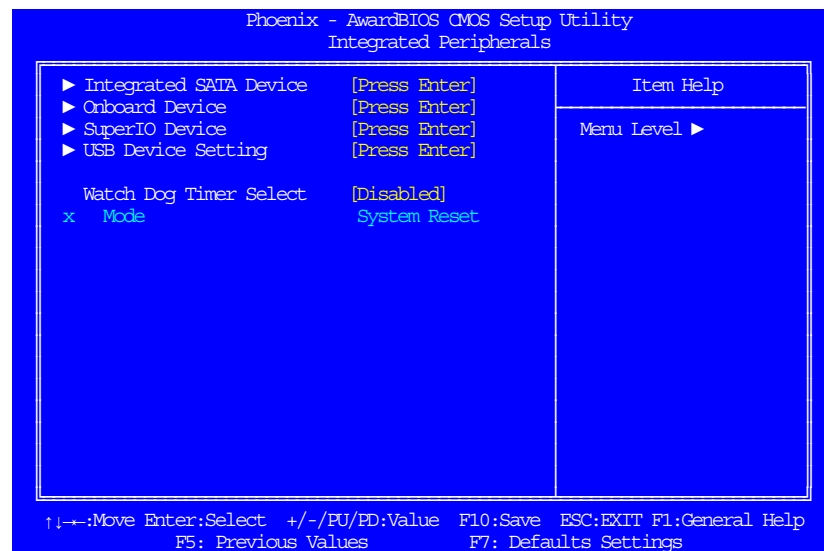


Fig. 57: Integrated Peripherals Page

Integrated SATA Device

For the description of the Integrated SATA Device refer to chapter 6.5.1.

Onboard Device

For the description of the Onboard Device refer to chapter 6.5.2.

SuperIO Device (Only available with 8HP or Rear I/O module)

For the description of the SuperIO Device refer to chapter 6.5.3.

USB Device Setting

For the description of the USB Device Setting refer to chapter 6.5.4.

Watch Dog Timer Select

If [Disabled] is selected the Watch Dog Timer will be inactive. The Watch Dog Timer can be set from [10 Sec] to [4 Min] and the Mode can be set to [System Reset] or [Power cycle]. [System Reset] causes a System Reset and the [Power cycle] causes a complete Power cycle. Default setting is [Disabled].

6.5.1 Integrated SATA Device

Use this menu to specify your settings for the OnChip SATA Device.

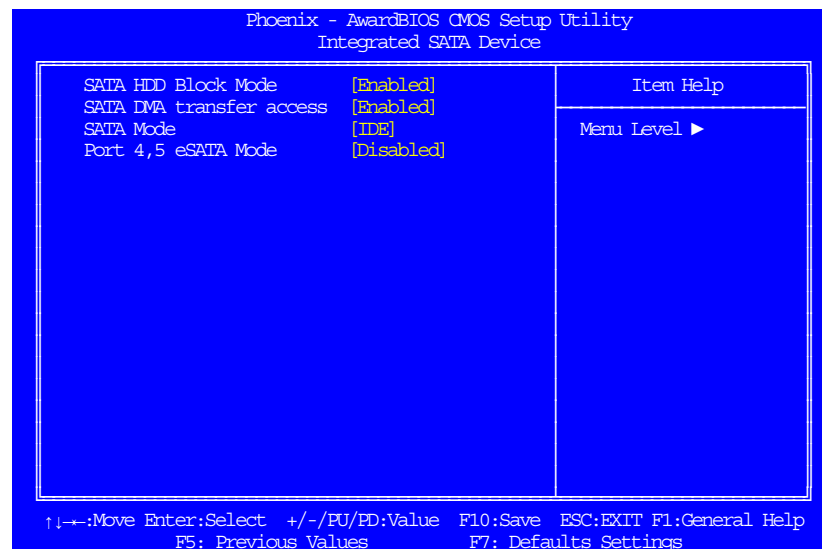


Fig. 58: OnChip SATA Device Page

SATA HDD Block Mode

The default is [Enabled] to use fast block mode. If necessary the support can be [Disabled].

SATA DMA transfer access

The default is [Enabled]. If necessary the support can be [Disabled].

SATA Mode

Please set the used SATA Mode [IDE] or [AHCI]. The default is [IDE].

Port 4,5 eSATA Mode

If [Enabled] set the Port 4 and 5 to eSATA Mode. The default is [Disabled].

6.5.2 Onboard Device

Settings to enable or disable the Onboard Devices.

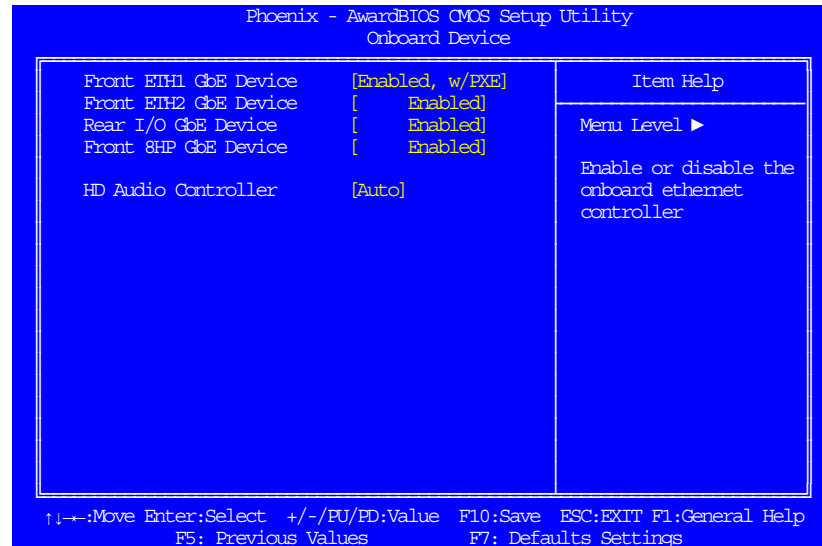


Fig. 59: Onboard Device Page

Front ETH1 GbE Device

Three options are available: [Enabled], [Enabled, w/PXE] and [Disabled].

The default setting is [Enabled, w/PXE]. This enables network boot-up with PXE protocol.

[Enabled] activates the GbE Device without PXE protocol.

[Disabled] deactivates the GbE Device.

Front ETH2 GbE Device

Two options are available: [Enabled] and [Disabled].

The default setting is [Enabled].

Rear I/O GbE Device (only with Rear I/O module)

Two options are available: [Enabled] and [Disabled].

The default setting is [Enabled].

Front 8HP GbE Device (only 8HP)

Two options are available: [Enabled] and [Disabled].

The default setting is [Enabled].

HD Audio Controller

Two options are available: [Auto] and [Disabled].

The default setting is [Auto].

6.5.3 Super IO Device (only 8HP or Rear I/O module)

Settings to enable or disable the SuperIO Devices.

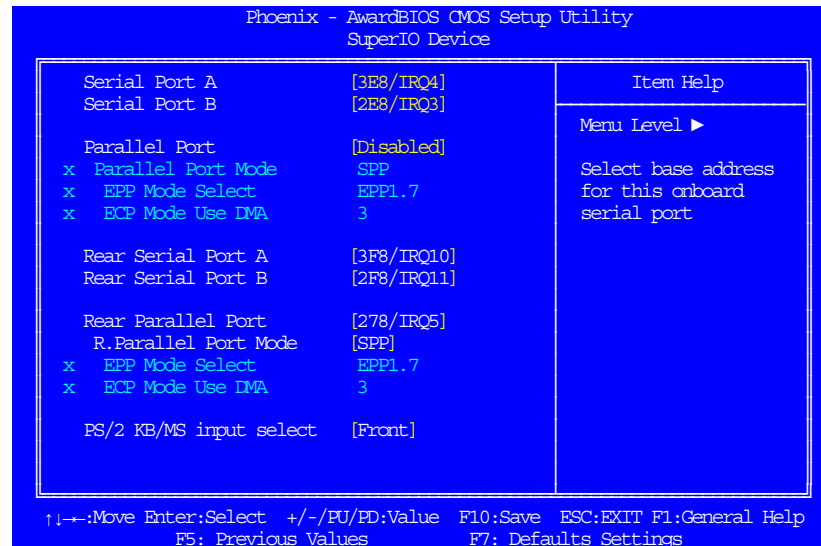


Fig. 60: SuperIO Device Page

Serial Port A

Please select the base address and interrupt for Serial Port A or disable it.

These I/O address/Interrupt combinations are possible:
[3F8/IRQ4], [2F8/IRQ3], [3E8/IRQ4] or [2E8/IRQ3]

The default setting is [3E8/IRQ4].

The recommended setting is [3E8/IRQ4].

Serial Port B

Please select the base address and interrupt for Serial Port B or disable it.

These I/O address/Interrupt combinations are possible:
[3F8/IRQ4], [2F8/IRQ3], [3E8/IRQ4] or [2E8/IRQ3]

The default setting is [Disabled].

The recommended setting is [2E8/IRQ3].

Parallel Port

Please select the base address and interrupt for Parallel Port or disable it.

These I/O address/Interrupt combinations are possible:
[378/IRQ7], [278/IRQ5] or [3BC/IRQ7]
The default setting is [Disabled].
The recommended setting is [378/IRQ7].

Parallel Port Mode

The default setting is [SPP].
These port modes are possible: [SPP], [EPP], [ECP],
[ECP+EPP] or [Normal]. Choose the preferred mode for
your application.

EPP Mode Select

If EPP Mode is selected, the mode can be set to [EPP1.9]
or [EPP1.7]. The default setting is [EPP1.7].

ECP Mode Use DMA

If ECP Mode is selected, the DMA channel can be set to
[1] or [3]. The default setting is [3].

Rear Serial Port A (only with Rear I/O module)

Please select the base address and interrupt for Rear
Serial Port A or disable it.
These I/O address/Interrupt combinations are possible:
[3F8/IRQ10], [2F8/IRQ10], [3E8/IRQ10] or [2E8/IRQ10]
The default setting is [3F8/IRQ10].
The recommended setting is [3F8/IRQ10].

Rear Serial Port B (only with Rear I/O module)

Please select the base address and interrupt for Rear
Serial Port B or disable it.
These I/O address/Interrupt combinations are possible:
[3F8/IRQ11], [2F8/IRQ11], [3E8/IRQ11] or [2E8/IRQ11]
The default setting is [2F8/IRQ11].
The recommended setting is [2F8/IRQ11].

Rear Parallel Port

Please select the base address and interrupt for Rear Parallel Port or disable it.

These I/O address/Interrupt combinations are possible: [378/IRQ5], [278/IRQ5] or [3BC/IRQ5]

The default setting is [278/IRQ5].

The recommended setting is [278/IRQ5].

Parallel Port Mode

The default setting is [SPP].

These port modes are possible: [SPP], [EPP], [ECP], [ECP+EPP] or [Normal]. Choose the preferred mode for your application.

EPP Mode Select

If EPP Mode is selected, the mode can be set to [EPP1.9] or [EPP1.7]. The default setting is [EPP1.7].

ECP Mode Use DMA

If ECP Mode is selected, the DMA channel can be set to [1] or [3]. The default setting is [3].

PS/2 KB/MS input select (Only with KBC supporting BIOS)

If the BIOS has Key Board Controller-support (KBC-support), the PS/2 keyboard and mouse input can be set to [Front] or [RearIO]. The default setting is [Front].

6.5.4 USB Device Setting

Setting to enable or disable the USB Device Setting.

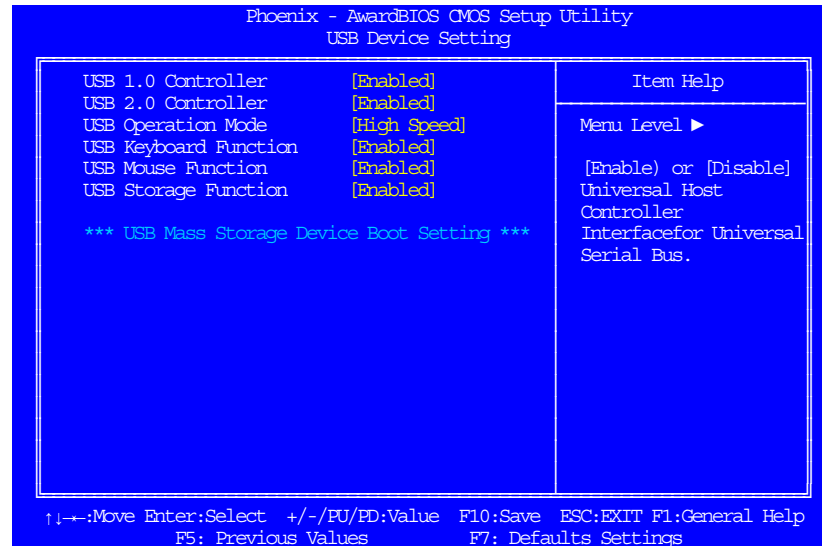


Fig. 61:USB Device Page

USB 1.0 Controller

Two options are available: [Enabled] and [Disabled].
The default setting is [Enabled].

USB 2.0 Controller

Two options are available: [Enabled] and [Disabled].
The default setting is [Enabled].

USB Operation Mode

Two options are available: [Full/Low Speed] and [High Speed]. The default setting is [High Speed].

USB Keyboard Function

Two options are available: [Enabled] and [Disabled]. If your system contains a USB keyboard, choose [Enabled]. The default setting is [Enabled].

USB Mouse Function

Two options are available: [Enabled] and [Disabled]. If your system contains a USB mouse, choose [Enabled].

The default setting is [Enabled].

USB Storage Function

Two options are available: [Enabled] and [Disabled]. If your system contains a USB Storage device, choose [Enabled]. The default setting is [Enabled].

6.6 Power Management Setup

The Power Management Menu allows you to reduce power consumption. This features turn off the video display and shuts down the hard disk after a period of inactivity.

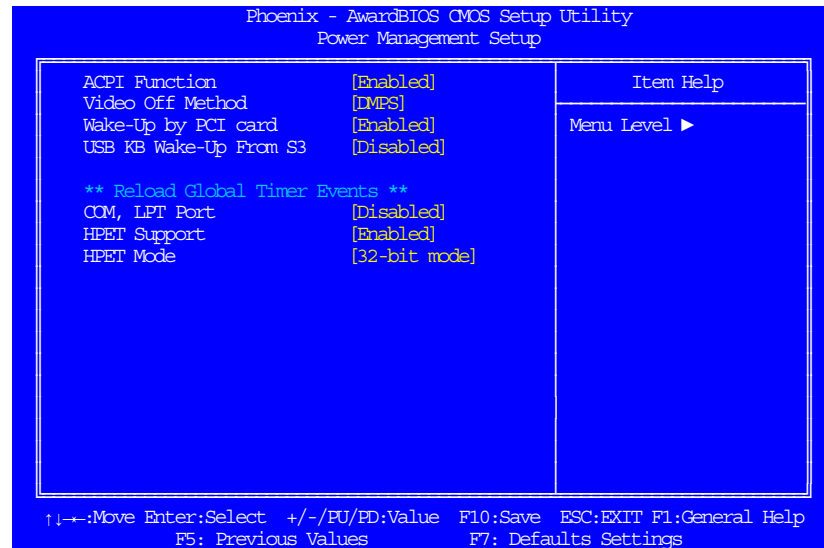


Fig. 62: Power Management Setup Page

ACPI Function

Two options are available: [Enable] and [Disable]. This item allows you to enable/disable the Advanced Configuration and Power Management (ACPI). The default setting is [Enabled].

Video Off Method

The default setting is [DPMS].

Three options are available: (This item selects the way how the monitor is blanked.)

[V/H SYNC+Blank] - This selection will cause the system to turn off the vertical and horizontal synchronization ports and also writes blanks to the video buffer.

[Blank Screen] - This option only writes blanks to the video buffer.

[DPMS] - Display power management signalling according to DMPS specification.

Wake-Up by PCI card

This function enables or disables wake-up by PCI card.
Default value is [Disabled].

USB KB Wake-Up From S3

This function enables or disables wake-up from ACPI Suspend Type S3 for USB keyboards.
Default value is [Disabled].

Reload Global Timer Events

Reload Global Timer events are I/O events. When they occur, they prevent the system from entering a power saving mode or will wake up the system from such a mode.

The system remains alert for anything that occurs to a device which is configured as [Enabled], even when the system is in a power down mode.

COM,LPT Port

This function enables or disables COM/LPT events.
Default value is [Disabled].

HPET Support

This function enables or disables the HPET Support.
Default value is [Enabled].

HPET Mode

This function selects the HPET Mode.
Default value is [32-bit mode]. If your OS support 64-bit mode, choose [64-bit mode].

6.7 PnP/PCI Configurations

This section describes the configuration of the PCI bus system.

PCI (Personal Computer Interconnect) is a bus that allows I/O devices to operate at high speed.

This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.

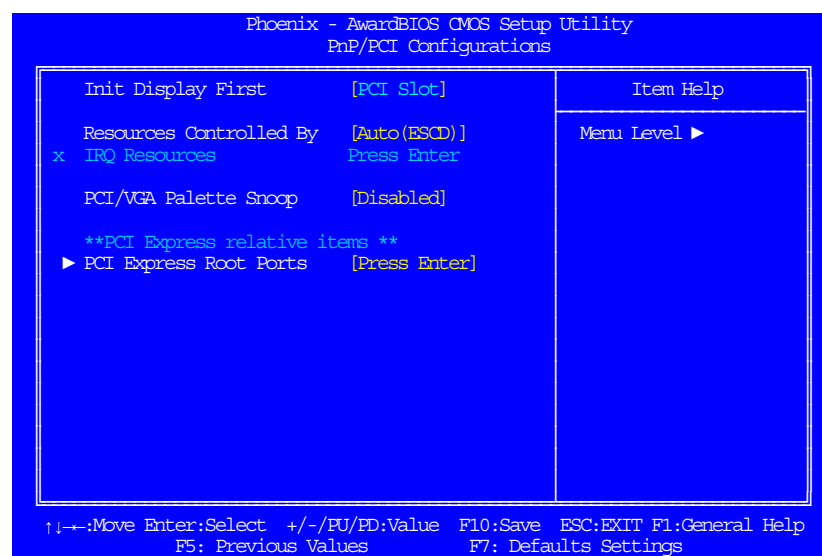


Fig. 63:PnP/PCI Configurations Page

Init Display First

The user can choose which device is initialized first as the primary device, an external PCI–graphics card or the [Onboard] graphics controller.

Default setting is [PCI Slot].

Resources Controlled By

The Award Plug and Play BIOS has the ability to configure all plug and play compatible devices automatically. If you set this option to [Manual], choose specific resources by following submenus (a sub menu is preceded by an “x”). Two options are available: [Auto (ESCD)] and [Manual]. The default setting is [Auto (ESCD)].

IRQ Resources

When resources are controlled manually, assign each system interrupt a type, depending on the type of device using the interrupt.

PCI/VGA Palette Snoop

Some non-standard VGA cards, such as graphics accelerators or MPEG video cards may not show colors properly. The setting [Enable] should correct this problem. Otherwise leave this with the default setting set to [Disable].

PCI Express Root Ports

For the description of the PCI Express Root Ports Setting refer to chapter 6.7.1.

6.7.1 PCI Express Root Ports

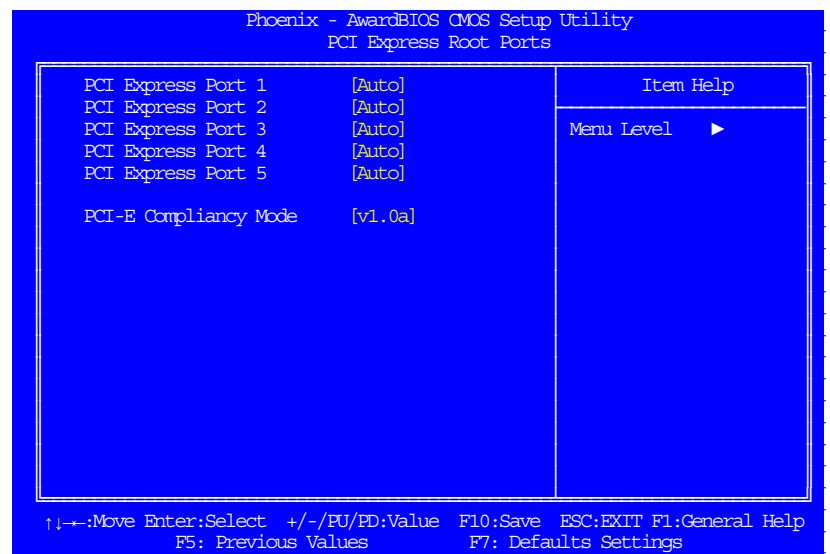


Fig. 64:PCI Express Root Ports Page

PCI Express Port X

Port default value is [AUTO].

PCI-E Compliancy Mode

Choose [v1.0a] or [v1.0] PCI Express standards

Default value [v1.0a]

6.8 PC Health Status

This Setup screen shows the actual temperature of the system.

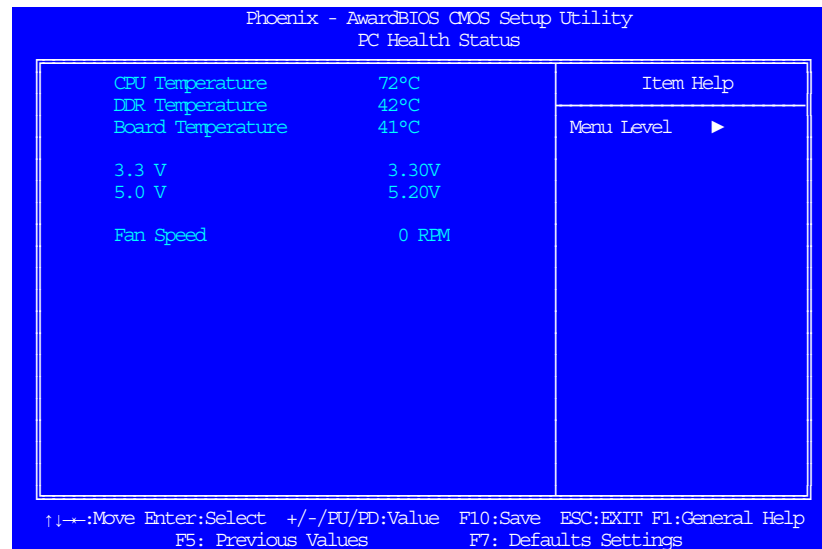


Fig. 65:PC Health Status Page

CPU Temperature

Shows the actual temperature of the CPU.

DDR Temperature

Shows the actual temperature below the RAM sockets.

Board Temperature

Shows the actual temperature of the CPU board.

3.3 V

Shows the exact voltage value of the 3.3 V circuit.

5.0 V

Shows the exact voltage value of the 5.0 V circuit.

Fan Speed

Shows the exact speed of the CPU fan (if installed).

6.9 Frequency Control

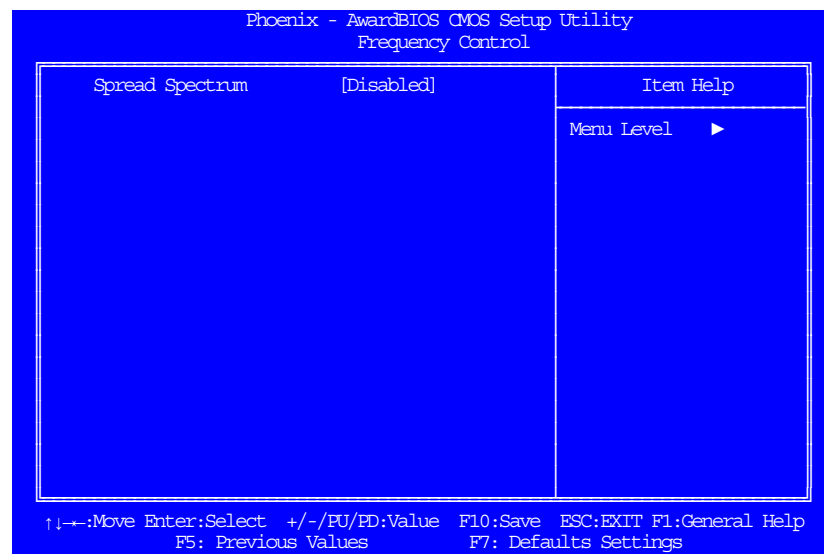


Fig. 66:Frequency/Voltage Control Page

Spread Spectrum

This function can be enabled to reduce existing electromagnetic interferences.

We recommend the default value [Disabled].

Appendix 1

SM Bus Addresses

Primary SM bus (ICH9M = Master)	
0xD2	Clock generator - CK505
0xA0	SO-DIMM0 - SPD
0xA4	SO-DIMM1 - SPD
<i>tbd</i>	Intel GbE 82574 - 2 nd FP
<i>tbd</i>	Intel GbE 82574 - 3 rd Rear I/O
0xAA	PCI Express Mini Card Socket
0xAC	8HP daughter-board EEPROM (only if a 8HP extension is present)
0xC0	Microchip PIC - I ² C Interface #2
0xA8	EEPROM for PIC

Tab. 13: Primary SM Bus

Appendix 2

PCI Devices

Bus	Device	Func.	Vendor	Device	Description
00	00	0	8086	2a40	Host bridge: Intel Corporation Mobile 4 Series Chipset Memory Controller Hub
00	02	0	8086	2a42	VGA compatible controller: Intel Corporation Mobile 4 Series Chipset Integrated Graphics Controller
00	02	1	8086	2a43	Display controller: Intel Corporation Mobile 4 Series Chipset Integrated Graphics Controller
00	19	0	8086	10f5	Ethernet controller: Intel Corporation 82567LM Gigabit Network Connection
00	1a	0	8086	2937	USB Controller: Intel Corporation 82801I (ICH9 Family) USB UHCI Controller #4
00	1a	1	8086	2938	USB Controller: Intel Corporation 82801I (ICH9 Family) USB UHCI Controller #5
00	1a	2	8086	2939	USB Controller: Intel Corporation 82801I (ICH9 Family) USB UHCI Controller #6
00	1a	7	8086	293c	USB Controller: Intel Corporation 82801I (ICH9 Family) USB2 EHCI Controller #2
00	1b	0	8086	293e	Audio device: Intel Corporation 82801I (ICH9 Family) HD Audio Controller
00	1c	0	8086	2940	PCI bridge: Intel Corporation 82801I (ICH9 Family) PCI Express Port 1
00	1c	1	8086	2942	PCI bridge: Intel Corporation 82801I (ICH9 Family) PCI Express Port 2
00	1c	2	8086	2944	PCI bridge: Intel Corporation 82801I (ICH9 Family) PCI Express Port 3
00	1c	3	8086	2946	PCI bridge: Intel Corporation 82801I (ICH9 Family) PCI Express Port 4
00	1c	4	8086	2948	PCI bridge: Intel Corporation 82801I (ICH9 Family) PCI Express Port 5
00	1d	0	8086	2934	USB Controller: Intel Corporation 82801I (ICH9 Family) USB UHCI Controller #1
00	1d	1	8086	2935	USB Controller: Intel Corporation 82801I (ICH9 Family) USB UHCI Controller #2

00	1d	2	8086	2936	USB Controller: Intel Corporation 82801I (ICH9 Family) USB UHCI Controller #3
00	1d	7	8086	293a	USB Controller: Intel Corporation 82801I (ICH9 Family) USB2 EHCI Controller #1
00	1e	0	8086	2448	PCI bridge: Intel Corporation 82801 Mobile PCI Bridge
00	1f	0	8086	2917	ISA bridge: Intel Corporation ICH9M-E LPC Interface Controller
00	1f	2	8086	2918	IDE interface: Intel Corporation ICH9M/M-E 2 port SATA IDE Controller
00	1f	3	8086	2930	SMBus: Intel Corporation 82801I (ICH9 Family) SMBus Controller
00	1f	5	8086	292d	IDE interface: Intel Corporation ICH9M/M-E 2 port SATA IDE Controller
01	00	0	8086	10d3	Ethernet controller: Intel Corporation 82574L Gigabit Network Connection (ETH2)
02	00	0	8086	10d3	Ethernet controller: Intel Corporation 82574L Gigabit Network Connection (REAR ETH)
03	00	0	1095	3132	Mass storage controller: Silicon Image, Inc. Sil 3132 Serial ATA Raid II Controller (REAR I/O module)
04	00	0	8086	10d3	Ethernet controller: Intel Corporation 82574L Gigabit Network Connection (ETH3)
05	03	0	12d8	8150	PCI bridge: Pericom Semiconductor PCI to PCI Bridge

Tab. 14: PCI Devices

Appendix 3

Revision History

Date	Version	Changes	Proofed to release
09.06.2009	0.0	First draft	
24.06.2009	0.1	First internal release	
23.08.2010	1.0	Production release	

Tab. 15:Revision History

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Terminology

- (G)MCH** (Graphics) Memory Controller Hub
- CMOS** Complementary metal-oxide-semiconductor - a technology to build circuits like microprocessors
- Core** The internal base logic in the Mobile Intel® 915 Express chipset (G)MCH
- CPU** Central Processing Unit or processor
- CRT** Cathode Ray Tube
- DBI** Dynamic Bus inversion
- DDR2** Second generation Double Data Rate SDRAM memory technology
- DDR3** Third generation Double Data Rate SDRAM memory technology
- DMA** Direct Memory Access, feature that allows hardware subsystems to access system memory independent of the CPU
- DMI** Direct Media Interface - The chip-to-chip interconnect between the Mobile Intel® 915 Express chipset and the Penryn. It is an Intel Proprietary interface
- DVI** Digital Visual Interface is the interface specified by the DDWG (Digital Display Working Group)
- EMI** Electromagnetic Interference
- Fast Ethernet** Ethernet connection with a frame transfer speed up to 100Mbit/s.

- Firmware** A computer program that is embedded in a hardware device like a Flash ROM. The computer's BIOS is a firmware.
- FSB** Front Side Bus - Connection between Mobile Intel® 915 Express chipset and the CPU. Also known as the Host interface.
- Gigabit Ethernet** Ethernet connection with a frame transfer speed up to 1000Mbit/s.
- Host** This term is used synonymously with processor
- I²C** Inter-IC (a two wire serial bus created by Philips)
- ICH** The I/O Controller Hub component that contains the main PCI interface, LPC interface, USB2, Serial ATA, and other I/O functions. It communicates with the (G)MCH over a proprietary interconnect called DMI.
- iDCT** Inverse Discrete Cosine Transform, a mathematical function used for applications like image processing
- IDE** The predecessor of SATA - a parallel bus system for connecting hard disks and other devices.
- iHDMI** Integrated High Definition Multimedia Interface
- Intel® TxT** Intel® Trusted Execution Technology - a technology to protect programme execution against software-based attacks.
- Intel® VT-d** Intel® Virtualization Technology (Intel® VT) for Directed I/O - protecting virtual machines for DMA breaks (a possible threat for data security).

- INTx** An interrupt request signal where X stands for interrupts A,B,C and D.
- IRDA** Infrared Data Association and the acronym of an optical wireless communication interface.
- IRQ** Interrupt Request - Signal used in a computer system to react to an event occurring during processing.
- ITPM** Integrated Trusted Platform Model - a security model based on the Trusted Platform Module microcontroller.
- KBC** Keyboard Controller
- Lanes** A unidirectional communication point-to-point connection
- LCD** Liquid Crystal Display
- LFP** Local Flat Panel
- LPC Bus** Low Pin Count Bus - Bus to connect low-bandwidth devices to the CPU with only seven signals.
- LVDS** Low Voltage Differential Signalling - A high speed, low power data transmission standard used for display connections to LCD panels.
- NCTF** Non-Critical to Function
- NTSC** National Television Standards Committee - color encoding system use in broadcast television systems.
- PAL** Phase Alternate Line - color encoding system use in broadcast television systems.

- PAVP** Protected Audio - Video Path for supporting secure playback of Intel HD Audio and Video content - a copy protection system for digital signals.
- PCI** Peripheral Component Interconnect - Parallel computer bus for attaching peripheral devices to a motherboard.
- PCI Express** A standard for expansion interface divided into lanes.
- PIO** Programmed Input/Output is a method of transferring data between the CPU and a peripheral. Used by ATA- / IDE- Interfaces
- POST** Power-on Self Test is a pre-boot sequence to verify and start the computer system.
- PWM** Pulse Width Modulation
- Rank** A unit of DRAM corresponding 4 to 8 devices in parallel. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
- RS-232** A standard for serial communication normally found by the COM – Ports.
- S.M.A.R.T** Self-Monitoring, Analysis, and Reporting Technology - system to provide a higher data security on hard disks.
- SATA** Serial Advanced Technology Attachment - computer bus technology for connecting hard disks and other devices
- SCI** System Control Interrupt
- SDVO** Digital display channel that serially transmits digital display data to an external SDVO device.
The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e.,

TMDS, LVDS, TV-Out). This interface is not electrically compatible with the previous digital display channel - DVO. For the Mobile Intel® 915 Express chipset family, it will be multiplexed on a portion of the x16 graphics PCI Express Interface.

SDVO Device Third party codec that utilizes SDVO as an input. May have a variety of output formats, including DVI, LVDS, TV-out, etc.

SIM Subscriber Identity Module (Card) used to store information in mobile phones.

SMBus Two-wire bus for low-bandwidth communication on a motherboard.

SO-DIMM Small Outline Dual In-line Memory Module is a form factor for memory modules.

SPI-Flash Non-volatile computer memory that can be electrically erased and reprogrammed via the Serial Peripheral Interface Bus (SPI).

Ultra ATA The predecessor of SATA - a parallel bus system for connecting hard disks and other devices.

VLD Variable Length Decoding

Watchdog A watchdog (timer) is a computer hardware timing device that triggers a system reset if the main program "hangs", in order to keep the computer running.

x1 Refers to a Link or Port with one Physical Lane

x16 Refers to a Link or Port with sixteen Physical Lanes

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