R&S®RTO-K91, R&S®RTO6-K91, R&S®RTP-K91
DDR3 Compliance Test
User Manual

1178877102
Version 09

ROHDE&SCHWARZ
Make ideas real

This document describes the following DDR3 Compliance Test Procedures:

- R&S®RTO-K91 (1337.8891.02)
- R&S®RTO6-K91 (1801.6993.02)
- R&S®RTP-K91 (1337.8840.02)

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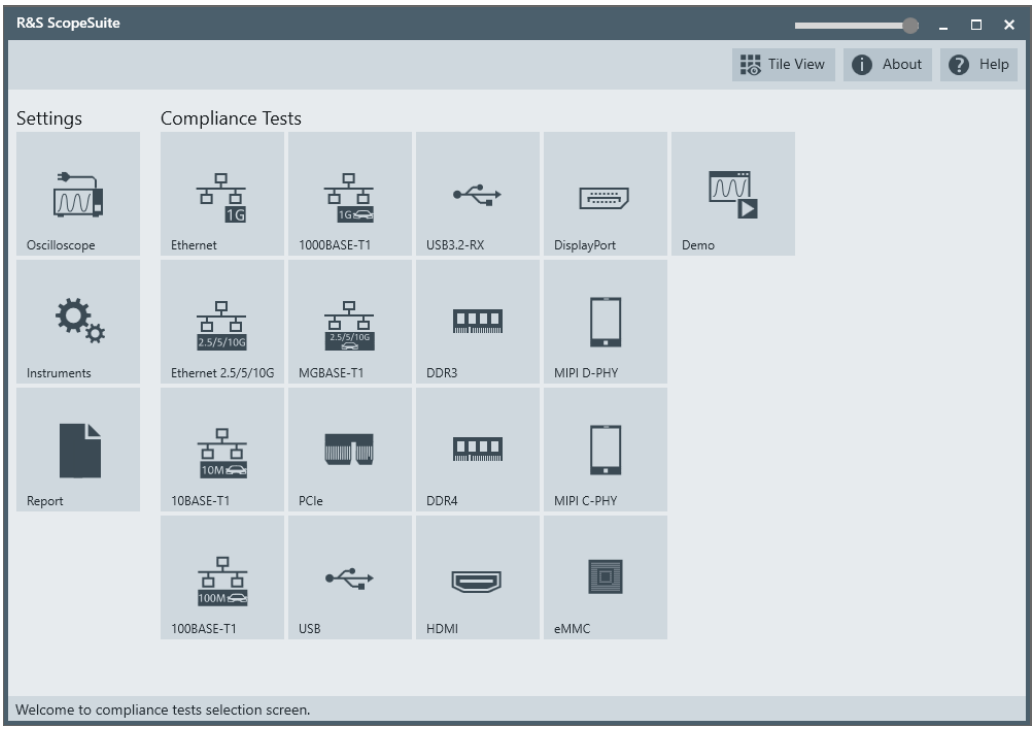
1178.8771.02 | Version 09 | R&S®RTO-K91, R&S®RTO6-K91, R&S®RTP-K91

Throughout this manual, products from Rohde & Schwarz are indicated without the ® symbol , e.g. R&S®ScopeSuite is indicated as R&S ScopeSuite.

Contents

1 R&S ScopeSuite overview

The R&S ScopeSuite software is used with R&S RTO/RTO6/RTP oscilloscopes. It can be installed on a test computer or directly on the oscilloscope. For system requirements, refer to the Release Notes.



The R&S ScopeSuite main panel has several areas:

- "Settings": connection settings to oscilloscope and other instruments also default report settings
- "Compliance Tests": selection of the compliance test
- "Demo": accesses demo test cases that can be used for trying out the software without having a connection to an oscilloscope
- : shift sideways to change the transparency of the dialog box
- "Help": opens the help file, containing information about the R&S ScopeSuite configuration
- "About": gives information about the R&S ScopeSuite software
- "Tile View": allows a personalization of the compliance test selection
  You can configure which tests are visible in the compliance test section and which are hidden, so that only the ones you use are displayed.

► To hide a test from the "Compliance Tests" view, do one of the following:

a) Right-click on the compliance test that you want to hide.
The icon of the test changes, see Figure 1-1. Now with a left click you can hide the test.

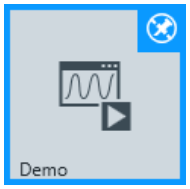


Figure 1-1: Unpin icon

b) Click on "Title View" to show a list of the available test cases. By clicking a test case in the show list, you can pin/unpin it from the main panel.

2 Preparing the measurements

2.1 Test equipment

For DDR3 compliance tests, the following test equipment is needed:

- R&S RTP with 4 channels and minimum 8 GHz bandwidth, or
  R&S RTO2000 with 4 channels and minimum 4 GHz bandwidth
  R&S RTO6 with 4 channels and minimum 4 GHz bandwidth
- R&S RTP-K91 DDR3 compliance test option (required option, installed on the R&S RTO/RTO6/RTP)
- 4 modular probes, R&S ZM90 with 9 GHz bandwidth. See also Chapter 2.1.1, "Soldering guide for modular probes", on page 9.
- 4 modular probe tips R&S RT-ZMA10 or R&S RT-ZMA14
- The free-of-charge R&S ScopeSuite software, which can be installed on a computer or directly on the R&S RTO/RTO6/RTP.

2.1.1 Soldering guide for modular probes

All single-ended signals such as ADD, CMD, DQ, DM, CS, CKE should be soldered in such a way that the signal is connected to the + part on the probe tip. The ground of the signal is connected to the - part on the same probe tip.

All differential signals such as CK, DQS should be soldered differentially:

- The + signal is connected to the + part on the probe tip.
- The - signal is connected to the - part on the same probe tip.
- The ground of the signal is connected to the ground of the same probe tip.

2.2 Installing software and license

The preparation steps are performed only once for each computer and instrument that are used for testing.

Uninstall older versions of the R&S ScopeSuite

If an older version of the R&S ScopeSuite is installed, make sure to uninstall the old version before you install the new one. You can find the version number of the current installation in "Help" menu > "About". To uninstall the R&S ScopeSuite, use the Windows " Control Panel" > "Programs".

For best operation results, we recommend that the installed firmware versions of the R&S ScopeSuite and the oscilloscope are the same.

To install the R&S ScopeSuite

1. Download the latest R&S ScopeSuite software from the "Software" section on the Rohde & Schwarz R&S RTO/RTO6/RTP website:
   www.rohde-schwarz.com/product/rtp.html
   www.rohde-schwarz.com/product/rto.html
2. Install the R&S ScopeSuite software:
   - On the computer that is used for testing, or
   - On the R&S RTO/RTO6/RTP.

   For system requirements, refer to the Release Notes.

To install the license key on the R&S RTO/RTO6/RTP

► When you got the license key of the compliance test option, enable it on the oscilloscope using [Setup] > "SW Options".
For a detailed description, refer to the R&S RTO/RTO6/RTP user manual, chapter "Installing Options", or to the online help on the instrument.

2.3 Setting up the network

If the R&S ScopeSuite software runs on a test computer, the computer and the testing oscilloscope require a LAN connection.

There are two ways of connection:

- LAN (local area network): It is recommended that you connect to a LAN with DHCP server. This server uses the Dynamic Host Configuration Protocol (DHCP) to assign all address information automatically.
- Direct connection of the instruments and the computer or connection to a switch using LAN cables: Assign fixed IP addresses to the computer and the instruments and reboot all devices.

To set up and test the LAN connection

1. Connect the computer and the instruments to the same LAN.
2. Start all devices.
3. If no DHCP server is available, assign fixed IP addresses to all devices.
4. Ping the instruments to make sure that the connection is established.
5. If VISA is installed, check if VISA can access the instruments.
   a) Start VISA on the test computer.
   b) Validate the VISA address string of each device.

See also:

- Chapter 2.5, "Connecting the R&S RTO/RTO6/RTP", on page 11

2.4 Starting the R&S ScopeSuite

To start the R&S ScopeSuite on the test computer or on the oscilloscope:

► Double-click the R&S ScopeSuite program icon.

To start the R&S ScopeSuite on the instrument, in the R&S RTO/RTO6/RTP firmware:

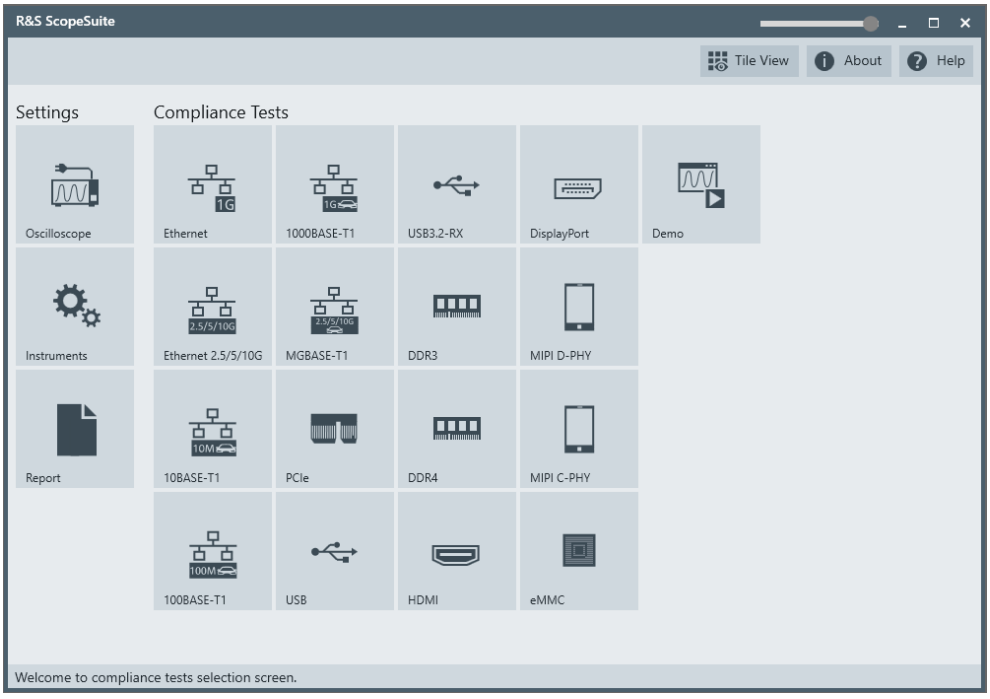
► In the "Apps" dialog, open the "Compliance" tab.

2.5 Connecting the R&S RTO/RTO6/RTP

If the R&S ScopeSuite is installed directly on the instrument, the software detects the R&S RTO/RTO6/RTP firmware automatically, and the "Oscilloscope" button is not available in the R&S ScopeSuite.

If the R&S ScopeSuite software runs on a test computer, the computer and the testing oscilloscope require a LAN connection, see Chapter 2.3, "Setting up the network", on page 10. The R&S ScopeSuite software needs the IP address of the oscilloscope to establish connection.

1. Start the R&S RTO/RTO6/RTP.
2. Start the R&S ScopeSuite software.
3. Click "Settings" > "Oscilloscope".

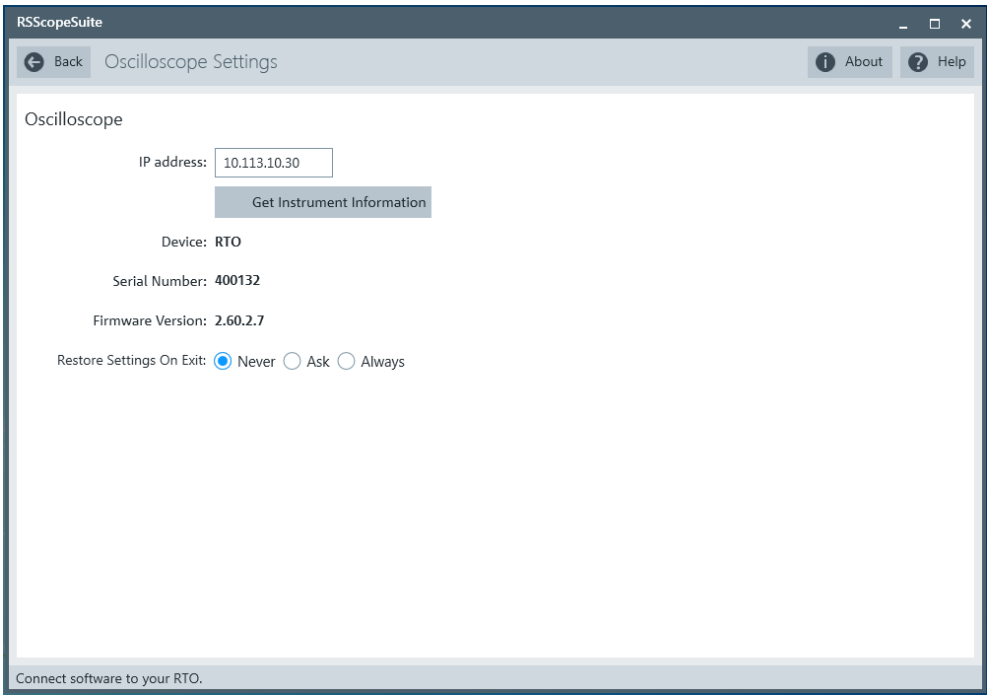


4. Enter the IP address of the oscilloscope.

To obtain the IP address: press the Rohde & Schwarz logo at the top-right corner of the oscilloscope's display.

5. Click "Get Instrument Information".

   The computer connects with the instrument and gets the instrument data.

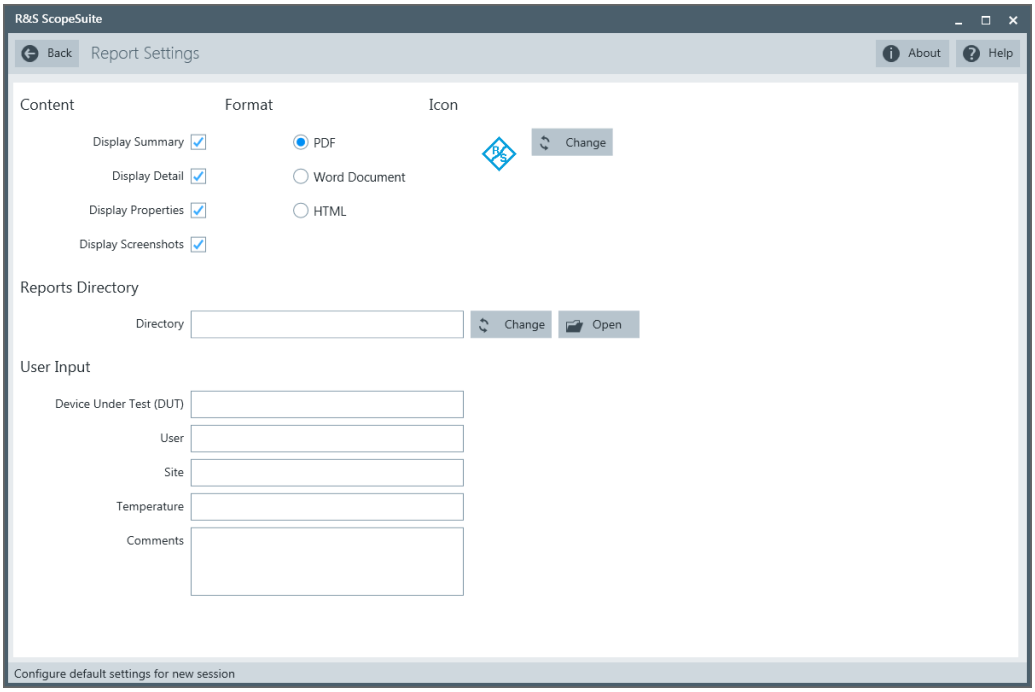


If the connection fails, an error message is shown.

2.6 Report configuration

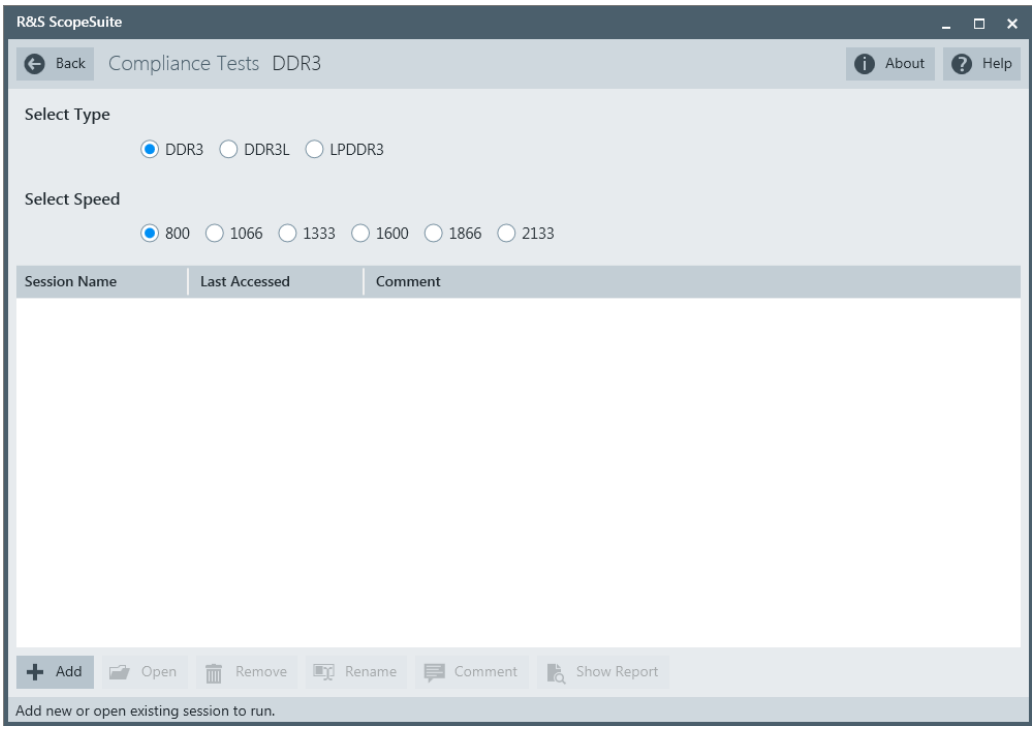
In the "Report Configuration" menu, you can select the format of the report and the details to be included in the report. You can also select an icon that is displayed in the upper left corner of the report.

Also, you can enter common information on the test that is written in the "General Information" section of the test report.


R&S ScopeSuite
Back
Report Settings
About
Help
Content
Format
Icon
Display Summary
Display Detail
Display Properties
Display Screenshots
PDF
Word Document
HTML
Change
Reports Directory
Directory
Change
Open
User Input
Device Under Test (DUT)
User
Site
Temperature
Comments
Configure default settings for new session

3 Performing tests

3.1 Starting a test session



After you open a compliance test, the "Session Selection" dialog appears. In this dialog, you can create new sessions, open or view existing report.

The following functions are available for handling test sessions:

Function	Description
"Add"	Adds a new session
"Open"	Opens the selected session
"Remove"	Removes the selected session
"Rename"	Changes the "Session Name"
"Comment"	Adds a comment
"Show report"	Generates a report for the selected session

To add a test session

1. In the R&S ScopeSuite window, select the compliance test.
2. In the "Session Selection" dialog press "Add".
3. If necessary change the "Session Name"

To open a test session

1. In the R&S ScopeSuite window, select the compliance test.
2. In the "Session Selection" dialog, select the session you want to open and double click on it.
   Alternatively, select the session and press "Open".

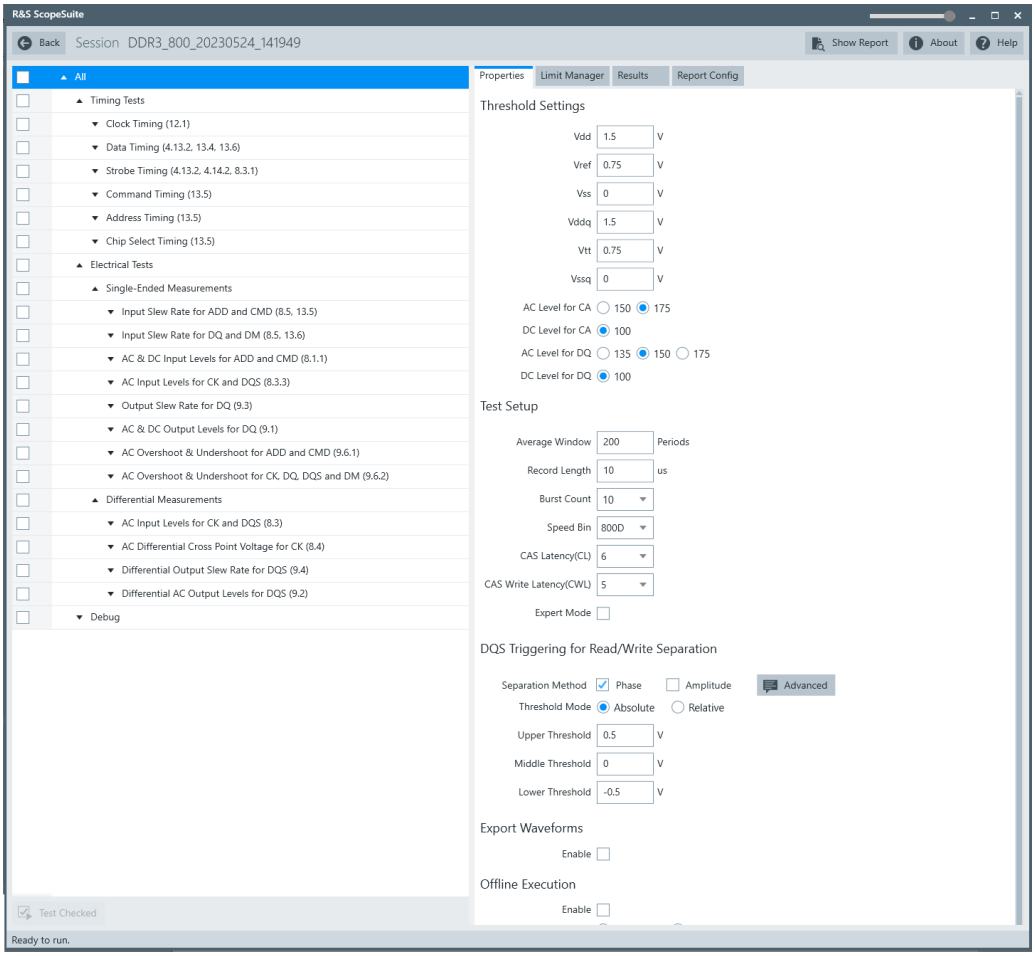
To show a report for a test session

1. In the R&S ScopeSuite window, select the compliance test.
2. In the "Session Selection" dialog, select the session you want the report for and press "Show report".

3.2 Configuring the test

1. In the R&S ScopeSuite window, select the compliance test to be performed:
   - "DDR3"
2. Open a test session, see Chapter 3.1, "Starting a test session", on page 14.
3. Adjust the "Properties" settings for the test cases you want to perform.
4. Click "Limit Manager" and edit the limit criteria, see Chapter 3.2.1.1, "Limit manager", on page 17.
5. If you want to use special report settings the "Report Config" tab to define the format and contents of the report. Otherwise the settings defined in "RSScopeSuite" > "Settings" > "Report" are used. See Chapter 2.6, "Report configuration", on page 12.
6. Click "Test Checked"/"Test Single" and proceed as described in the relevant test case chapter.

3.2.1 General test settings



Each session dialog is divided into several sections:

- "Properties": shows the settings that can be made for the test case selected on the left side of the dialog. You can differentiate between the "All" and the sub test properties
  In the "All" > "Properties" tab you can configure the settings for all test cases in the current session. Once you change and save a setting in this tab, the changes will be done for all test in the sessions. At the same time, there will be a special marking for the functions that have different settings for different sub tests.
- "Limit Manager": sets the measurement limits that are used for compliance testing, see Chapter 3.2.1.1, "Limit manager", on page 17.
- "Results": shows an overview of the available test results for this session.
- "Instruments": defines instruments settings for connecting to external devices, that are specific for this test session.
  When a session is first created the global settings ("RSScopeSuite" > "Settings" > "Instruments") are copied to the session. This "Instruments" tab can be used to change those copied defaults.
- "Report Config": defines the format and contents of the report for this session.

When a session is first created the global settings ("RSScopeSuite" > "Settings" > "Report") are copied to the session. This "Report Config" tab can be used to change those copied defaults.

- "Test Checked"/ "Test Single": starts the selected test group.

3.2.1.1 Limit manager

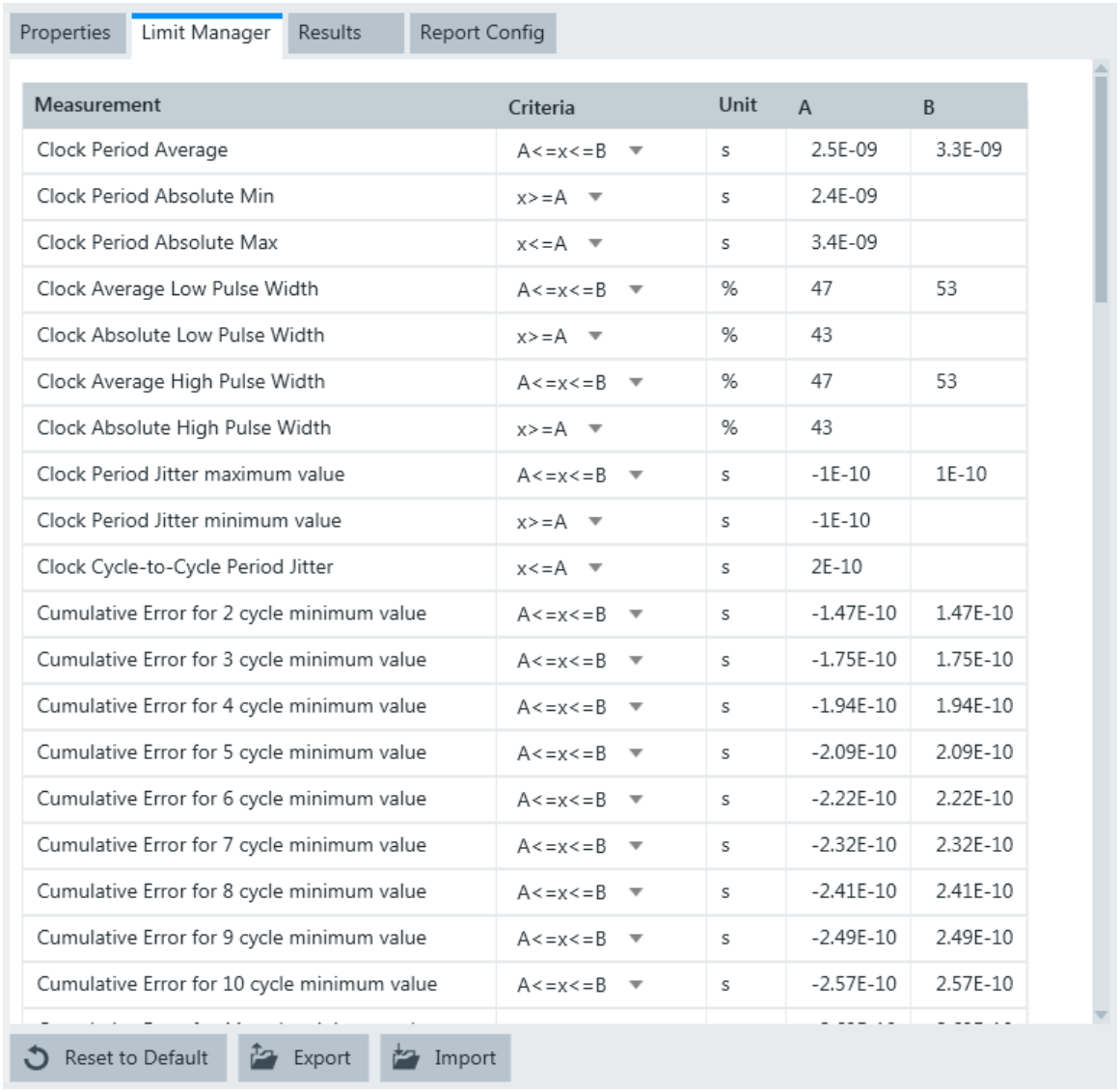
The "Limit Manager" shows the measurement limits that are used for compliance testing.

Each limit comprises the comparison criterion, the unit, the limit value A, and a second limit value B if the criterion requires two limits.

You can set the values to defaults, change the values in the table, export the table in xml format, or import xml files with limit settings.

You can also return the values to the original limits with "Reset to default".

► Check and adjust the measurement limits.



3.2.2 Test configuration for DDR3

The test configuration consists of some test-specific configuration settings. The values for the settings in this tab depend on the selected "Speed" and "Type" of standard.

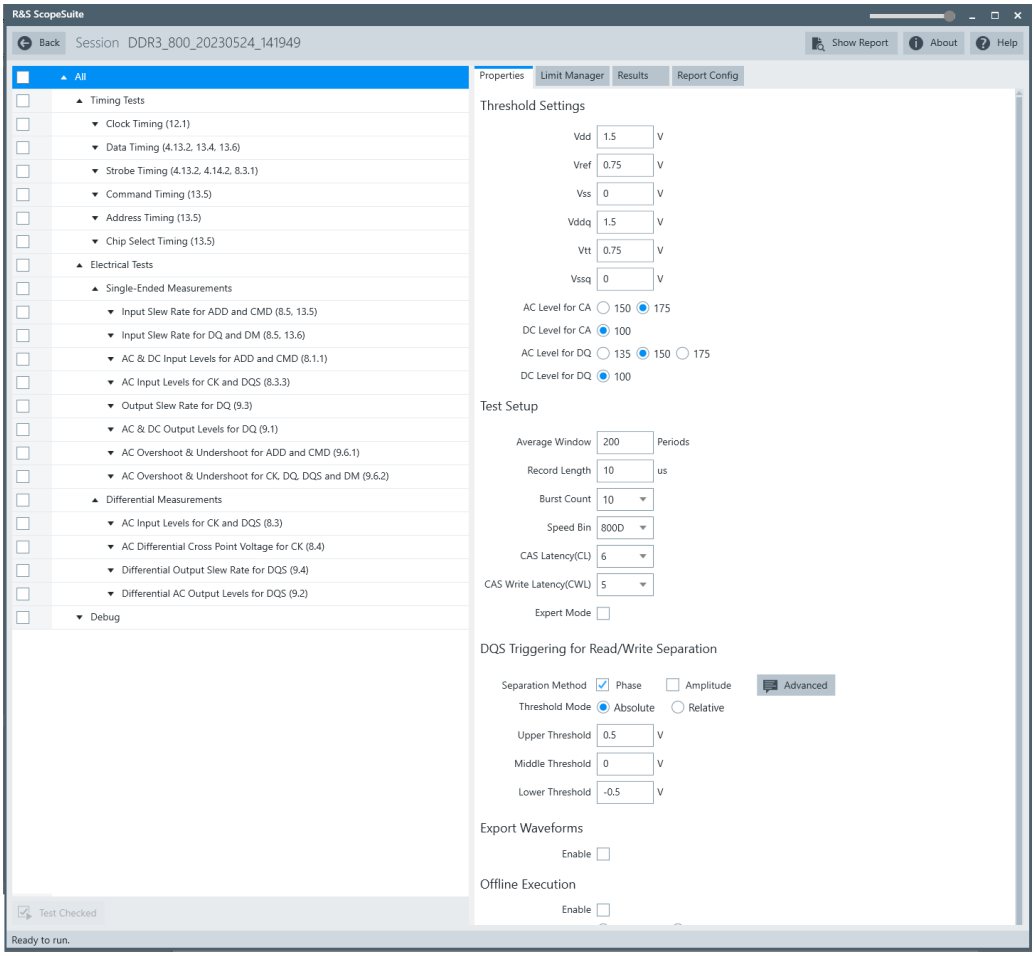


Figure 3-1: Configuration for DDR3 compliance tests

Signals
Selects the channel for the specified signal.

For electrical tests consider also how many test signals are enabled. For example, if only the ADD/CMD signal is selected, only ADD/CMD signal is used to run the test. If both the ADD and the CMD signals are selected, test is run using ADD signal first, followed by the CMD signal.

Additionally, for some test cases "Invert" is available. To invert means to reflect the voltage values of all signal components against the ground level.

You can use inversion, for example, to switch the polarity of a differential signal without changing the probe connections.

The following signals are available according to the selected test case:

"ADD"	Address signal.
"CMD"	Command signal.
"CK"	Differential clock input signal.
"DQS"	Data strobe signal.
"DQ"	Data input/output signal.

"DM" Data mask signal.

"CS" Chip select signal.

"CKE" Clock enable signal.

Threshold Settings
The following threshold settings are defined:

"V_{DD}" Power Supply: 1.5 V +/- 0.075 V

"V_{REF}" Reference voltage

"V_{SS}" Ground

"V_{DDQ}" DQ Power Supply: 1.5 V +/- 0.075 V

"V_{TT}" $V_{TT} = V_{DDQ}/2$

"V_{SSQ}" DQ Ground

"AC Level for CA"
AC level for the command address.

"DC Level for CA"
DC level for the command address.

"AC Level for DQ"
AC level for the data input/output signal.

"DC Level for DQ"
DC level for the data input/output signal.

Average Window
Sets the average window in periods.

Record Length
Sets the number of waveform samples in one waveform record.

Burst Count
Sets the burst count.

Speed Bin
Selects which speed bin is used for the tests.

CAS Latency (CL)
Selects the value for the CAS latency. This is the delay, measured in clock cycles, between the internal read command and the availability of the first bit of output data.

CAS Write Latency (CWL)
Selects the value for the CAS write latency. This is the delay, measured in clock cycles, between the internal write command and the availability of the first bit input data.

Separation method
Selects the separation method.

"Phase" Checks the phase difference between DQ and DQS to differentiate the type (read or write) of burst.

"Amplitude" Checks the peak-peak amplitude difference between read and write signals on DQS to differentiate the type (read or write) of burst.

"Advanced" Enables the definition of more detailed trigger conditions:

- "Min Phase for Read"/"Max Phase for Read": sets the minimum/ maximum phase for the read burst.
- "Min Phase for Write"/"Max Phase for Write": sets the minimum/ maximum phase for the write burst.
- "Amplitude Relationship": sets the amplitude relationship between the read and write burst.
- "P-P Amplitude Threshold": sets the peak-peak amplitude threshold.

Threshold Mode
Selects between the absolute and relative threshold mode.

Upper/Middle/Lower Threshold ← Threshold Mode
Sets the upper/middle/lower for the absolute threshold mode.

Top/Middle/Base Ratio ← Threshold Mode
Set the top/middle/base ratio for the relative threshold mode.

Export Waveforms
Enables you to export a waveform. You can later load the waveforms to run the tests in the offline mode, see Offline Execution.

You can define an export directory, or use the default one:

```
MyDocuments\Rohde-Schwarz\RSScopeSuite\<Version>\Waveforms\
<ComplianceTest>\<SubTest>\<Speed>\<SessionName>
```

For example:

```
MyDocuments\Rohde-Schwarz\RSScopeSuite\4.10.0\Waveforms\DDR3\
DDR3\1333\DDR3_1333_20180413_144116
```

Offline Execution

If enabled, allows you to use exported waveforms as a source for the execution of the compliance test.

You can select one waveform for each needed signal.

3.3 Initiating the test

To perform compliance tests, the device under test is connected to the test board in a test-specific way. Using a probe, the test board is connected with the R&S RTO/RTO6/RTP. The probe connections are test-specific. The R&S ScopeSuite guides you step-by-step through the connection setup and the test sequence.

1. Set the test setup on a nonconductive, static-approved work surface.
2. In the R&S ScopeSuite window, select the compliance test.
3. Open a test session, see Chapter 3.1, "Starting a test session", on page 14.
4. Check the test configuration settings and adjust, if necessary. See: Chapter 3.2, "Configuring the test", on page 15.

5. Click "Test Checked" for starting all checked test cases or "Test Single" for starting only the selected test case.

   The R&S ScopeSuite test wizard explains the following individual setup steps. A detailed test description can be found in the following chapters:
   - Chapter 3.5, "Starting DDR3 Tests", on page 24

3.4 Getting test results

For each test, the test data - report, diagrams and waveform files - is saved in the following folder:

```
%ProgramData%\Rohde-Schwarz\RSScopeSuite2\<version>\Sessions\DDR3\
<Session_Name>
```

If you resume an existing session, new measurements are appended to the report, new diagrams and waveform files are added to the session folder. Existing files are not deleted or replaced. Sessions data remain until you delete them in the "Results" tab of the session.

The report format can be defined in "RSScopeSuite" > "Settings" > "Report" for all compliance tests (see also Chapter 2.6, "Report configuration", on page 12). If you want to use special report settings for a session, you can define the format and contents of the report in the "Report Config" tab of the session.

All test results are listed in the "Results" tab. Reports can be provided in PDF, MSWord, or HTML format. To view and print PDF reports, you need a PDF viewer, for example, the Acrobat Reader.

The test report file can be created at the end of the test, or later in the "Session Selection" dialog.

To show a test report

1. In the R&S ScopeSuite window, select the compliance test to be performed.
2. Select the session name in the "Session Selection" dialog and click "Show report".

   The report opens in a separate application window, depending on the file format. You can check the test results and print the report.

To delete the results, diagrams and waveform files of a session

1. In the "Session Selection" dialog select the session and open it.
2. In the "Results" tab, select the result to be deleted.
3. Click "Remove".

3.5 Starting DDR3 Tests

Before you run the test, complete the following actions:

- LAN connection of the oscilloscope and the computer running the R&S ScopeSuite, see Chapter 2.5, "Connecting the R&S RTO/RTO6/RTP", on page 11

1. Select "DDR3" in the R&S ScopeSuite start window.
2. In the "Session Selection" dialog, set the "Select Type" standard. The following "Types" are available:
   - "DDR3": Double data rate type three. Used for desktops and servers.
   - "DDR3L": DDR3 low voltage. It is used in laptops and low power PCs.
   - "LPDDR3": low power DDR3. Consumes very low power and is used for mobile phones.
3. Set the "Select Speed". There are preset speeds you can select from: "800"/"1066"/"1333"/"1600"/"1866"/"2133"
4. Add a new test session. Open it, see Chapter 3.1, "Starting a test session", on page 14.
5. Check the test configuration settings. Adjust, if necessary. See:
   - Chapter 3.2.2, "Test configuration for DDR3", on page 18
   - Chapter 3.2.1.1, "Limit manager", on page 17
6. Select/check the test cases you want to run and click "Test Single"/"Test checked".
7. A step-by step guide explains the following individual setup steps. When you have finished all steps of the step-by-step guide, the compliance test runs automatically.

4 Timing tests

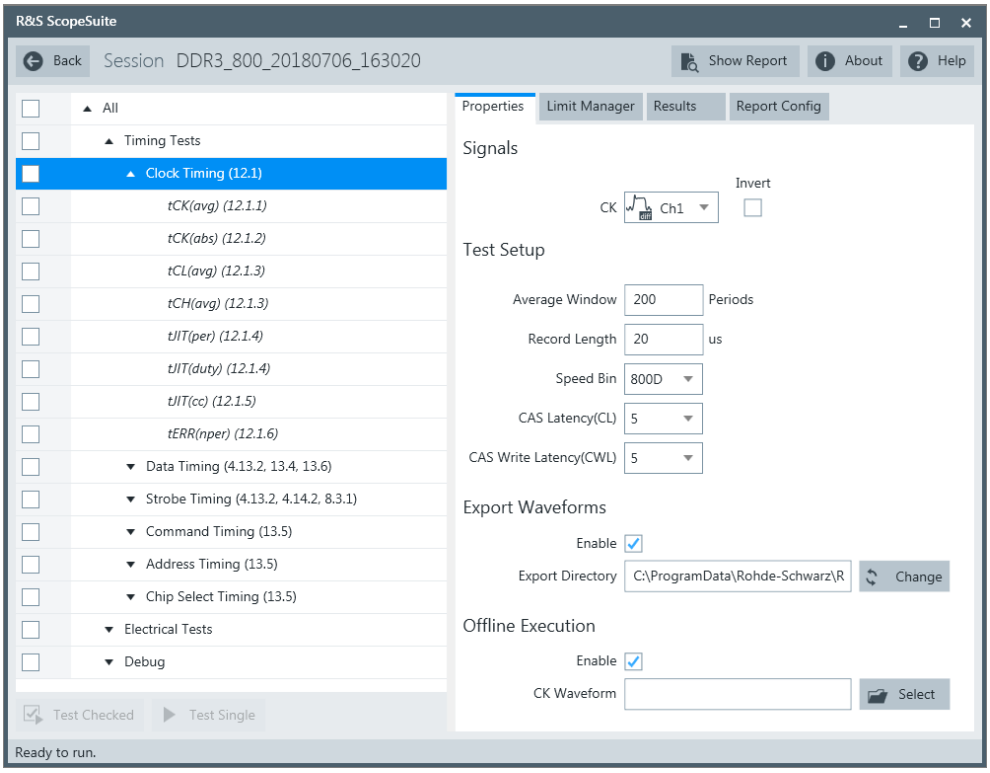
4.1 Clock timing

4.1.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	1
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	1
DUT	DDR3 device that supports the selected type	1

4.1.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Timing Tests" > "Clock Timing".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

4.1.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

4.1.4 Measurements

The clock timing measurements consist of up to eight measurements. They test the limits as defined in the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/ JESD209-3C(LPDDR3) specifications.

4.1.4.1 Average clock period - $t_{CK(avg)}$

This test aims to verify that the average clock period tCK(avg) is within the limits defined in section 12.1.1 (DDR3/DDR3L)/ 11.1.1 (LPDDR3) of the specification. This is the average clock period calculated across any consecutive 200 cycle window. The clock period is defined from rising edge to rising edge.

4.1.4.2 Absolute clock period - $t_{CK(abs)}$

This test aims to verify that the average absolute clock period tCK(abs) is within the limits defined in section 12.1.2 (DDR3/DDR3L)/ 11.1.2 (LPDDR3) of the specification. This is the absolute clock period from one rising edge to the next rising edge.

4.1.4.3 Average low pulse width - $t_{CL(avg)}$

This test aims to verify that the average low pulse width tCL(avg) is within the limits defined in section 12.1.3 (DDR3/DDR3L)/ 11.1.3 (LPDDR3) of the specification. This is the average low pulse width, as calculated across any consecutive 200 low pulses.

4.1.4.4 Average high pulse width - $t_{CH(avg)}$

This test aims to verify that the average high pulse width tCL(avg) is within the limits defined in section 12.1.3 (DDR3/DDR3L)/ 11.1.3 (LPDDR3) of the specification. This is the average low pulse width, as calculated across any consecutive 200 low pulses.

4.1.4.5 Clock period jitter - $t_{JIT(per)}$

This test aims to verify that the clock period jitter tJIT(per) is within the limits defined in section 12.1.4 (DDR3/DDR3L)/ 11.1.4 (LPDDR3) of the specification. It is the largest deviation of any signal t_{CK} from $t_{CK(avg)}$. It defines the single period jitter when the DLL is already locked.

4.1.4.6 Half period jitter - $t_{JIT(duty)}$

This test aims to verify that the half period jitter tJIT(duty) is within the limits defined in section 12.1.4 (DDR3/DDR3L)/ 11.1.4 (LPDDR3) of the specification. This is the largest deviation of any signal t_{CK} from $t_{CK(avg)}$.

4.1.4.7 Cycle to cycle period jitter - $t_{JIT(cc)}$

This test aims to verify that the cycle to cycle period jitter tJIT(cc) is within the limits defined in section 12.1.5 (DDR3/DDR3L)/ 11.1.5 (LPDDR3) of the specification. This is the absolute difference in clock period between two consecutive clock cycles. It defines the cycle to cycle jitter when the DLL is already locked.

4.1.4.8 Cumulative error - $t_{ERR(nper)}$

This test aims to verify that the cumulative error tERR(nper) is within the limits defined in section 12.1.6 (DDR3/DDR3L)/ 11.1.6 (LPDDR3) of the specification. This is the cumulative error across n multiple consecutive cycles from tCK(avg).

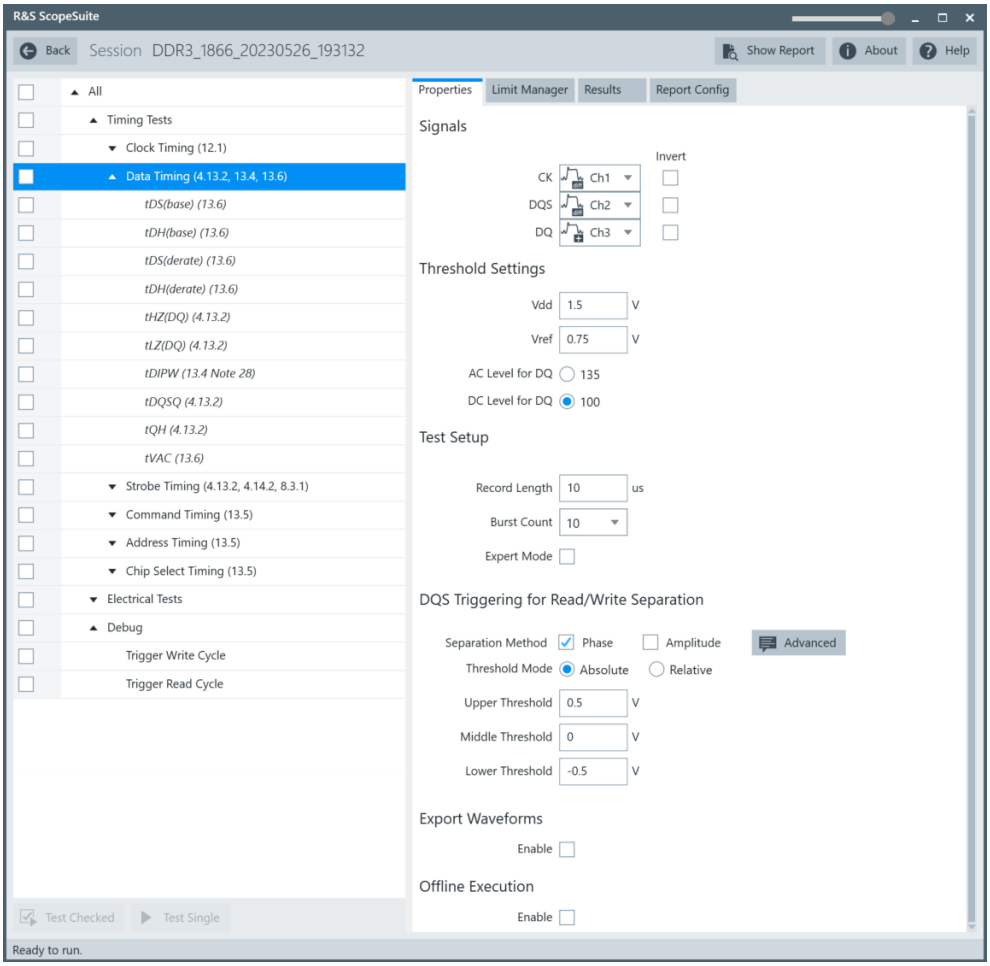
4.2 Data timing

4.2.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	3
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	3
DUT	DDR3 device that supports the selected type	1

4.2.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Timing Tests" > "Data Timing".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

4.2.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

4.2.4 Measurements

The data timing measurements consist of up to 10 measurements. They test the limits as defined in the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/ JESD209-3C(LPDDR3) specifications.

4.2.4.1 Differential DQ and DM input setup time- $t_{DS(base)}$

This test aims to verify that time interval from the data or data mask (DQ/DM rising/ falling edge) setup time to the associated DQS crossing edge is within the limits defined in section 13.6 of the specification.

4.2.4.2 Differential DQ and DM input hold time - $t_{DH(base)}$

This test aims to verify that the time interval from the data or data mask (DQ/DM rising/ falling edge) hold time to the associated DQS crossing edge is within the limits defined in section 13.6 of the specification.

4.2.4.3 Differential DQ and DM input setup time with derating support - $t_{DS-Diff(derate)}$

This test aims to verify that the time interval from data or data mask (DQ/DM rising/ falling edge) setup time to the associated DQS crossing is within the limits defined in section 13.6 of the specification.

4.2.4.4 Differential DQ and DM input hold time with derating support - $t_{DH-Diff(derate)}$

This test aims to verify that the time interval from data or data mask (DQ/DM rising/ falling edge) hold time to the associated DQS crossing is within the limits defined in section 13.6 of the specification.

4.2.4.5 DQ out high impedance time from CK/CK# - $t_{HZ(DQ)}$

This test aims to verify that the data high impedance time from CK/CK# is within the limits defined in section 4.13.2 of the specification.

4.2.4.6 DQ Low-impedance time from CK/CK# - $t_{LZ(DQ)}$

This test aims to verify that the data low impedance time from CK/CK# is within the limits defined in section 4.13.2 of the specification.

4.2.4.7 Data input pulse width - t_{DIPW}

This test aims to verify that the data and mask input pulse width for each input is within the limits defined in section 13.4 Note 28 of the specification.

4.2.4.8 DQS-DQ skew for DQS and associated DQ signals - t_{DQSQ}

This test aims to verify that the strobe to data skew, per group, per access is within the limits defined in section 4.13.2 of the specification.

4.2.4.9 DQ/DQS output hold time from DQS - t_{QH}

This test aims to verify that the data output hold time from strobe is within the limits defined in section 4.13.2 of the specification.

4.2.4.10 t_{VAC} time above $V_{IH(ac)}$ $V_{IL(ac)}$

This test aims to verify that t_{VAC} is within the limits defined in the specification. This is the time to remain above/below $V_{IH(AC)}$/$V_{IL(AC)}$ for a data transition to be considered as valid.

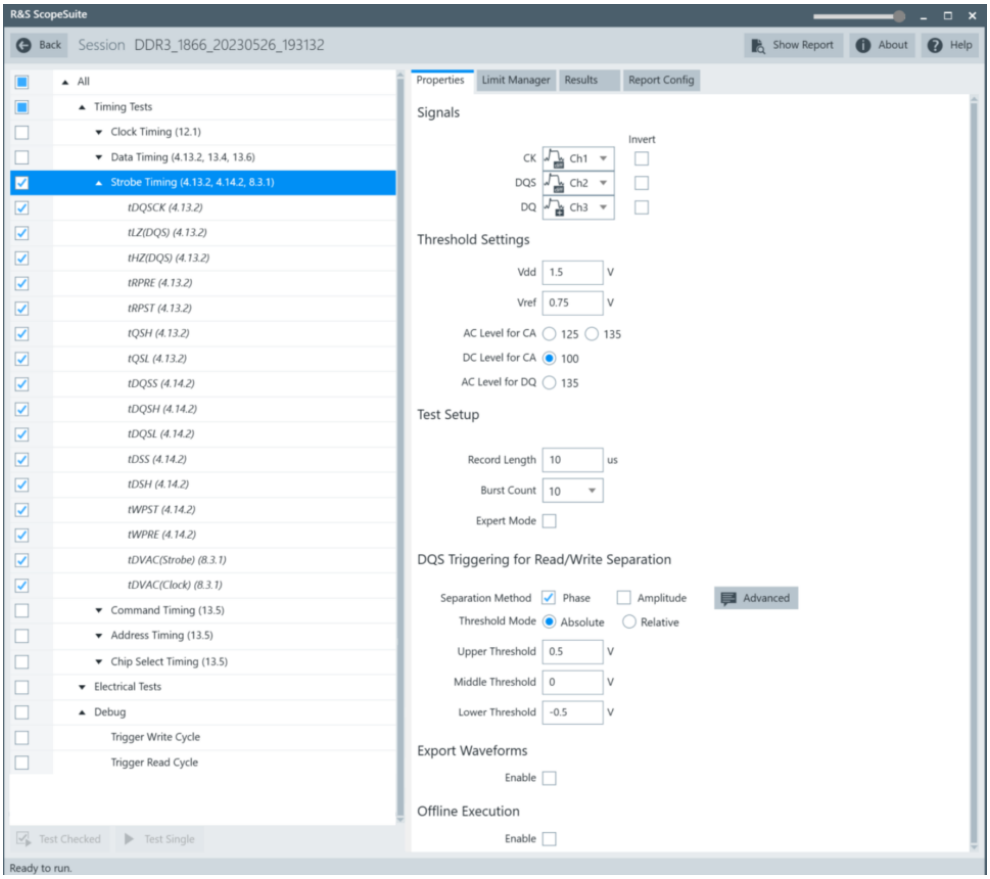
4.3 Strobe timing

4.3.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	3
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	3
DUT	DDR3 device that supports the selected type	1

4.3.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Timing Tests" > "Strobe Timing".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

4.3.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

4.3.4 Measurements

The strobe measurements consist of up to 10 measurements. They test the limits as defined in the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/JESD209-3C(LPDDR3) specifications.

4.3.4.1 DQS output access time from CK/CK # - t_{DQSCK}

This test aims to verify that the strobe rising edge output access time from rising CK/CK# is within the limits defined in section 4.13.2 of the specification.

4.3.4.2 Low-impedance time from CK/CK# - t_{LZ}

This test aims to verify that the strobe low-impedance time is within the limits defined in section 4.13.2 of the specification.

4.3.4.3 High-impedance time from CK/CK# - t_{HZ}

This test aims to verify that the strobe high-impedance time is within the limits defined in section 4.13.2 of the specification.

4.3.4.4 Differential read preamble - t_{RPRE}

This test aims to verify that the strobe differential READ preamble is within the limits defined in section 4.13.2 of the specification.

4.3.4.5 Read postamble - t_{RPST}

This test aims to verify that the strobe differential READ postamble is within the limits defined in section 4.13.2 of the specification.

4.3.4.6 Differential output high time - t_{QSH}

This test aims to verify that the strobe differential output high time is within the limits defined in section 4.13.2 of the specification.

4.3.4.7 Differential output low time - t_{QSL}

This test aims to verify that the strobe differential output low time is within the limits defined in section 4.13.2 of the specification.

4.3.4.8 DQS latching transition to associated clock edge - t_{DQSS}

This test aims to verify that the time interval from the strobe rising edge to CK/CK# rising edge is within the limits defined in section 4.14.2 of the specification.

4.3.4.9 DQS input high pulse width - t_{DQSH}

This test aims to verify that the strobe differential input high pulse width is within the limits defined in section 4.14.2 of the specification.

4.3.4.10 DQS input low pulse width - t_{DQSL}

This test aims to verify that the strobe differential input low pulse width is within the limits defined in section 4.14.2 of the specification.

4.3.4.11 DQS falling edge to CK setup time - t_{DSS}

This test aims to verify that the time interval from the strobe falling edge setup time to the CK/CK# rising edge is within the limits defined in section 4.14.2 of the specification.

4.3.4.12 DQS falling edge hold time from CK - t_{DSH}

This test aims to verify that the strobe falling edge hold time from CK/CK# rising edge is within the limits defined in section 4.14.2 of the specification.

4.3.4.13 Write postamble - t_{WPST}

This test aims to verify that the strobe differential WRITE postamble is within the limits defined in section 4.14.2 of the specification.

4.3.4.14 Write preamble - t_{WPRE}

This test aims to verify that the strobe differential WRITE preamble is within the limits defined in section 4.14.2 of the specification.

4.3.4.15 Time before ringback - $t_{DVAC(Strobe)}$

This test aims to verify that the time before ringback for strobe is within the limits defined in section 8.3.1 of the specification. This is the "time above AC-level" during a differential AC-swing.

4.3.4.16 Time before ringback - $t_{DVAC(Clock)}$

This test aims to verify that the time before ringback for CK /CK# is within the limits defined in section 8.3.1 of the specification. This is the "time above AC-level" during a differential AC-swing.

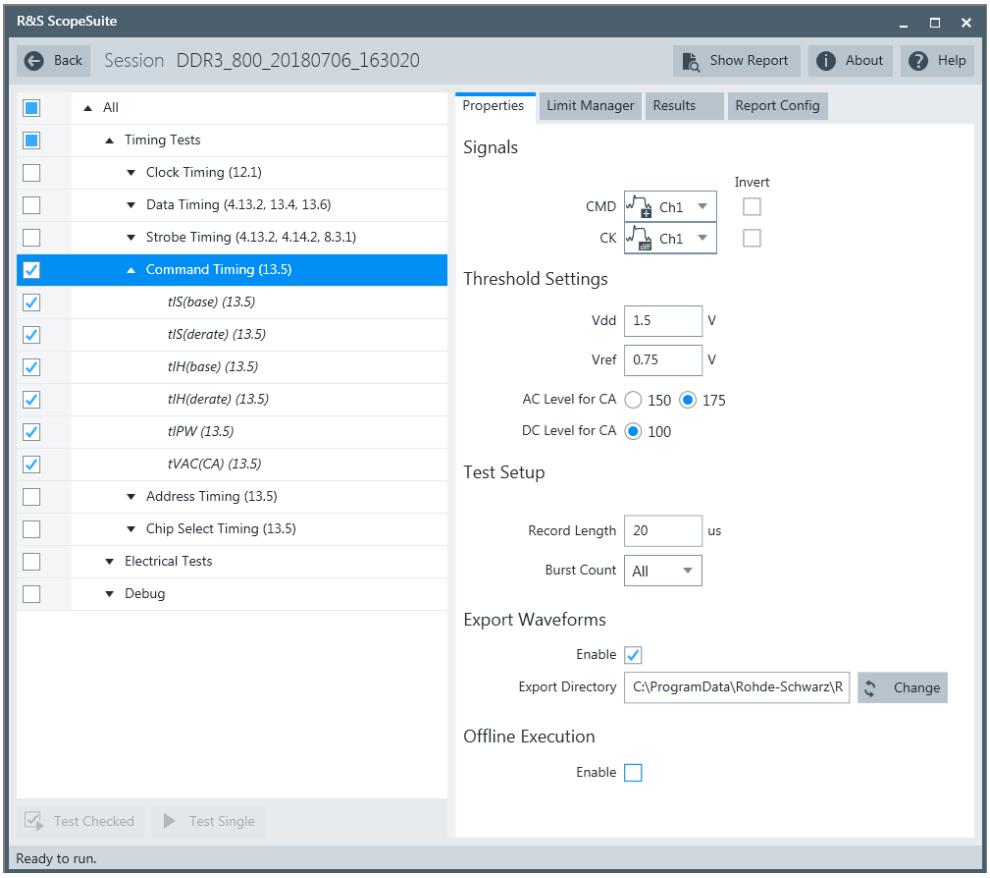
4.4 Command timing

4.4.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

4.4.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Timing Tests" > "Command Timing".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

4.4.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

4.4.4 Measurements

The command timing measurements consist of up to six measurements. They test the limits as defined in section 13.5 (DDR3/DDR3L)/ 4.2 (LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/JESD209-3C(LPDDR3) specifications.

4.4.4.1 Address and control input setup time - t_{IS}

This test aims to verify that the command and address setup time from CK/CK# is within the limits defined in the specification.

4.4.4.2 Address and control input setup time with derating support - $t_{IS\ (Derated)}$

This test aims to verify that the command and address setup time from CK/CK# is within the limits defined in the specification.

4.4.4.3 Address and control input hold time - t_{IH}

This test aims to verify that the command and address hold time from CK/CK# is within the limits defined in the specification.

4.4.4.4 Address and control input hold time with derating support - $t_{IH\ (Derated)}$

This test aims to verify that the command and address hold time from CK/CK# is within the limits defined in the specification.

4.4.4.5 Address and control input pulse width t_{IPW}

This test aims to verify that the control and address input pulse width for each input is within the limits defined in the specification.

4.4.4.6 $t_{VAC\ (CA)}$

This test aims to verify that $t_{VAC\ (CA)}$ is within the limits defined in the specification. This is the time to remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for a command transition to be considered as valid.

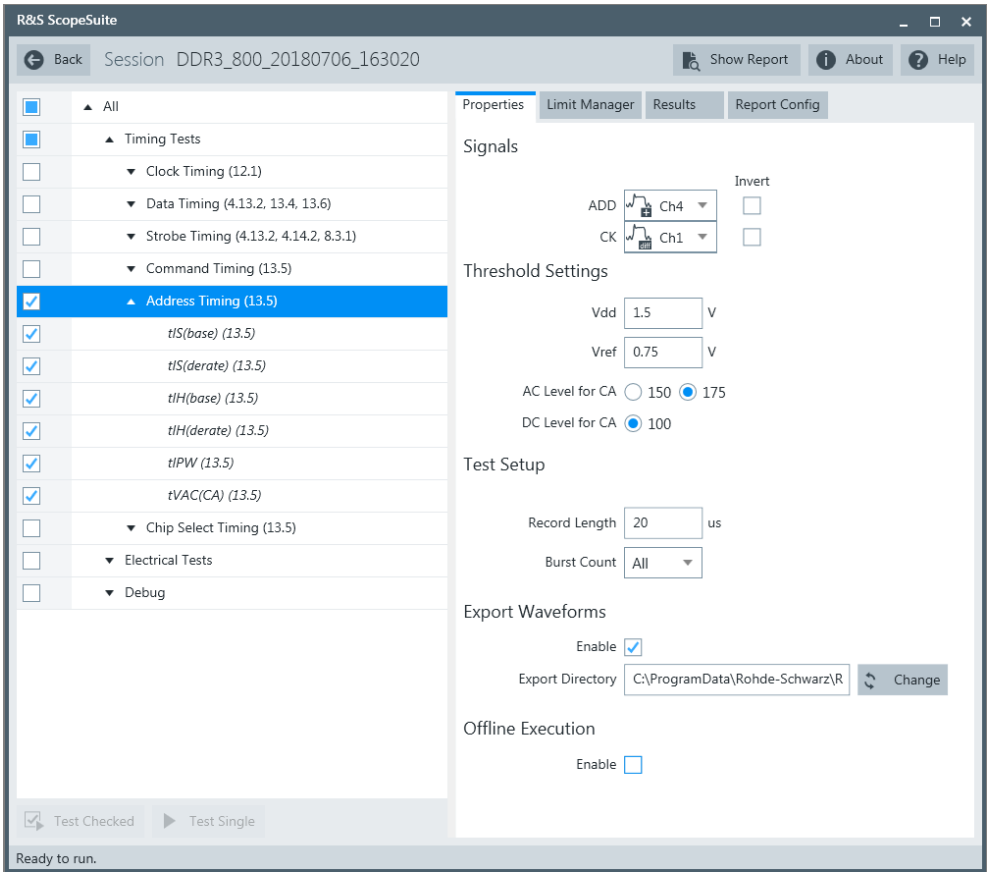
4.5 Address timing

4.5.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

4.5.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Timing Tests" > "Address Timing".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

4.5.3 Measurements

The address timing measurements consist of up to six measurements. They test the limits as defined in section 13.5 (DDR3/DDR3L)/ 4.2 (LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/JESD209-3C(LPDDR3) specifications.

For details on the measurements, see Chapter 4.4.4, "Measurements", on page 37.

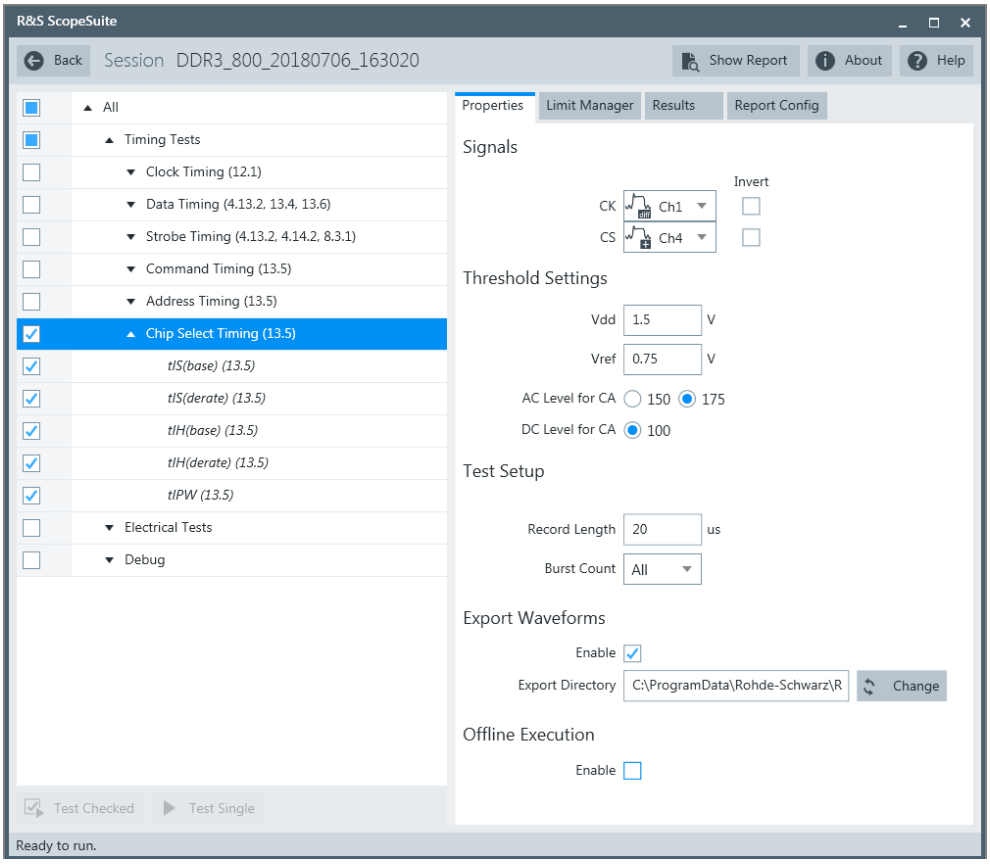
4.6 Chip select timing

4.6.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

4.6.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Timing Tests" > "Chip Select Timing".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

4.6.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

4.6.4 Measurements

The chip select timing measurements consist of up to six measurements. They test the limits as defined in section 13.5 (DDR3/DDR3L)/ 4.2 (LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/JESD209-3C(LPDDR3) specifications.

4.6.4.1 Address and control input setup time - t_{IS}

This test aims to verify that the chip select setup time from CK/CK# is within the limits defined in the specification.

4.6.4.2 Address and control input setup time with derating support - t_{IS} (derated)

This test aims to verify that the chip select setup time from CK/CK# is within the limits defined in the specification.

4.6.4.3 Address and control input hold time - t_{IH}

This test aims to verify that the chip select hold time from CK/CK# is within the limits defined in the specification.

4.6.4.4 Address and control input hold time with derating support - t_{IH} (derated)

This test aims to verify that the chip select hold time from CK/CK# is within the limits defined in the specification.

4.6.4.5 t_{IPW}

This test aims to verify that the chip select input pulse width for each input is within the limits defined in the specification.

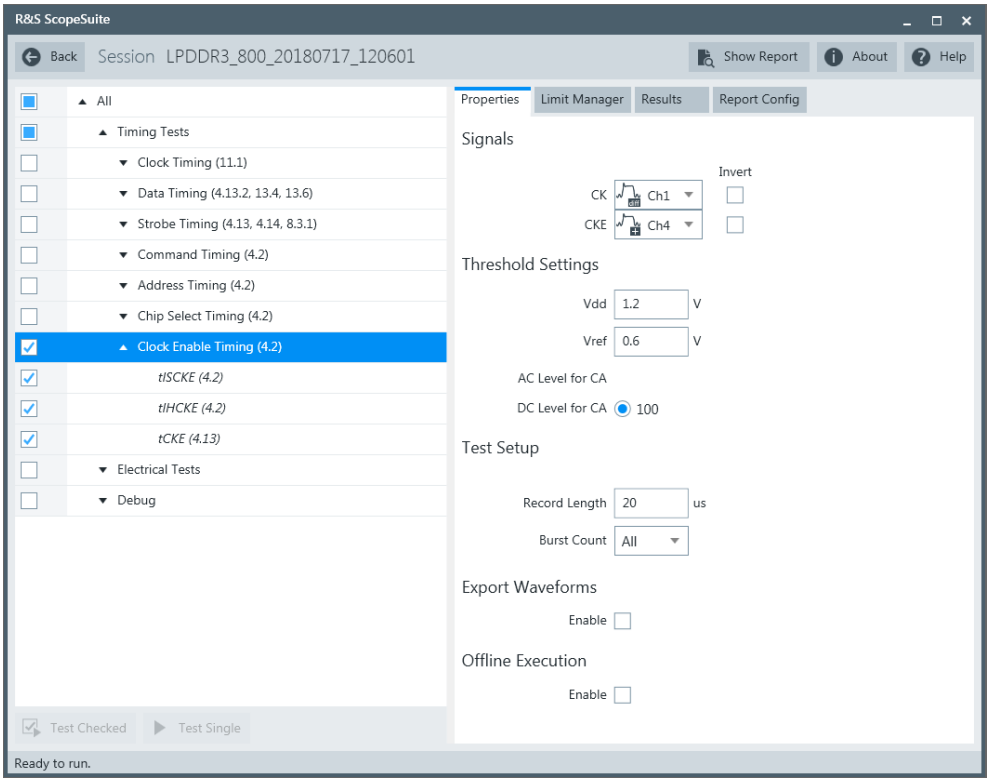
4.7 Clock enable timing

4.7.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

4.7.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Timing Tests" > "Clock Enable Timing".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

4.7.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

4.7.4 Measurements

The clock enable timing measurements consist of up to three measurements. They test the limits as defined in the JESD209-3C(LPDDR3) specification.

4.7.4.1 Clock enable input setup time - t_{ISCKE}

This test aims to verify that the clock enable input setup time from CKE is within the limits defined in section 4.2 of the specification.

4.7.4.2 Clock enable input hold time - t_{IH}

This test aims to verify that the clock enable hold time from CKE is within the limits defined in section 4.2 of the specification.

4.7.4.3 Clock enable minimum pulse width t_{CKE}

This test aims to verify that the minimum pulse width for each input is within the limits defined in section 4.13 of the specification.

5 Electrical tests

5.1 Single-ended signals

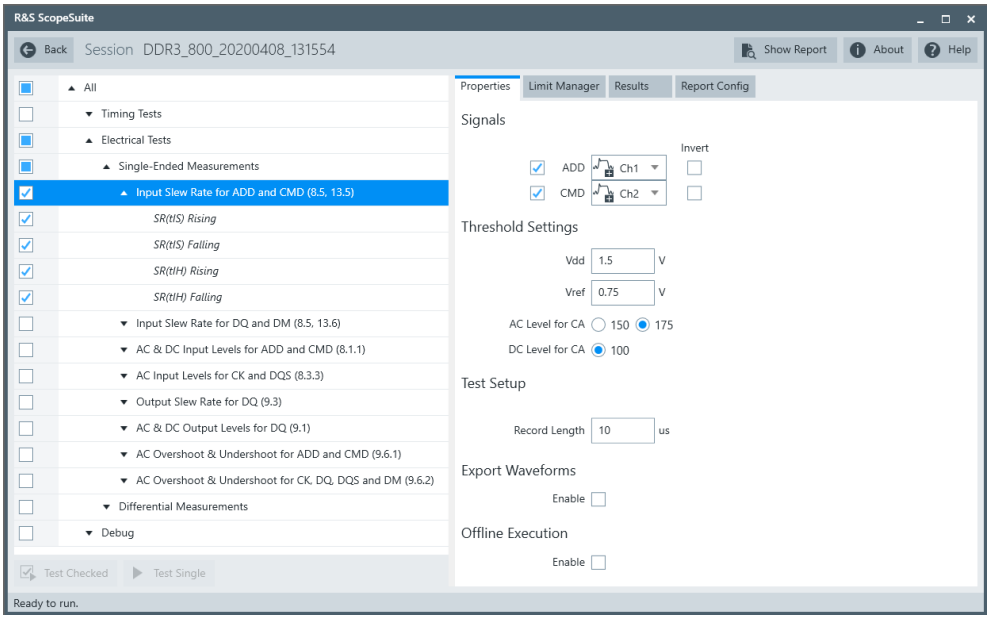
5.1.1 Input slew rate for ADD and CMD

5.1.1.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

5.1.1.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Single-Ended Signals" > "Input Slew Rate for ADD and CMD".



3. Enable the "Signals" you want to use.
   If only the ADD/CMD signal is selected, only ADD/CMD signal will be used to run the test.
   If both the ADD and the CMD signals are selected, test will be run using ADD signal first, followed by the CMD signal.
4. Enable the tests that you want to run.
5. Click "Test Single".
6. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
7. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.1.1.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.1.1.4 Measurements

The input slew rates for address and command measurements consist of up to four measurements. It tests the limits as defined in sections 8.5 and 13.5 (DDR3/DDR3L)/

7.6 and 11.5 (LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/ JESD209-3C(LPDDR3) specifications.

Setup slew rate rising - SR(tIS) rising

This test aims to verify that the setup slew rate for rising signal is within the limits defined in the specification.

Setup slew rate falling - SR(tIS) falling

This test aims to verify that the setup slew rate for falling signal is within the limits defined in the specification.

Hold slew rate rising - SR(tIH) rising

This test aims to verify that the hold slew rate for rising signal is within the limits defined in the specification.

Hold slew rate falling - SR(tIH) falling

This test aims to verify that the hold slew rate for falling signal is within the limits defined in the specification.

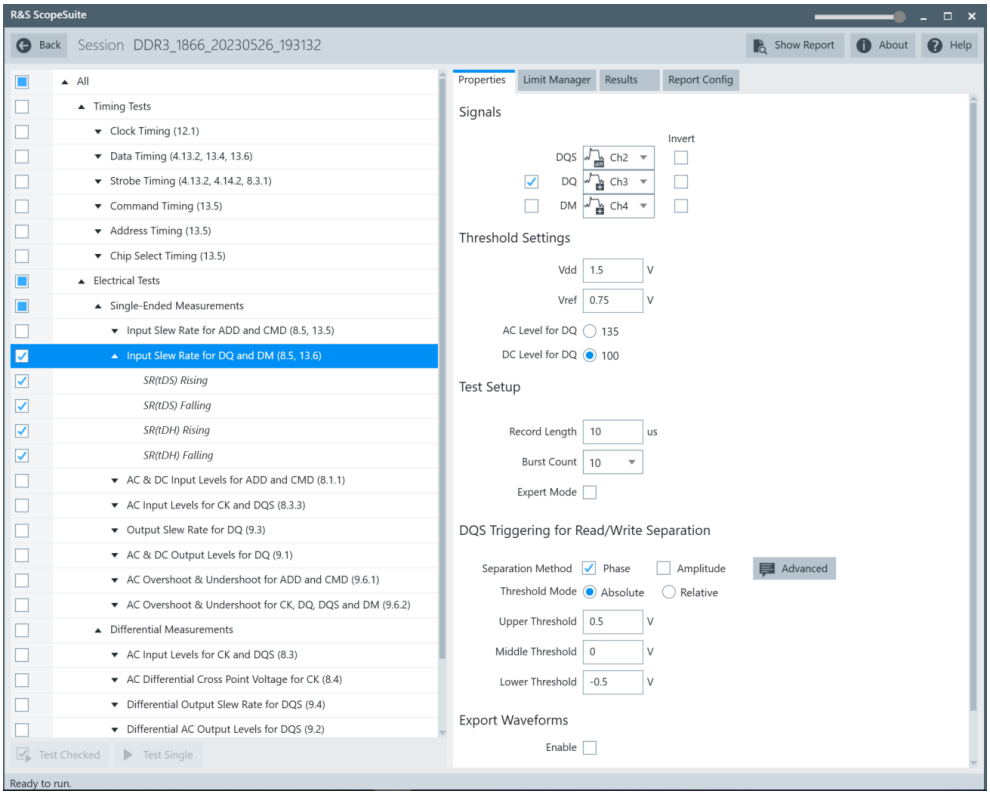
5.1.2 Input slew rate for DQ and DM

5.1.2.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

5.1.2.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Single-Ended Signals" > "Input Slew Rate for DQ and DM".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.1.2.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.1.2.4 Measurements

The input slew rates for data and mask measurements consist of up to four measurements. It tests the limits as defined in sections 8.5 and 13.6 (DDR3/DDR3L)/ 7.6 and

11.6 (LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/ JESD209-3C(LPDDR3) specifications.

Setup slew rate rising - SR(tIS) rising

This test aims to verify that the setup slew rate for rising signal is within the limits defined in the specification.

Setup slew rate falling - SR(tIS) falling

This test aims to verify that the setup slew rate for falling signal is within the limits defined in the specification.

Hold slew rate rising - SR(tIH) rising

This test aims to verify that the hold slew rate for rising signal is within the limits defined in the specification.

Hold slew rate falling - SR(tIH) falling

This test aims to verify that the hold slew rate for falling signal is within the limits defined in the specification.

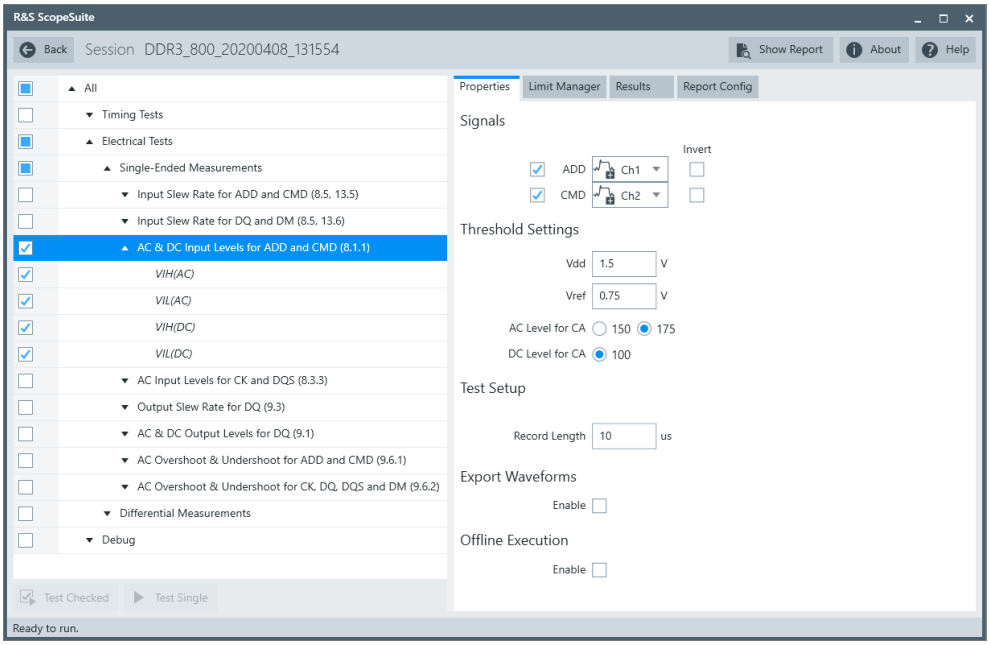
5.1.3 AC & DC input levels for ADD and CMD

5.1.3.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

5.1.3.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Single-Ended Signals" > "AC & DC input Levels for ADD and CMD".



3. Enable the "Signals" you want to use.
   If only the ADD/CMD signal is selected, only ADD/CMD signal will be used to run the test.
   If both the ADD and the CMD signals are selected, test will be run using ADD signal first, followed by the CMD signal.
4. Enable the tests that you want to run.
5. Click "Test Single".
6. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
7. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.1.3.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.1.3.4 Measurements

The AC and DC logic input levels for single-ended address and command measurements consist of up to four measurements. It tests the limits as defined in section

8.1.1(DDR3) / 3.1(DDR3L) / 7.1.1(LPDDR3) of the JESD79-3F(DDR3)/ JESD79-3-1A-01(DDR3L)/JESD209-3C(LPDDR3) specifications.

$V_{IH(AC)}$

This test aims to verify that the AC input logic high is within the limits defined in the specification.

$V_{IL(AC)}$

This test aims to verify that the AC input logic low is within the limits defined in the specification.

$V_{IH(DC)}$

This test aims to verify that the DC input logic high is within the limits defined in the specification.

$V_{IL(DC)}$

This test aims to verify that the DC input logic low is within the limits defined in the specification.

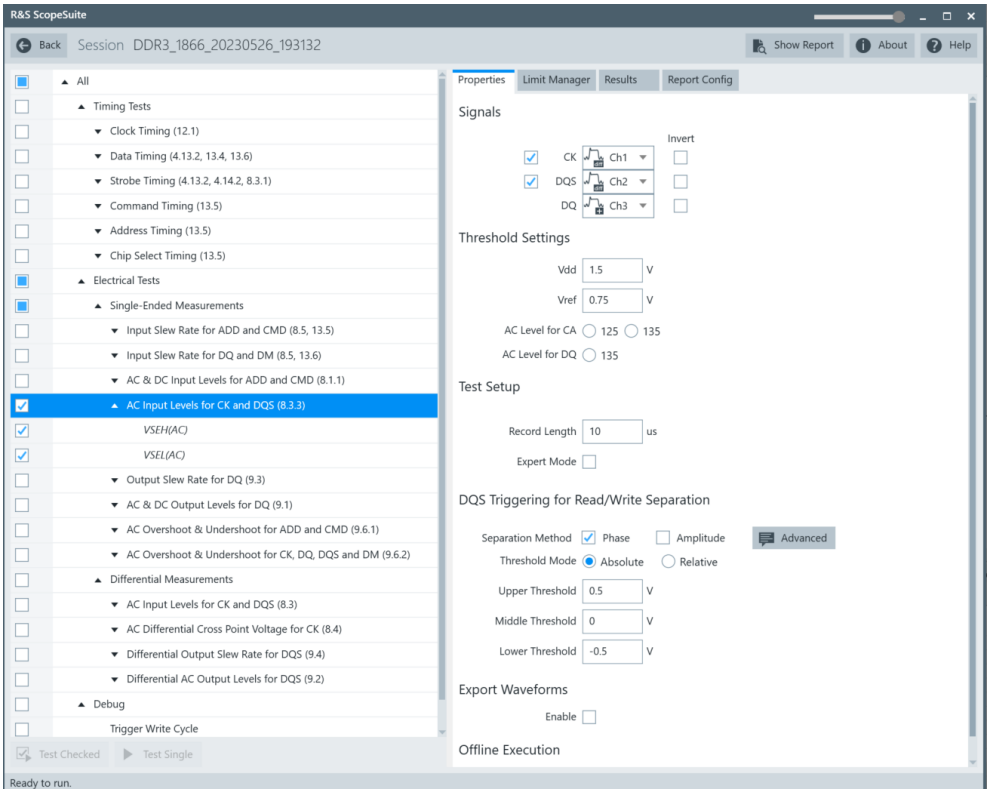
5.1.4 AC input levels for CK and DQS

5.1.4.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

5.1.4.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Single-Ended Signals" > "AC Input Levels for CK and DQS".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.1.4.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.1.4.4 Measurements

The single-ended AC input levels for clock and strobe measurements consist of up to two measurements. It tests the limits as defined in section 8.3.3 (DDR3) / 7.4.3 (LPDDR3) of the JESD79-3F(DDR3)/JESD209-3C(LPDDR3) specifications.

$V_{SEH(AC)}$

This test aims to verify that the single-ended high level for strobes/clock is within the limits defined in the specification.

$V_{SEL(AC)}$

This test aims to verify that the single-ended low level for strobes/clock is within the limits defined in the specification.

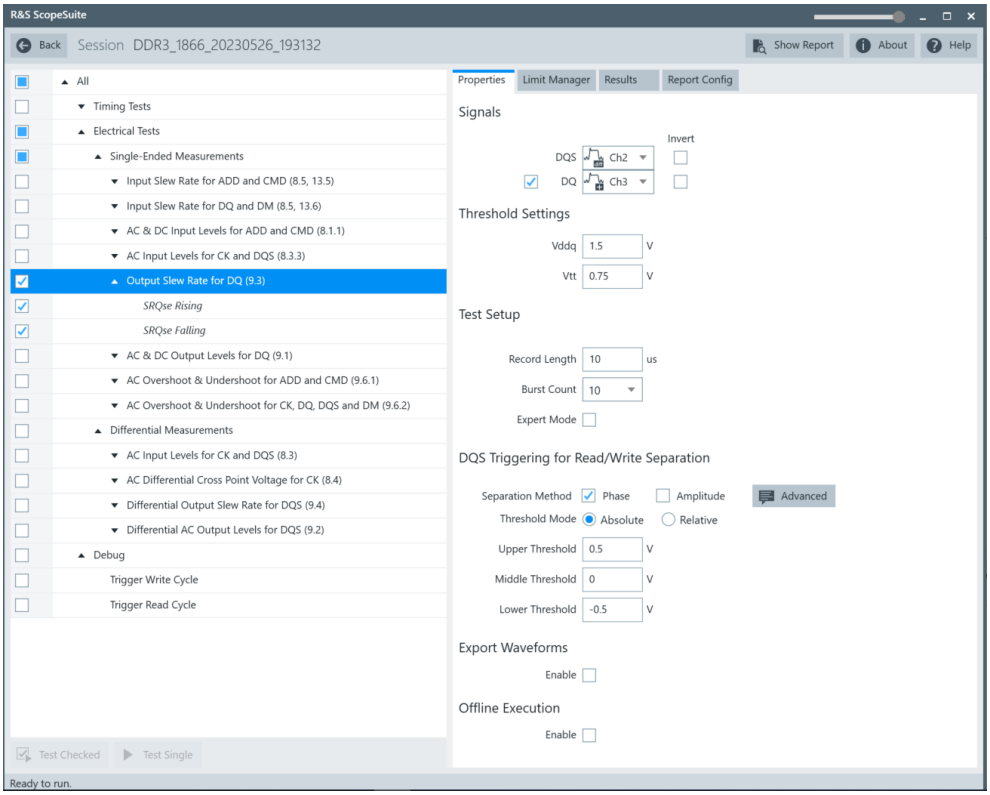
5.1.5 Output slew rate for DQ

5.1.5.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

5.1.5.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Single-Ended Signals" > "Output Slew Rate for DQ".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.1.5.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.1.5.4 Measurements

The single-ended output slew rate for data consists of up to two measurements. It tests the limits as defined in section 9.3 (DDR3) / 8 (DDR3L)/ 8.3 (LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/JESD209-3C(LPDDR3) specifications.

Slew rate query output single-ended signals rising- SRQse rising

This test aims to verify that the single-ended output slew rate for rising edge is within the limits defined in the specification. It is measured from VOL(AC) to VOH(AC).

Slew rate query output single-ended signals falling - SRQse falling

This test aims to verify that the single-ended output slew rate for falling edge is within the limits defined in the specification. It is measured from $V_{OH(AC)}$ to $V_{OL(AC)}$.

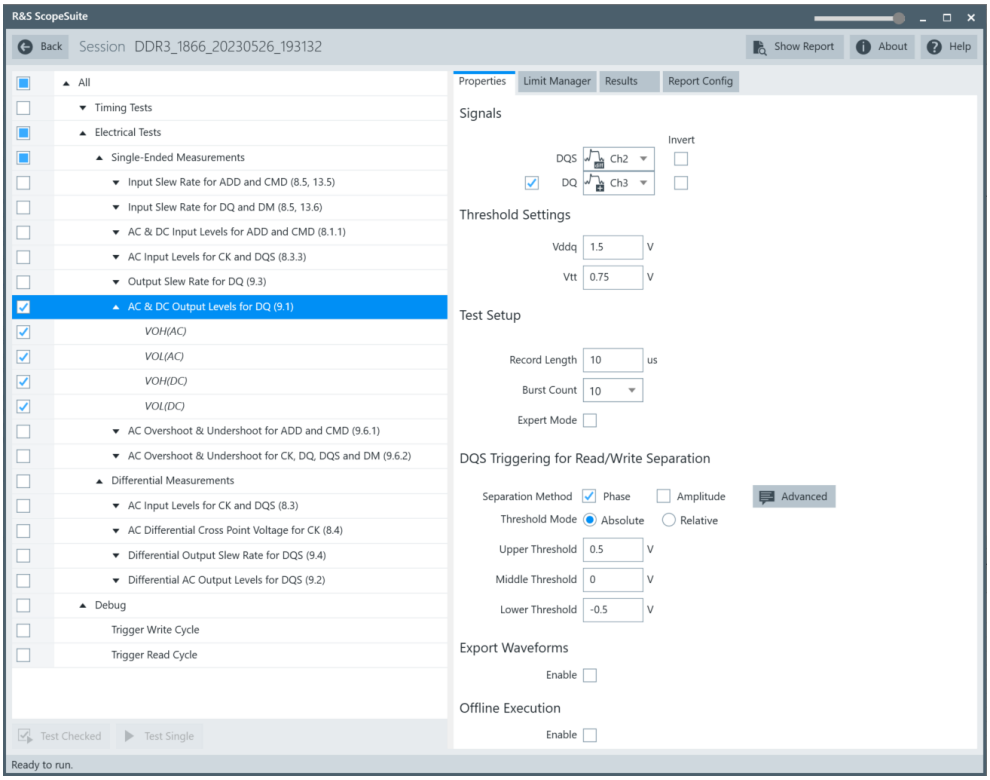
5.1.6 AC & DC output levels for DQ

5.1.6.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

5.1.6.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Single-Ended Signals" > "AC & DC Output Levels for DQ".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.1.6.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.1.6.4 Measurements

The AC & DC output levels for data measurements consist of up to four measurements. It tests the limits as defined in section 9.1 (DDR3/DDR3L)/ 8.1(LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/JESD209-3C(LPDDR3) specifications.

$V_{OH(AC)}$

This test aims to verify that the AC output high measurement level for the output slew rate is within the limits defined in the specification.

$V_{OL(AC)}$

This test aims to verify that the AC output low measurement level for the output slew rate is within the limits defined in the specification.

$V_{OH(DC)}$

This test aims to verify that the DC output high measurement level for IV curve linearity is within the limits defined in the specification.

$V_{OL(DC)}$

This test aims to verify that the DC output low measurement level for IV curve linearity is within the limits defined in the specification.

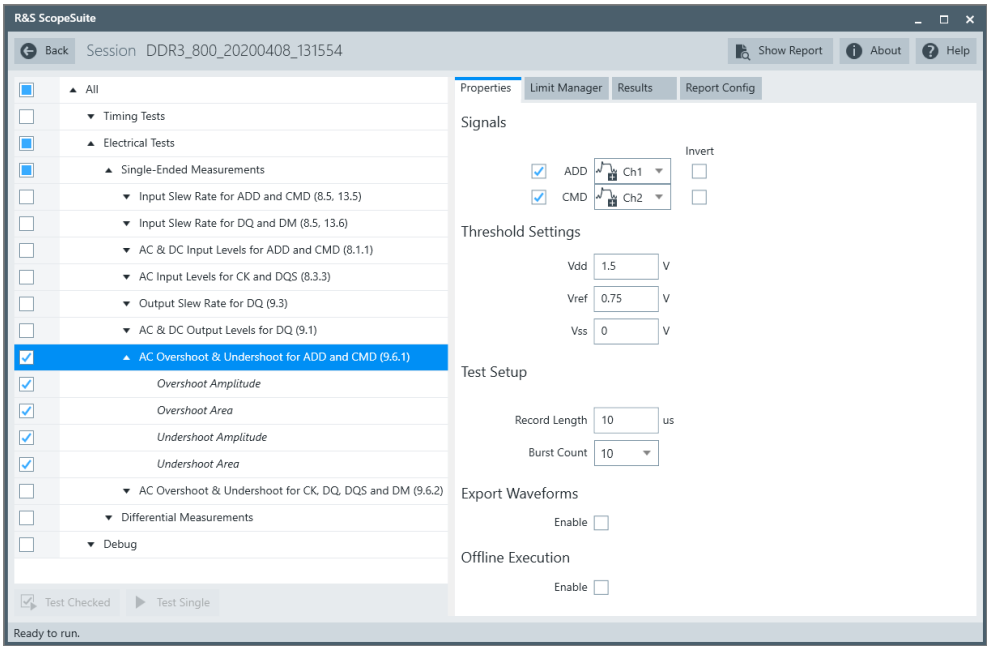
5.1.7 AC Overshoot & Undershoot for ADD and CMD

5.1.7.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

5.1.7.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Single-Ended Signals" > "AC Overshoot & Undershoot for ADD and CMD".



3. Enable the "Signals" you want to use.
   If only the ADD/CMD signal is selected, only ADD/CMD signal will be used to run the test.
   If both the ADD and the CMD signals are selected, test will be run using ADD signal first, followed by the CMD signal.
4. Enable the tests that you want to run.
5. Click "Test Single".
6. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
7. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.1.7.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.1.7.4 Measurements

The overshoot and undershoot for address and control measurements consist of up to four measurements. It tests the limits as defined in section 9.6.1 (DDR3/DDR3L)/

8.5(LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/ JESD209-3C(LPDDR3) specifications.

Overshoot amplitude

This test aims to verify that the maximum peak amplitude allowed for overshoot area is within the limits defined in the specification.

Overshoot area

This test aims to verify that the maximum overshoot area above V_{DD} is within the limits defined in the specification.

Undershoot amplitude

This test aims to verify that the maximum peak amplitude allowed for undershoot area is within the limits defined in the specification.

Undershoot area

This test aims to verify that the maximum undershoot area below V_{SS} is within the limits defined in the specification.

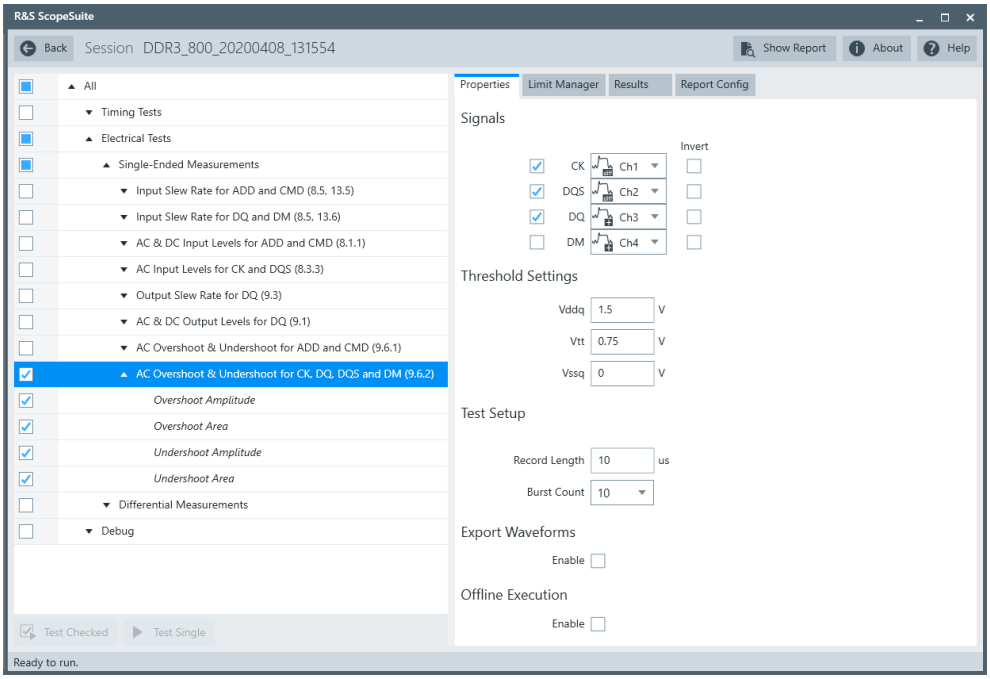
5.1.8 AC overshoot & undershoot for CK, DQ, DQS, and DM

5.1.8.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	4
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	4
DUT	DDR3 device that supports the selected type	1

5.1.8.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Single-Ended Signals" > "AC Overshoot & Undershoot for CK, DQ, DQS, and DM".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.1.8.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.1.8.4 Measurements

The overshoot and undershoot for clock, data, strobe and mask measurements consist of up to four measurements. It tests the limits as defined in section 9.6.2 (DDR3/ DDR3L)/ 8.5(LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/ JESD209-3C(LPDDR3) specifications.

Overshoot amplitude

This test aims to verify that the maximum peak amplitude allowed for overshoot area is within the limits defined in the specification.

Overshoot area

This test aims to verify that the maximum overshoot area above V_{DDQ} is within the limits defined in the specification.

Undershoot amplitude

This test aims to verify that the maximum peak amplitude allowed for undershoot area is within the limits defined in the specification.

Undershoot area

This test aims to verify that the maximum undershoot area below VSSQ is within the limits defined in the specification.

5.2 Differential signals

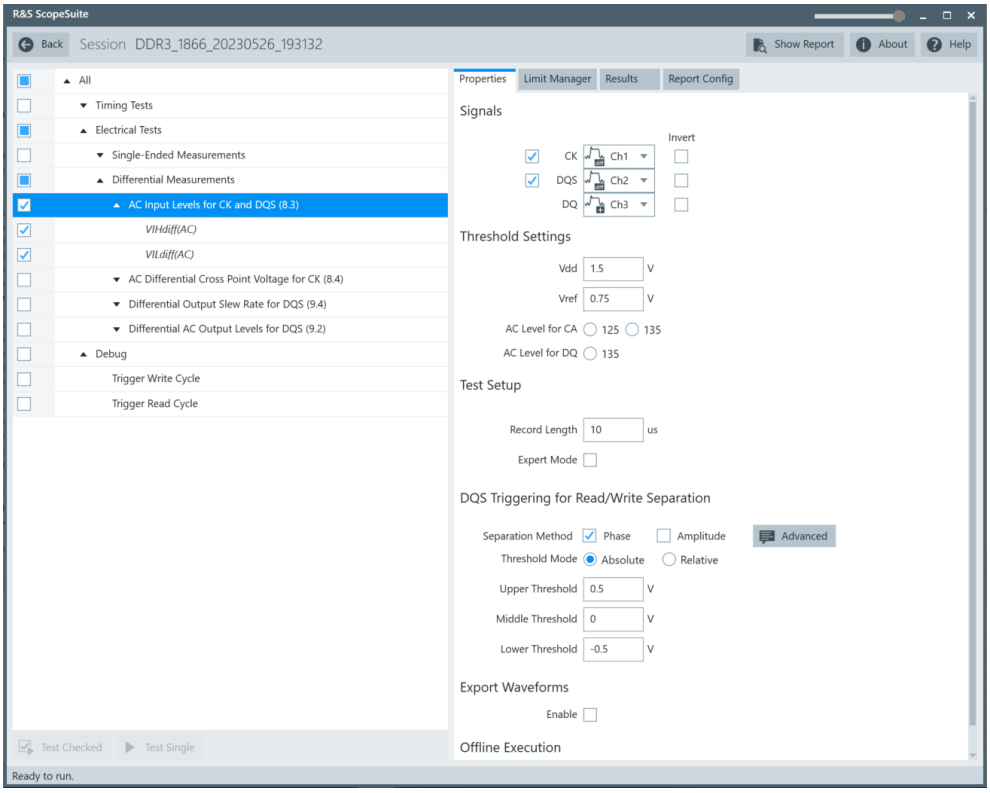
5.2.1 AC input levels for CK and DQS

5.2.1.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

5.2.1.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Differential Signals" > "AC Input Levels for CK and DQS".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.2.1.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.2.1.4 Measurements

The differential AC input levels for clock and strobe measurements consist of up to two measurements. It tests the limits as defined in section 8.3 (DDR3) / 10.1(DDR3L) /

7.4.2 (LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/ JESD209-3C(LPDDR3) specifications.

Differential input high AC - $V_{IHdiff(AC)}$

This test aims to verify that the AC differential input high is within the limits defined in the specification.

Differential input low AC - $V_{ILdiff(AC)}$

This test aims to verify that the AC differential input low is within the limits defined in the specification.

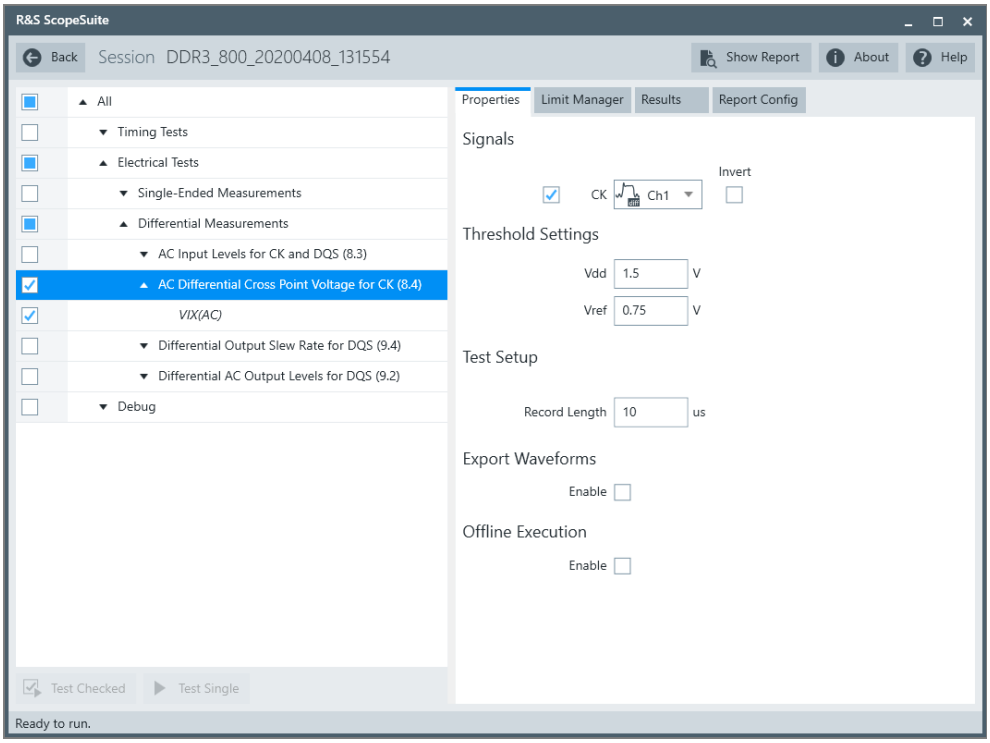
5.2.2 AC Differential Cross Point Voltage for CK

5.2.2.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	3
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	3
DUT	DDR3 device that supports the selected type	1

5.2.2.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Differential Signals" > "AC Differential Cross Point Voltage for CK".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.2.2.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.2.2.4 Measurements

The differential cross point voltage for clock measurement consists of one measurement. It tests the limits as defined in section 8.4 (DDR3) / 11(DDR3L) / 7.5 (LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/JESD209-3C(LPDDR3) specifications.

Differential input cross point voltage - $V_{IX(AC)}$

This test aims to verify that the differential input cross point voltage is within the limits defined in the specification. It is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.

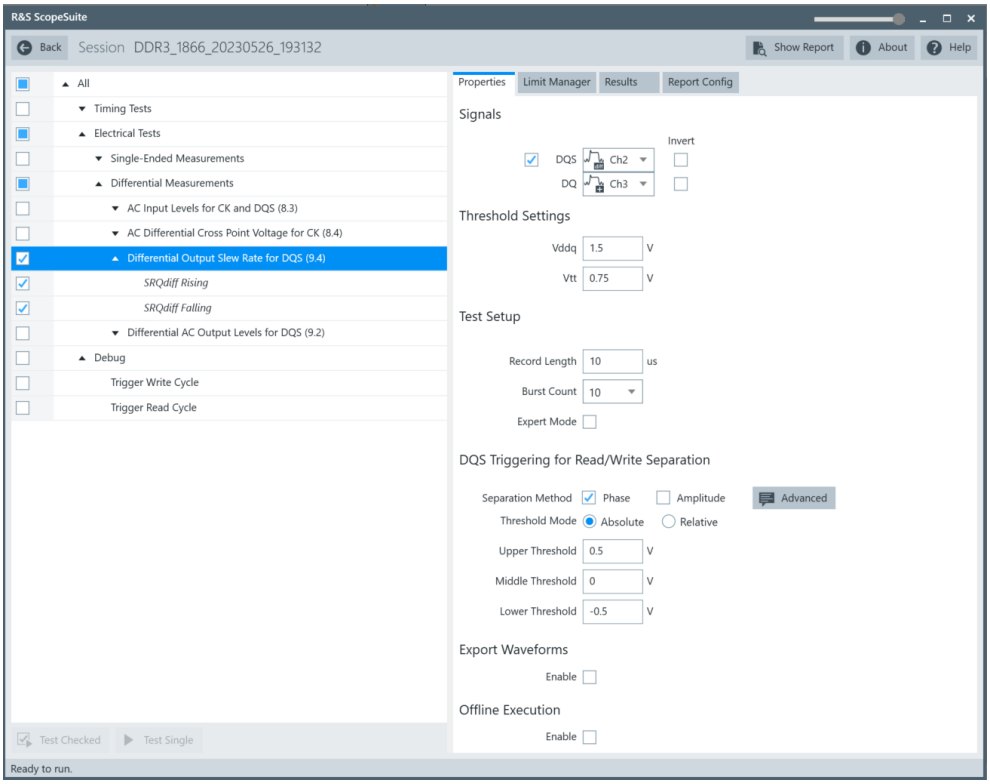
5.2.3 Differential output slew rate for DQS

5.2.3.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

5.2.3.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Differential Signals" > "Differential Output Slew Rate for DQS".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.2.3.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.2.3.4 Measurements

The differential output slew rate for strobe consists of up to two measurements. It tests the limits as defined in section 9.4 (DDR3) / 9 (DDR3L) / 8.4 (LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/JESD209-3C(LPDDR3) specifications.

Slew rate query output differential signals rising- SRQdiff rising

This test aims to verify that the differential output slew rate for rising edge is within the limits defined in the specification. It is measured from $V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$.

Slew rate query output differential signals falling - SRQdiff falling

This test aims to verify that the differential output slew rate for falling edge is within the limits defined in the specification. It is measured from $V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$.

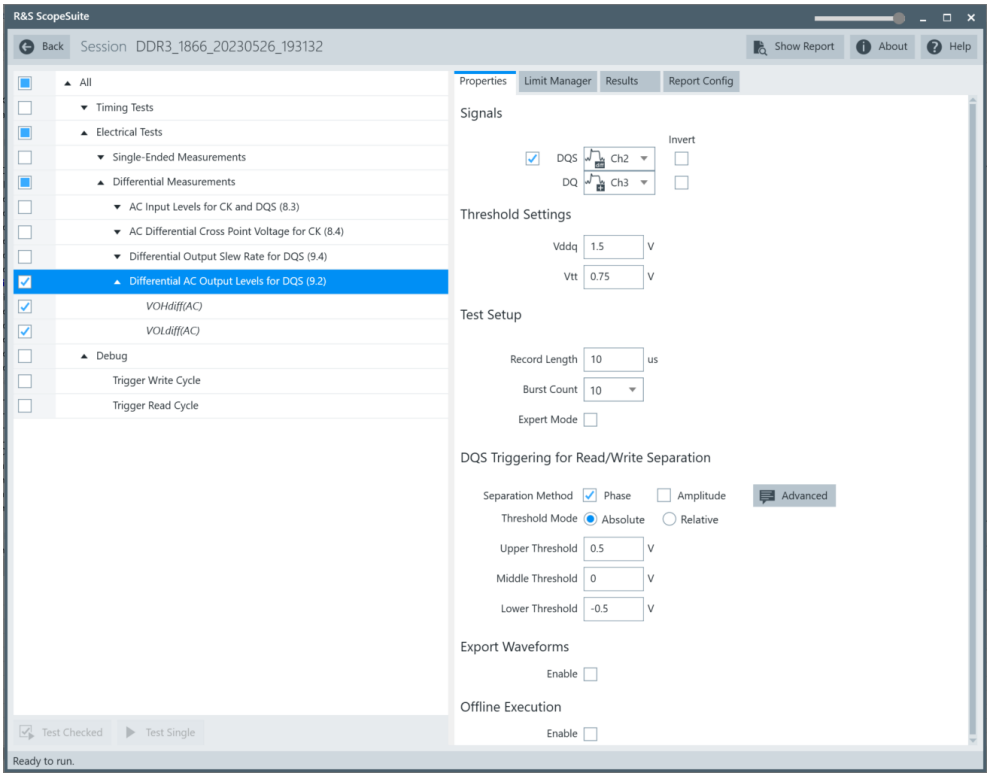
5.2.4 Differential AC output levels for DQS

5.2.4.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR3 device that supports the selected type	1

5.2.4.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Electrical Tests" > "Differential Signals" > "Differential AC Output Levels for DQS".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

5.2.4.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

5.2.4.4 Measurements

The differential AC output levels for strobe measurements consist of up to two measurements. It tests the limits as defined in section 9.2 (DDR3/DDR3L) / 8.2(LPDDR3) of the JESD79-3F(DDR3)/JESD79-3-1A-01(DDR3L)/JESD209-3C(LPDDR3) specifications.

$V_{OHdiff(AC)}$

This test aims to verify that the AC differential output high measurement level for the output slew rate is within the limits defined in the specification.

$V_{OLdiff(AC)}$

This test aims to verify that the AC differential output low measurement level for the output slew rate is within the limits defined in the specification.

6 Debug tests

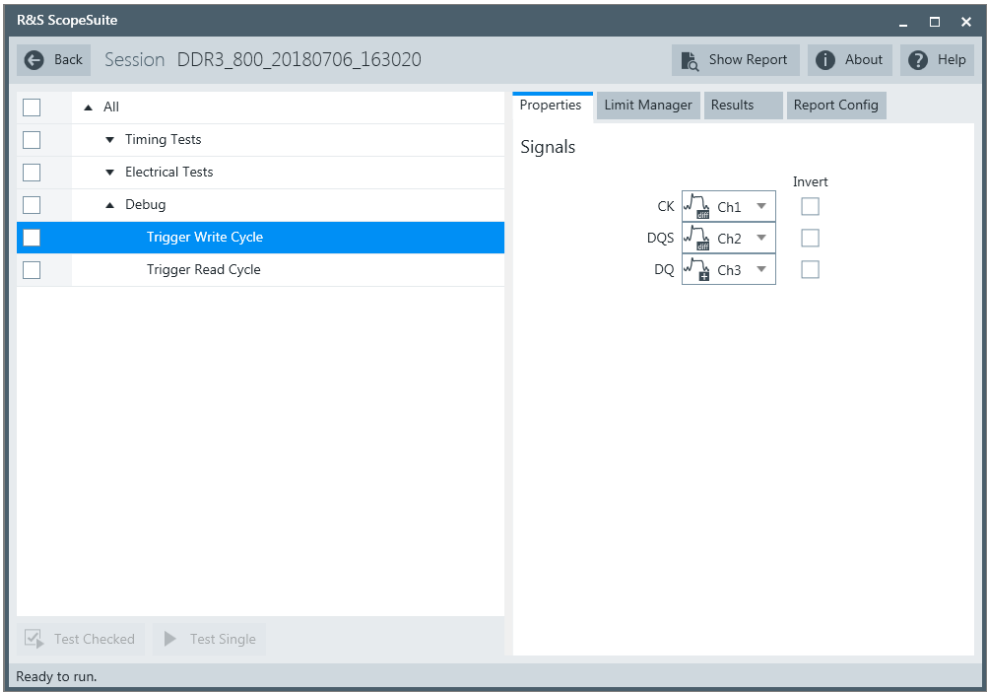
6.1 Trigger write cycle

6.1.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	3
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	3
DUT	DDR3 device that supports the selected type	1

6.1.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.
2. Select "Debug" > "Trigger Write Cycle".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

6.1.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

6.1.4 Measurements

This test case helps you to see the signals of CK, DQS, DQ during the write operation of DDR3. The signals are triggered to make the write burst visible.

6.2 Trigger read cycle

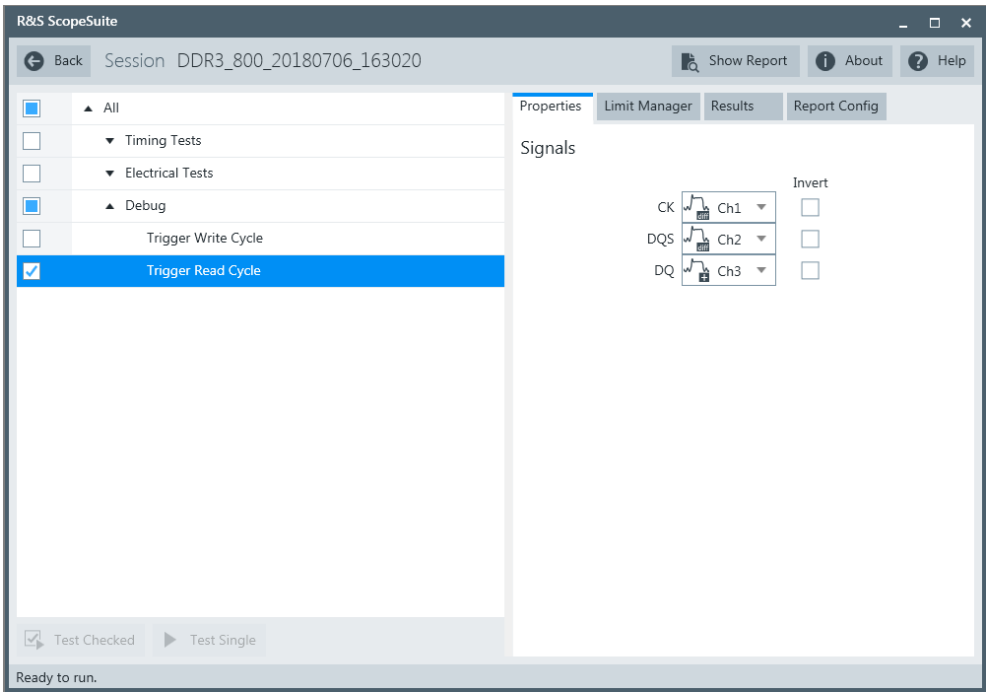
6.2.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz bandwidth R&S RTO2000/RTO6 with 4 channels and minimum 4 GHz bandwidth	1
Modular Probe	Probe with minimum 9 GHz bandwidth	3
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	3
DUT	DDR3 device that supports the selected type	1

6.2.2 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DDR3 Tests", on page 24.

2. Select "Debug" > "Trigger Read Cycle".



3. Enable the tests that you want to run.
4. Click "Test Single".
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.
6. You can also run the test in offline mode, using downloaded waveforms. For details, see Chapter 3.2.2, "Test configuration for DDR3", on page 18.

6.2.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1.1, "Soldering guide for modular probes", on page 9.

6.2.4 Measurements

This test case helps you to see the signals of CK, DQS, DQ during the read operation of DDR3. The signals are triggered to make the read burst visible.