R&S®RTO-K26/-K27, R&S®RTO6-K26/-K27, R&S®RTP-K26/-K27
D-PHY Compliance Test
User Manual

1326101002
Version 09

ROHDE&SCHWARZ
Make ideas real

This manual describes the D-PHY compliance test procedures with the following option:

- R&S®RTO-K26 (1317.5668.02) - D-PHY
- R&S®RTO6-K26 (1801.6958.02) - D-PHY
- R&S®RTP-K26 (1337.8727.02) - D-PHY
- R&S®RTO-K27 (1803.6584.02) - D-PHY 2.5
- R&S®RTO6-K27 (1803.6578.02) - D-PHY 2.5
- R&S®RTP-K27 (1800.5993.02) - D-PHY 2.5

The tests require the R&S ScopeSuite software.

The software contained in this product uses several valuable open source software packages. For information, see the "Open Source Acknowledgment" document, which is available for download from the R&S RTO/RTO6/RTP product page at http://www.rohde-schwarz.com/product/rto.html > "Software".
Rohde & Schwarz would like to thank the open source community for their valuable contribution to embedded computing.

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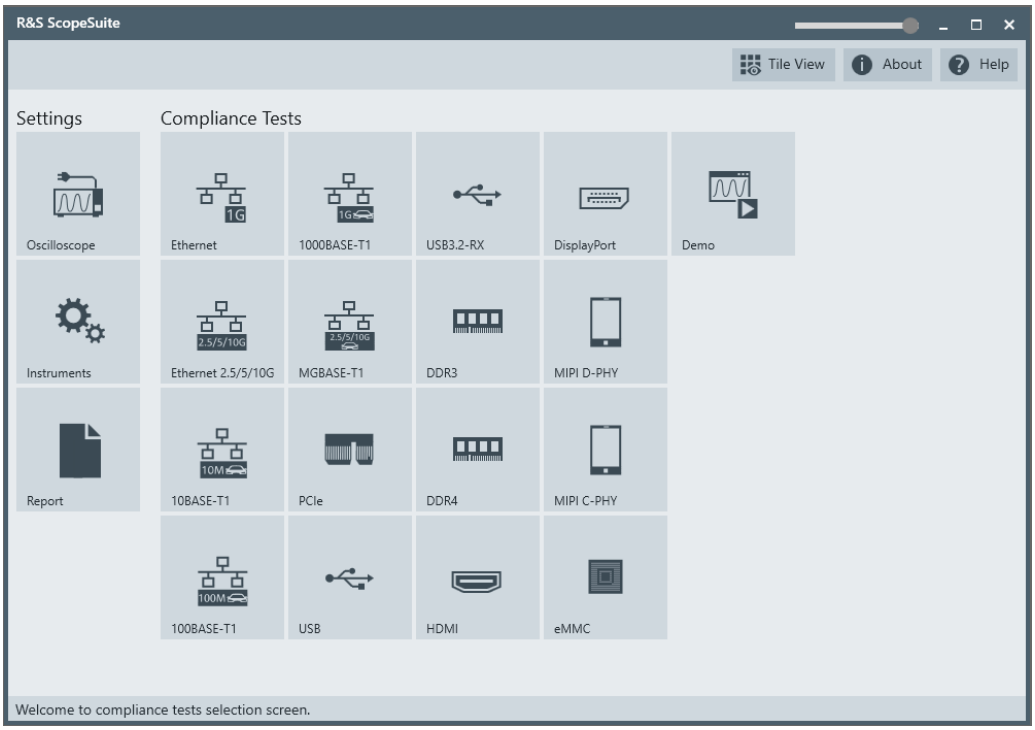
The following abbreviations are used throughout this manual: R&S®RTO is abbreviated as R&S RTO, R&S®RTP is abbreviated as R&S RTP and R&S®ScopeSuite is abbreviated as R&S ScopeSuite.

Contents

1 R&S ScopeSuite overview

The R&S ScopeSuite software is used with R&S RTO/RTO6/RTP oscilloscopes. It can be installed on a test computer or directly on the oscilloscope. For system requirements, refer to the Release Notes.



The R&S ScopeSuite main panel has several areas:

- "Settings": connection settings to oscilloscope and other instruments also default report settings
- "Compliance Tests": selection of the compliance test
- "Demo": accesses demo test cases that can be used for trying out the software without having a connection to an oscilloscope
- : shift sideways to change the transparency of the dialog box
- "Help": opens the help file, containing information about the R&S ScopeSuite configuration
- "About": gives information about the R&S ScopeSuite software
- "Tile View": allows a personalization of the compliance test selection
  You can configure which tests are visible in the compliance test section and which are hidden, so that only the ones you use are displayed.

► To hide a test from the "Compliance Tests" view, do one of the following:

a) Right-click on the compliance test that you want to hide.
The icon of the test changes, see Figure 1-1. Now with a left click you can hide the test.

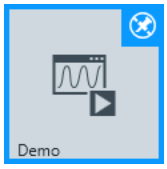


Figure 1-1: Unpin icon

b) Click on "Title View" to show a list of the available test cases. By clicking a test case in the show list, you can pin/unpin it from the main panel.

2 Preparing the measurements

2.1 Test equipment

For D-PHY compliance tests, the following test equipment is needed:

- R&S RTO/RTO6/RTP oscilloscope with 4 channels and at least 4 GHz bandwidth
- For measuring the clock signal (+ and -): either 1 differential probe or 2 single-ended probes with at least 4 GHz bandwidth. However, note that D-PHY Group 2 and Group 4 tests require 2 probes for the clock signal.
- For measuring the data signal (+ and -): 2 probes with at least 4 GHz bandwidth Available probes: R&S RT-ZD40 or R&S RT-ZM with a different probe tip selection.
- R&S RTO/ RTO6 / RTP-K26 D-PHY compliance test option (required option, installed on the oscilloscope)
- R&S RTO/ RTO6 / RTP-K27 D-PHY compliance test option (required option, installed on the oscilloscope)
- For Eye Tests, the following options are needed:

  For R&S RTP:

  – Option R&S RTP-K136 or R&S RTP-K137 Advanced eye analysis

  For R&S RTO/ R&S RTO6:

  – R&S RTO/R&S RTO6-K91 (DDR3) or R&S RTO/R&S RTO6-K93 (DDR4)
- Recommended test fixture for LP-TX tests: MIPI D-PHY Capacitive Load (C_{LOAD}) fixture from The University of New Hampshire InterOperability Laboratory (UNH-IOL)
- Recommended termination board for HS-TX tests: MIPI D-PHY Reference Termination Board (RTB) from The University of New Hampshire InterOperability Laboratory (UNH-IOL)
- The free-of-charge R&S ScopeSuite software, which can be installed on a computer or directly on the oscilloscope.

2.2 Installing software and license

The preparation steps are performed only once for each computer and instrument that are used for testing.

Uninstall older versions of the R&S ScopeSuite

If an older version of the R&S ScopeSuite is installed, make sure to uninstall the old version before you install the new one. You can find the version number of the current installation in "Help" menu > "About". To uninstall the R&S ScopeSuite, use the Windows " Control Panel" > "Programs".

For best operation results, we recommend that the installed firmware versions of the R&S ScopeSuite and the oscilloscope are the same.

To install the R&S ScopeSuite

1. Download the latest R&S ScopeSuite software from the "Software" section on the Rohde & Schwarz R&S RTO/RTO6/RTP website:
   www.rohde-schwarz.com/product/rtp.html
   www.rohde-schwarz.com/product/rto.html
2. Install the R&S ScopeSuite software:
   - On the computer that is used for testing, or
   - On the R&S RTO/RTO6/RTP.

   For system requirements, refer to the Release Notes.

To install the license key on the R&S RTO/RTO6/RTP

► When you got the license key of the compliance test option, enable it on the oscilloscope using [Setup] > "SW Options".
For a detailed description, refer to the R&S RTO/RTO6/RTP user manual, chapter "Installing Options", or to the online help on the instrument.

2.3 Setting up the network

If the R&S ScopeSuite software runs on a test computer, the computer and the testing oscilloscope require a LAN connection.

For some test cases, you need an additional instrument: arbitrary waveform generator (AWG), vector network analyzer (VNA), or spectrum analyzer. These instruments can be used in automatic or manual mode. For automatic testing, a LAN connection to the additional instrument is required.

There are two ways of connection:

- LAN (local area network): It is recommended that you connect to a LAN with DHCP server. This server uses the Dynamic Host Configuration Protocol (DHCP) to assign all address information automatically.
- Direct connection of the instruments and the computer or connection to a switch using LAN cables: Assign fixed IP addresses to the computer and the instruments and reboot all devices.

To set up and test the LAN connection

1. Connect the computer and the instruments to the same LAN.
2. Start all devices.
3. If no DHCP server is available, assign fixed IP addresses to all devices.
4. Ping the instruments to make sure that the connection is established.

5. If VISA is installed, check if VISA can access the instruments.
   a) Start VISA on the test computer.
   b) Validate the VISA address string of each device.

See also:

- Chapter 2.5, "Connecting the R&S RTO/RTO6/RTP", on page 9

2.4 Starting the R&S ScopeSuite

To start the R&S ScopeSuite on the test computer or on the oscilloscope:

► Double-click the R&S ScopeSuite program icon.

To start the R&S ScopeSuite on the instrument, in the R&S RTO/RTO6/RTP firmware:

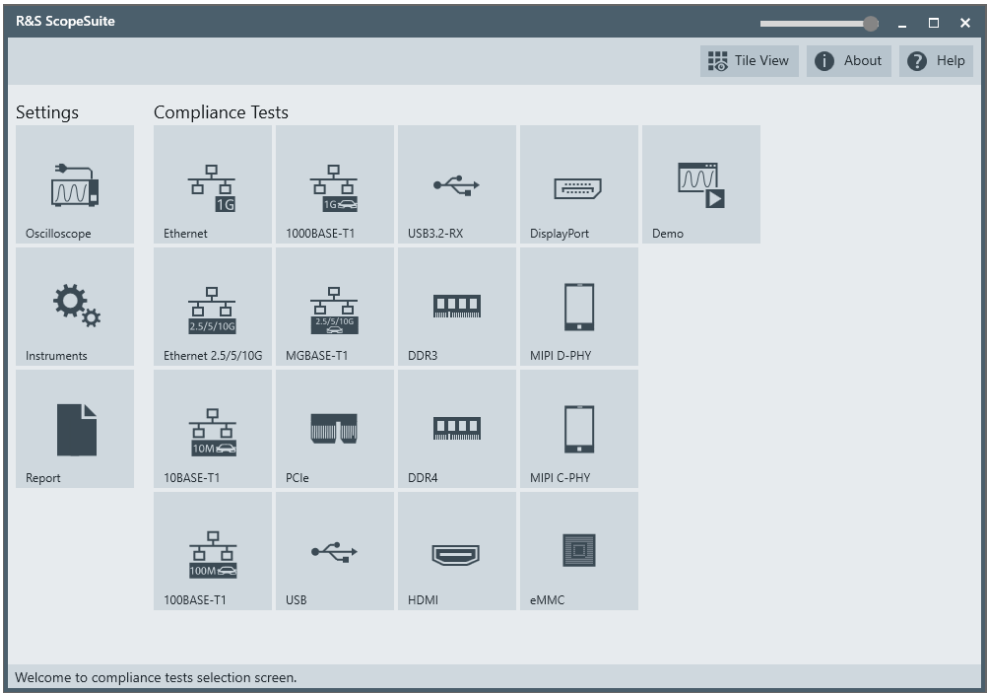
► In the "Apps" dialog, open the "Compliance" tab.

2.5 Connecting the R&S RTO/RTO6/RTP

If the R&S ScopeSuite is installed directly on the instrument, the software detects the R&S RTO/RTO6/RTP firmware automatically, and the "Oscilloscope" button is not available in the R&S ScopeSuite.

If the R&S ScopeSuite software runs on a test computer, the computer and the testing oscilloscope require a LAN connection, see Chapter 2.3, "Setting up the network", on page 8. The R&S ScopeSuite software needs the IP address of the oscilloscope to establish connection.

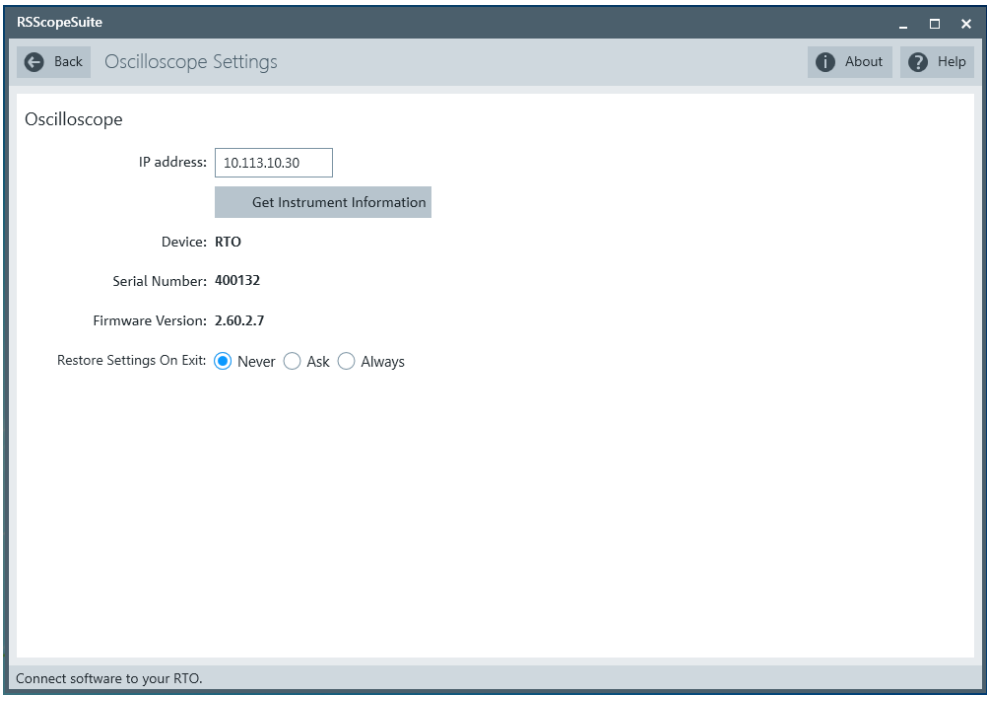
1. Start the R&S RTO/RTO6/RTP.
2. Start the R&S ScopeSuite software.
3. Click "Settings" > "Oscilloscope".



4. Enter the IP address of the oscilloscope.
   To obtain the IP address: press the Rohde & Schwarz logo at the top-right corner of the oscilloscope's display.

5. Click "Get Instrument Information".

   The computer connects with the instrument and gets the instrument data.

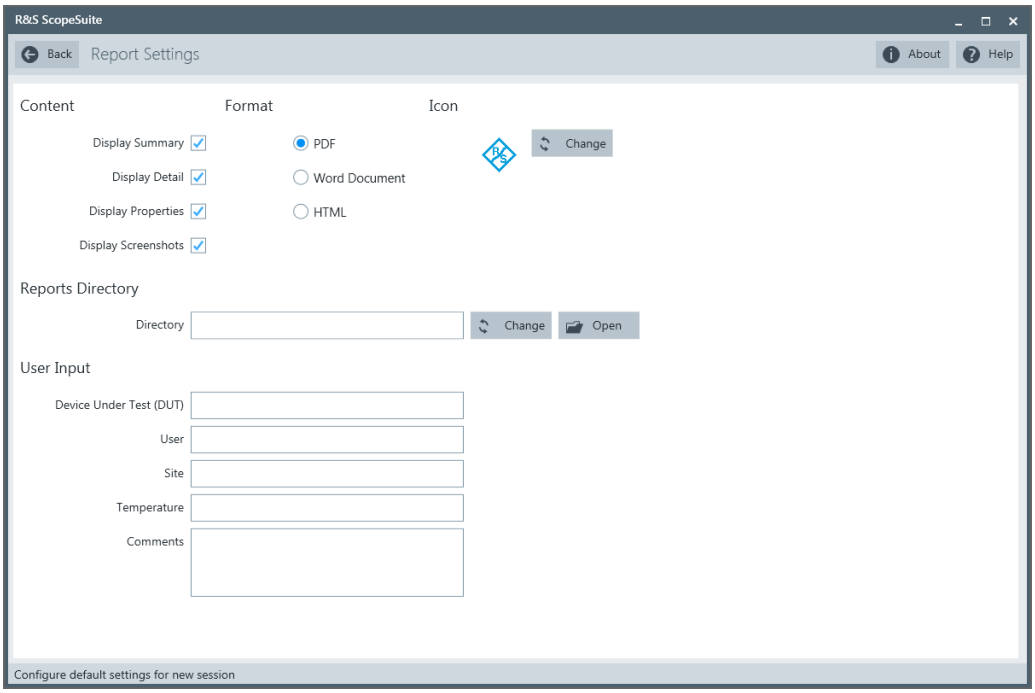


If the connection fails, an error message is shown.

2.6 Report configuration

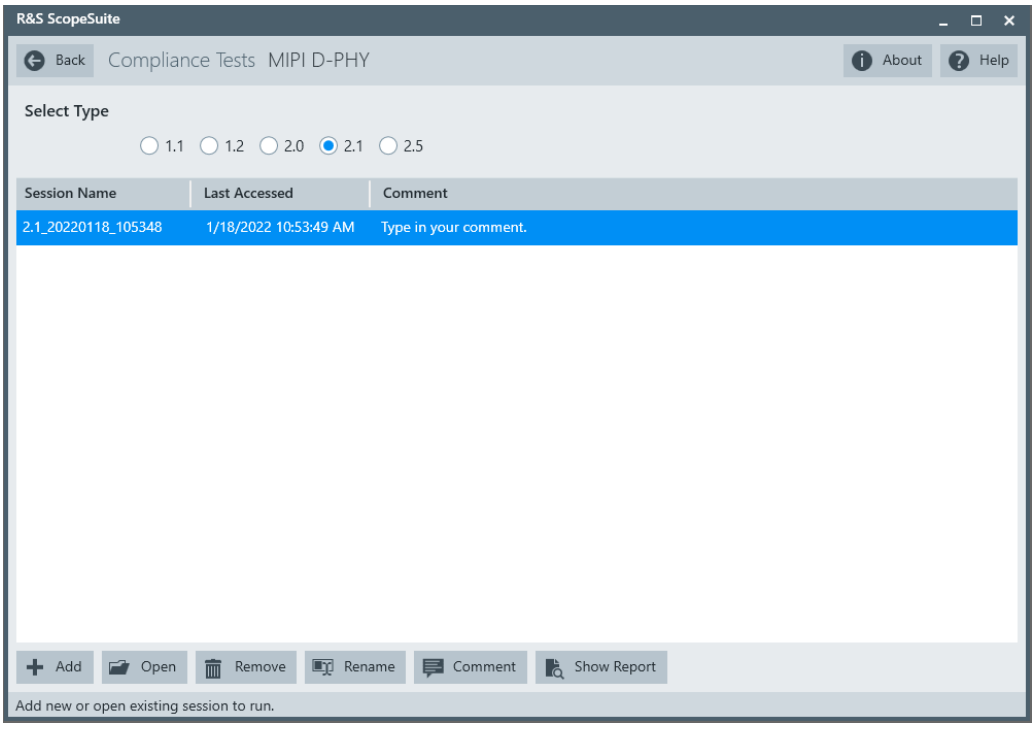
In the "Report Configuration" menu, you can select the format of the report and the details to be included in the report. You can also select an icon that is displayed in the upper left corner of the report.

Also, you can enter common information on the test that is written in the "General Information" section of the test report.



3 Performing tests

3.1 Starting a test session



After you open a compliance test, the "Session Selection" dialog appears. In this dialog, you can create new sessions, open or view existing report.

The following functions are available for handling test sessions:

Function	Description
"Add"	Adds a new session
"Open"	Opens the selected session
"Remove"	Removes the selected session
"Rename"	Changes the "Session Name"
"Comment"	Adds a comment
"Show report"	Generates a report for the selected session

To add a test session

1. In the R&S ScopeSuite window, select the compliance test.
2. In the "Session Selection" dialog press "Add".
3. If necessary change the "Session Name"

To open a test session

1. In the R&S ScopeSuite window, select the compliance test.
2. In the "Session Selection" dialog, select the session you want to open and double click on it.
   Alternatively, select the session and press "Open".

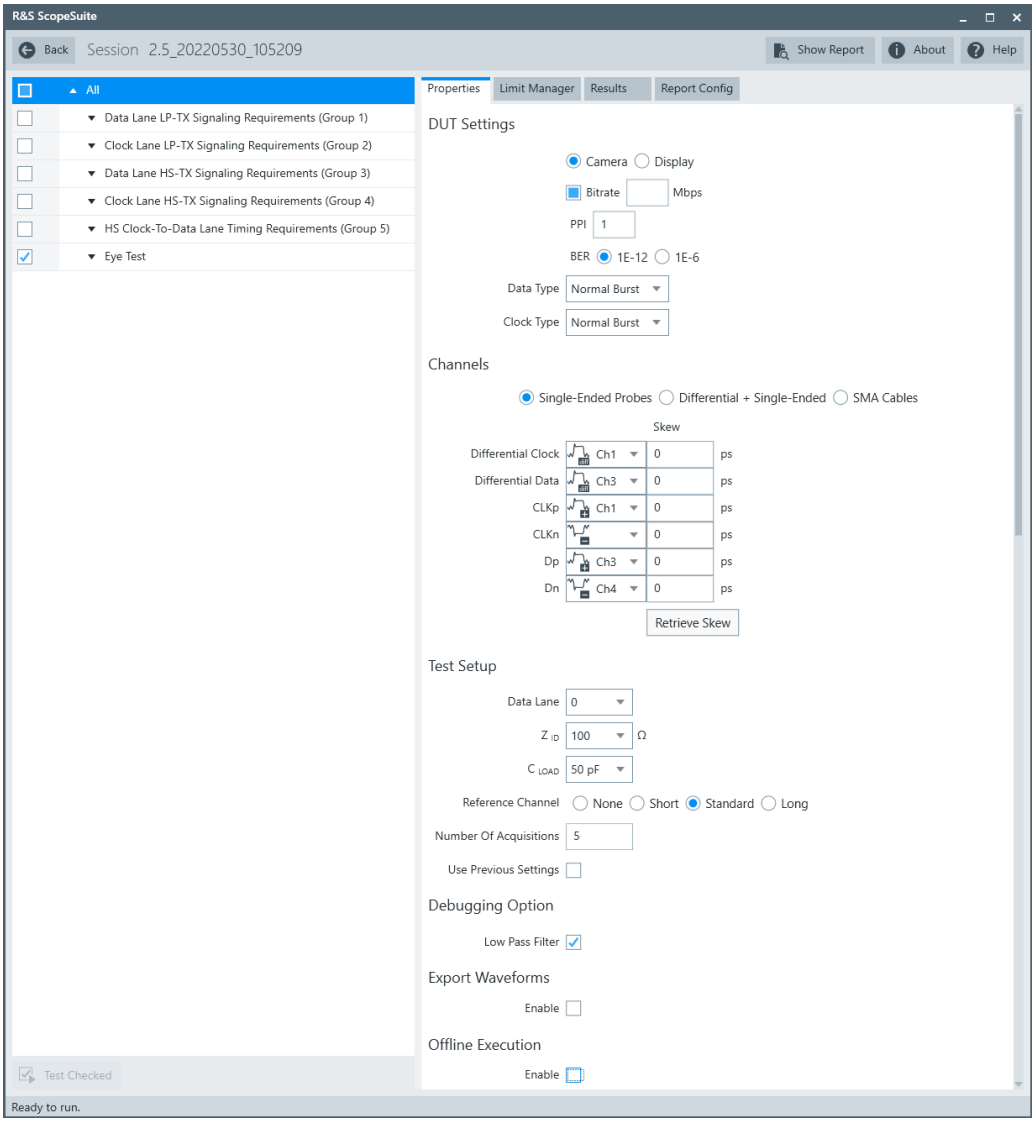
To show a report for a test session

1. In the R&S ScopeSuite window, select the compliance test.
2. In the "Session Selection" dialog, select the session you want the report for and press "Show report".

3.2 Configuring the test

1. In the R&S ScopeSuite window, select the compliance test to be performed:
   - "MIPI D-PHY"
2. Open a test session, see Chapter 3.1, "Starting a test session", on page 12.
3. Adjust the "Properties" settings for the test cases you want to perform.
4. Click "Limit Manager" and edit the limit criteria, see Chapter 3.2.1.1, "Limit manager", on page 15.
5. If you want to use special report settings the "Report Config" tab to define the format and contents of the report. Otherwise the settings defined in "RSScopeSuite" > "Settings" > "Report" are used. See Chapter 2.6, "Report configuration", on page 11.
6. Click "Test Checked"/"Test Single" and proceed as described in the relevant test case chapter.

3.2.1 General test settings



Each session dialog is divided into several sections:

- "Properties": shows the settings that can be made for the test case selected on the left side of the dialog. You can differentiate between the "All" and the sub test properties
  In the "All" > "Properties" tab you can configure the settings for all test cases in the current session. Once you change and save a setting in this tab, the changes will be done for all test in the sessions. At the same time, there will be a special marking for the functions that have different settings for different sub tests.
- "Limit Manager": sets the measurement limits that are used for compliance testing, see Chapter 3.2.1.1, "Limit manager", on page 15.
- "Results": shows an overview of the available test results for this session.
- "Instruments": defines instruments settings for connecting to external devices, that are specific for this test session.

When a session is first created the global settings ("RSScopeSuite" > "Settings" > "Instruments") are copied to the session. This "Instruments" tab can be used to change those copied defaults.

- "Report Config": defines the format and contents of the report for this session. When a session is first created the global settings ("RSScopeSuite" > "Settings" > "Report") are copied to the session. This "Report Config" tab can be used to change those copied defaults.
- "Test Checked"/ "Test Single": starts the selected test group.

3.2.1.1 Limit manager

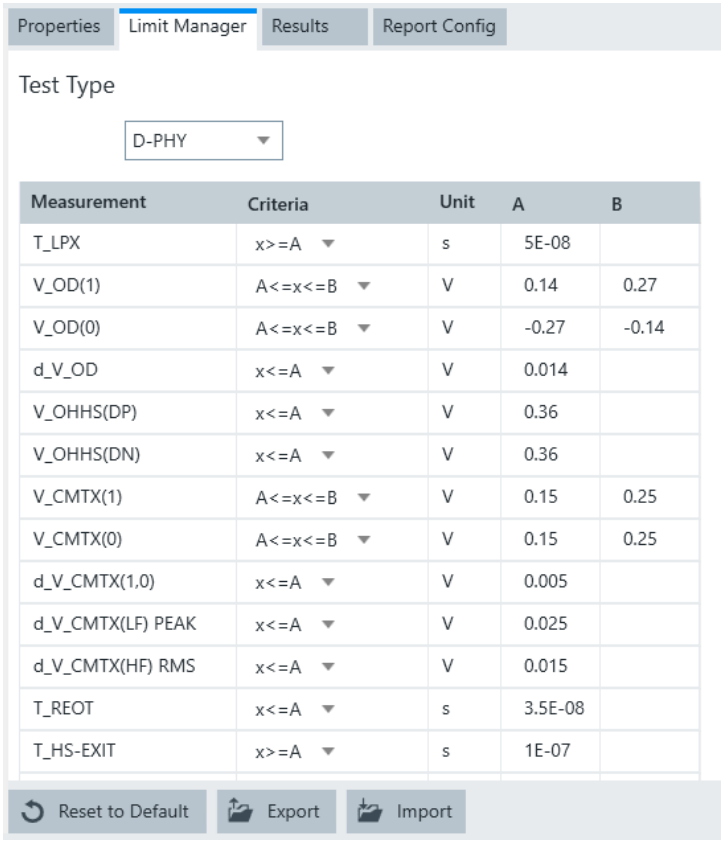
The "Limit Manager" shows the measurement limits that are used for compliance testing.

Each limit comprises the comparison criterion, the unit, the limit value A, and a second limit value B if the criterion requires two limits.

You can set the values to defaults, change the values in the table, export the table in xml format, or import xml files with limit settings.

You can also return the values to the original limits with "Reset to default".

1. Select the "Test Type".
2. Check and adjust the measurement limits.



Measurement	Criteria	Unit	A	B
T_LPX	x>=A	s	5E-08	
V_OD(1)	A<=x<=B	V	0.14	0.27
V_OD(0)	A<=x<=B	V	-0.27	-0.14
d_V_OD	x<=A	V	0.014	
V_OHHS(DP)	x<=A	V	0.36	
V_OHHS(DN)	x<=A	V	0.36	
V_CMTX(1)	A<=x<=B	V	0.15	0.25
V_CMTX(0)	A<=x<=B	V	0.15	0.25
d_V_CMTX(1,0)	x<=A	V	0.005	
d_V_CMTX(LF) PEAK	x<=A	V	0.025	
d_V_CMTX(HF) RMS	x<=A	V	0.015	
T_REOT	x<=A	s	3.5E-08	
T_HS-EXIT	x>=A	s	1E-07	

3.3 Getting test results

For each test, the test data - report, diagrams and waveform files - is saved in the following folder:

`%ProgramData%\Rohde-Schwarz\RSScopeSuite2\Sessions\D-PHY\<Session_Name>`

If you resume an existing session, new measurements are appended to the report, new diagrams and waveform files are added to the session folder. Existing files are not deleted or replaced. Sessions data remain until you delete them in the "Results" tab of the session.

The report format can be defined in "RSScopeSuite" > "Settings" > "Report" for all compliance tests (see also Chapter 2.6, "Report configuration", on page 11). If you want to use special report settings for a session, you can define the format and contents of the report in the "Report Config" tab of the session.

All test results are listed in the "Results" tab. Reports can be provided in PDF, MSWord, or HTML format. To view and print PDF reports, you need a PDF viewer, for example, the Acrobat Reader.

The test report file can be created at the end of the test, or later in the "Session Selection" dialog.

To show a test report

1. In the R&S ScopeSuite window, select the compliance test to be performed.
2. Select the session name in the "Session Selection" dialog and click "Show report".

   The report opens in a separate application window, depending on the file format. You can check the test results and print the report.

To delete the results, diagrams and waveform files of a session

1. In the "Session Selection" dialog select the session and open it.
2. In the "Results" tab, select the result to be deleted.
3. Click "Remove".

4 D-PHY compliance tests

D-PHY Ethernet compliance tests require option R&S RTO/RTO6/RTP-K26.

The software closely follows the MIPI Alliance's **Conformance Test Suite for D-PHY Physical Layer Version 1.1 Revision 03**, dated June 5th, 2013. Should anything remain unclear in this manual, please refer to that CTS document, which is available for members of the MIPI Alliance at https://members.mipi.org/wg/All-Members/home/approved-specs.

Table 4-1: Overview of D-PHY compliance tests

Test Groups and Tests	see
Group 1 (7 tests): **Data Lane LP-TX Signaling Requirements** 1.1.1 – Data Lane LP-TX Thevenin Output High Level Voltage (V_{OH}) 1.1.2 – Data Lane LP-TX Thevenin Output Low Level Voltage (V_{OL}) 1.1.3 – Data Lane LP-TX 15%-85% Rise Time (T_{RLP}) 1.1.4 – Data Lane LP-TX 85%-15% Fall Time (T_{FLP}) 1.1.5 – Data Lane LP-TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$) 1.1.6 – Data Lane LP-TX Pulse Width of Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) 1.1.7 – Data Lane LP-TX Period of Exclusive-OR Clock ($T_{LP\text{-}PER\text{-}TX}$)	page 24
Group 2 (5 tests): **Clock Lane LP-TX Signaling Requirements** 1.2.1 – Clock Lane LP-TX Thevenin Output High Level Voltage (V_{OH}) 1.2.2 – Clock Lane LP-TX Thevenin Output Low Level Voltage (V_{OL}) 1.2.3 – Clock Lane LP-TX 15%-85% Rise Time (T_{RLP}) 1.2.4 – Clock Lane LP-TX 85%-15% Fall Time (T_{FLP}) 1.2.5 – Clock Lane LP-TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$)	page 36
Group 3 (16 tests): **Data Lane HS-TX Signaling Requirements** 1.3.1 – Data Lane HS Entry: Data Lane T_{LPX} Value 1.3.2 – Data Lane HS Entry: Data Lane $T_{HS\text{-}PREPARE}$ Value 1.3.3 – Data Lane HS Entry: Data Lane $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ Value 1.3.4 – Data Lane HS-TX Differential Voltages $V_{OD(0)}$ and $V_{OD(1)}$ 1.3.5 – Data Lane HS-TX Differential Voltage Mismatch ΔV_{OD} 1.3.6 – Data Lane HS-TX Single-Ended Output Voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ 1.3.7 – Data Lane HS-TX Static Common-Mode Voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$ 1.3.8 – Data Lane HS-TX Static Common-Mode Voltage Mismatch $\Delta V_{CMTX(1,0)}$ 1.3.9 – Data Lane HS-TX Dynamic Common-Level Variations Between 50-450 MHz $\Delta V_{CMTX(LF)}$ 1.3.10 – Data Lane HS-TX Dynamic Common-Level Variations Above 450 MHz $\Delta V_{CMTX(HF)}$ 1.3.11 – Data Lane HS-TX 20%-80% Rise Time t_R 1.3.12 – Data Lane HS-TX 80%-20% Fall Time t_F 1.3.13 – Data Lane HS Exit: $T_{HS\text{-}TRAIL}$ Value 1.3.14 – Data Lane HS Exit: 30%-85% Post-EoT Rise Time T_{REOT} 1.3.15 – Data Lane HS Exit: T_{EOT} Value 1.3.16 – Data Lane HS Exit: $T_{HS\text{-}EXIT}$ Value	page 46

Test Groups and Tests	see
Group 4 (18 tests): **Clock Lane HS-TX Signaling Requirements** 1.4.1 – Clock Lane HS Entry: T_{LPX} Value 1.4.2 – Clock Lane HS Entry: $T_{CLK-PREPARE}$ Value 1.4.3 – Clock Lane HS Entry: $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ Value 1.4.4 – Clock Lane HS-TX Differential Voltages $V_{OD(0)}$ and $V_{OD(1)}$ 1.4.5 – Clock Lane HS-TX Differential Voltage Mismatch ΔV_{OD} 1.4.6 – Clock Lane HS-TX Single-Ended Output Voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ 1.4.7 – Clock Lane HS-TX Static Common-Mode Voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$ 1.4.8 – Clock Lane HS-TX Static Common-Mode Voltage Mismatch $\Delta V_{CMTX(1,0)}$ 1.4.9 – Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450 MHz $\Delta V_{CMTX(LF)}$ 1.4.10 – Clock Lane HS-TX Dynamic Common-Level Variations Above 450 MHz $\Delta V_{CMTX(HF)}$ 1.4.11 – Clock Lane HS-TX 20%-80% Rise Time t_R 1.4.12 – Clock Lane HS-TX 80%-20% Fall Time t_F 1.4.13 – Clock Lane HS Exit: $T_{CLK-TRAIL}$ Value 1.4.14 – Clock Lane HS Exit: 30%-85% Post-EoT Rise Time T_{REOT} 1.4.15 – Clock Lane HS Exit: T_{EOT} Value 1.4.16 – Clock Lane HS Exit: $T_{HS-EXIT}$ Value 1.4.17 – Clock Lane HS Clock Instantaneous: UI_{INST} Value 1.4.18 – Clock Lane HS Clock Delta UI: (ΔUI) Value 1.4.19 – TX Spread Spectrum Clocking (SSC) requirements 1.4.20 – Clock Lane HS Clock Period Jitter	page 69
Group 5 (4 tests): **HS-TX Clock-to-Data Lane Timing Requirements** 1.5.1 – HS Entry: $T_{CLK-PRE}$ Value 1.5.2 – HS Exit: $T_{CLK-POST}$ Value 1.5.3 – HS Clock Rising Edge Alignment to First Payload Bit 1.5.4 – Data-to-Clock Skew ($T_{SKEW[TX]}$) 1.5.5 – Initial HS Skew Calibration Burst $T_{SKEWCAL-SYNC}$ and $T_{SKEWCAL}$ 1.5.6 – Periodic HS Skew Calibration Burst $T_{SKEWCAL-SYNC}$ and $T_{SKEWCAL}$ 1.5.8 – Alternate calibration sequence $T_{PREAMBLE}$ and T_{ALTCAL} 1.5.9 – Preamble sequence $T_{PREAMBLE}$ and $T_{EXTSYNC}$ 1.5.10 – Clock and data lane $TX_{HS-Idle}$ $T_{HS\ IDLE-POST}$, $T_{HS-IDLE-CLKHS0}$, $T_{HS-IDLE-PRE}$	page 98
Eye Test 1.4.18 – Clock Lane HS Clock Delta UI: (ΔUI) Value 1.4.20 – Clock Lane HS Clock Period Jitter 1.5.7 – HS Data and Clock Eye Diagram	

Any D-PHY configuration consists of at least one clock lane module, and one or several data lane modules. Each module provides a synchronized connection between master and slave. During normal operation, a lane switches between the modes "low power" (LP) and "high speed" (HS). High speed functions are used for HS data transmission in bursts with an arbitrary number of payload data bytes. Low power functions

are mainly used for control, but have other optional use cases, like LP escape mode. The presence of HS and LP functions is correlated.

4.1 Starting D-PHY compliance tests

Before you run the test, complete the following actions:

- Initial setup of the equipment, see Chapter 2.2, "Installing software and license", on page 7
- LAN connection of the oscilloscope and the computer running the R&S ScopeSuite, see Chapter 2.5, "Connecting the R&S RTO/RTO6/RTP", on page 9

1. Select "D-PHY" in the R&S ScopeSuite start window.
2. In the "Session Selection" dialog, choose the D-PHY standard version.
   You can select one of the following : "1.1", "1.2", "2.0", "2.1", "2.5".
3. Add a new test session and name it. See Chapter 3.1, "Starting a test session", on page 12.
4. Open the test session.
5. Adjust the test configuration settings if necessary. See:
   - Chapter 3.2.1.1, "Limit manager", on page 15
   - Chapter 4.2, "Test configuration for D-PHY", on page 20
6. Select/check the test cases that you want to run and click "Test Single"/"Test checked".
7. A step-by step guide explains the following individual setup steps. When you have finished all steps of the step-by-step guide, the compliance test runs automatically.

4.2 Test configuration for D-PHY

The test configuration consists of the general configuration settings as described in Chapter 3.2, "Configuring the test", on page 13, and some additional test-specific configuration settings, described below:

- Low-power properties for DUT lanes in low power (LP) mode, groups 1 and 2.
- High speed for DUT lanes in high speed (HS) mode, groups 3, 4 and 5.

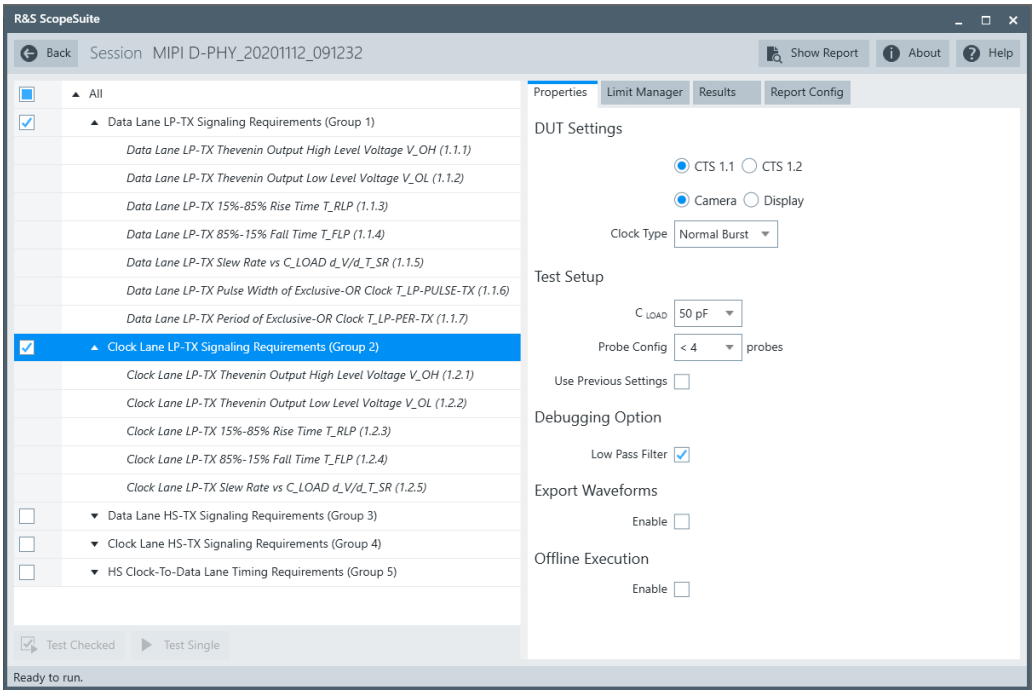


Figure 4-1: LP Configuration for D-PHY compliance test cases, Groups 1 and 2

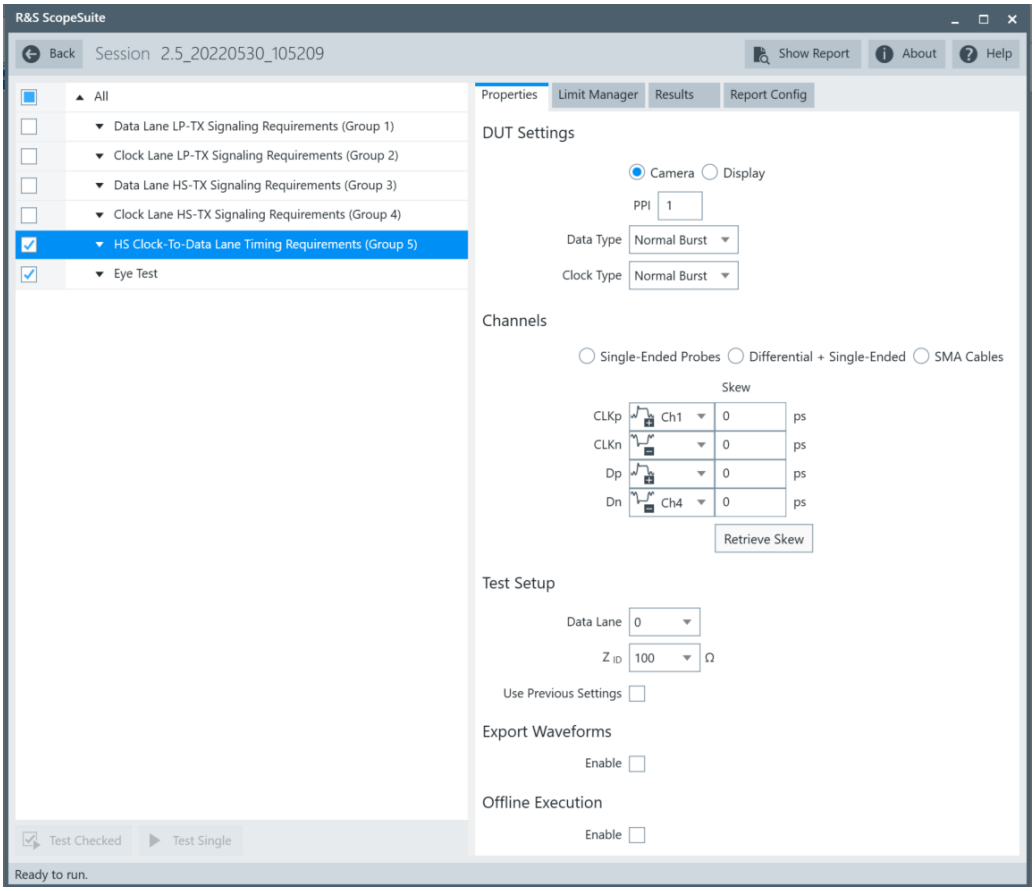


Figure 4-2: HS configuration for D-PHY compliance test cases, Groups 3, 4 and 5

Some fields are shared between the "Properties" for the high-speed and low-power modes, and other compliance tests in the R&S ScopeSuite.

DUT
Defines if the DUT is a camera (CSI-2) or display (DSI).

Bitrate ← DUT
If the bitrate of the DUT is known, enable "Bitrate" and enter the bitrate value in *Mbps*. This is useful if the signal is noisy. This selection is only applicable for Group 3 test cases.

Data/Clock Type ← DUT
Sets the data/clock type according to your DUT:

- If the DUT has a burst or non-continuous clock, select "Normal Burst".
- If the DUT has a partial burst clock, select "HS Entry and Exit".
- If the DUT has a continuous clock, select "All Continuous".

Channel selection
Selects the channels for CLK_p, CLK_n, D_p and D_n waveforms.

Select, if you are using a "Single-Ended Probes", "Differential + Single-Ended Probes" and "SMA Cables".

You can also define a skew value for each channel.

When opening a new session, the skew values are read from the oscilloscope and the skew fields are updated. To get the skew values set in the oscilloscope later, press "Retrieve Skew".

Data Lane
Select the data lane number to be tested. This selection is only applicable for Group 1, 3 and 5 test cases. Default selection is data lane "0".

C_{LOAD}
- If a C_{LOAD} test fixture with 50 pF termination capacitance is used, as required in the MIPI Alliance Specification for D-PHY, version 1.1, select "50 pF".
- If the 50 pF C_{LOAD} fixture is removed, select "Open".

The test results may not be valid, if no C_{LOAD} test fixture with 50 pF termination capacitance is used. The optional "Open" configuration setting is used to provide a qualitative estimate of the amount of C_{LOAD} contributed by the DUT's PCB.

Z_{ID}
The software supports all three cases of terminations, Z_{ID}:
- 100 ohms (nominal load)
- 80 ohms (minimum load)
- 125 ohms (maximum load)

Specify the termination which is applied to the DUT. This selection is only applicable for Group 3, 4 and 5 test cases.

Use Previous Settings
Check this if you want to use the previous settings (which include trigger conditions, vertical scale and horizontal time scale) for a new execution of the same group of test cases with the same configurations.

If this is not checked, the software:
- For LP configuration: uses the pre-defined trigger conditions, vertical scale and horizontal time scale.
- For HS configuration: goes through a set of pre-defined routines to determine the best trigger conditions and horizontal time scale.

Low Pass Filter
This setting is only applicable to Group 1 and Group 2 tests.

If "Low Pass Filter" is enabled, the software applies a 4^{th} order Butterworth low pass filter with a cutoff frequency of 400 MHz to the input signal, as required in the MIPI Alliance Specification for D-PHY, version 1.1. Keep this option enabled, as some measurements are sensitive to high-frequency noise.

Reference Channel
Select the "Short", "Standard" or "Long" for Reference Channel setting. The software the emulate the reference channel when performing HS-TX Data and Clock Eye Diagram. Select "None" if reference channel is present physically.

Number of Acquisitions
Sets the number of UI to construct the eye diagrams. Note that a greater value of the setting will require more processing time.

Export Waveform
Enables you to export a waveform. You can later load the waveforms to run the tests in the offline mode, see Offline Execution.

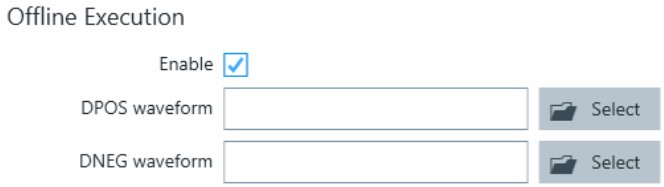
You can define an export directory, or use the default one:

```
MyDocuments\Rohde-Schwarz\RSScopeSuite\<Version>\Waveforms\
<ComplianceTest>\<SessionType>\<SessionName>
```

For example:

```
%ProgramData%\Rohde-Schwarz\RSScopeSuite\4.80.0\Sessions\D-PHY
```

Offline Execution



If enabled, allows you to use exported waveforms as a source for the execution of the compliance test.

You can select one waveform for each needed signal.

4.3 Data lane LP-TX signaling requirements (Group 1)

The purpose of Group 1 test cases is to verify various requirements specific to data lane low power (LP) signaling.

Group 1 consists of seven test cases, described in Chapter 4.3.3, "Measurements", on page 27. They perform related LP-TX measurements on a single data lane LP transmit waveform sequence.

The software is intended to facilitate the execution of a set of LP-TX measurements on a pair of captured LP data lane waveforms with ULPS Entry sequence.

These test cases are typically performed on CSI-2 and DSI Master devices, only.

4.3.1 Test setup

Table 4-2: Equipment for Group 1 Data Lane LP-TX Signaling Requirements test

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 / RTP with 4 channels and at least 4 GHz bandwidth	1
Probes	Differential probes: at least 4 GHz bandwidth, or Single-ended probes: at least 4 GHz bandwidth	2 (*)
Test fixture	UNH-IOL MIPI D-PHY Capacitive Load $©_{LOAD}$)[1]	1
DUT	Any MIPI D-PHY CSI-2 or DSI device	1
* In this group of tests, sampling the signals requires 2 probes: either single-ended, or differential used in single-ended mode.		
[1] We recommend to use a MIPI D-PHY Capacitive Load $©_{LOAD}$) test fixture from the University of New Hampshire InterOperability Laboratory (UNH-IOL). Refer to https://www.iol.unh.edu/services/testing/mipi/fixtures.php for details.		

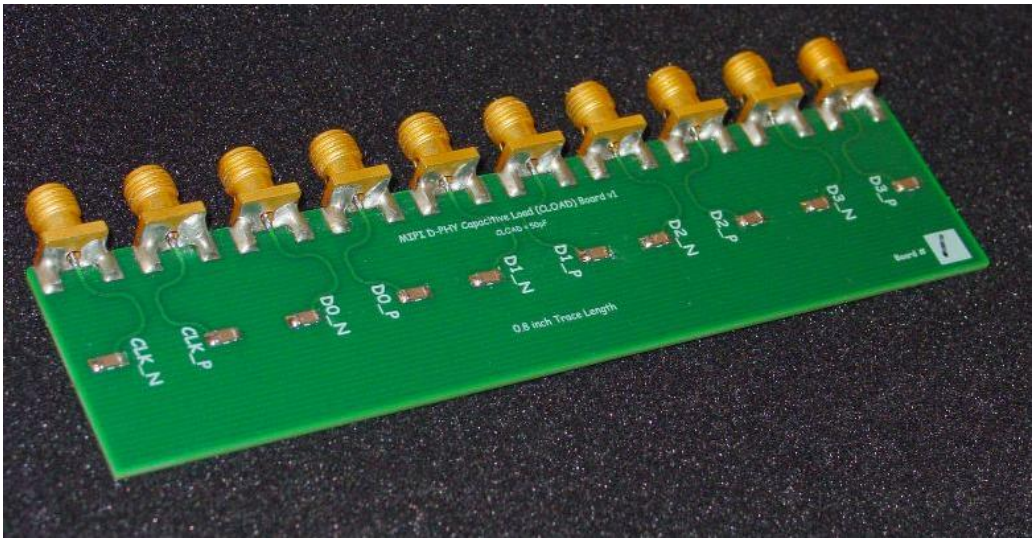
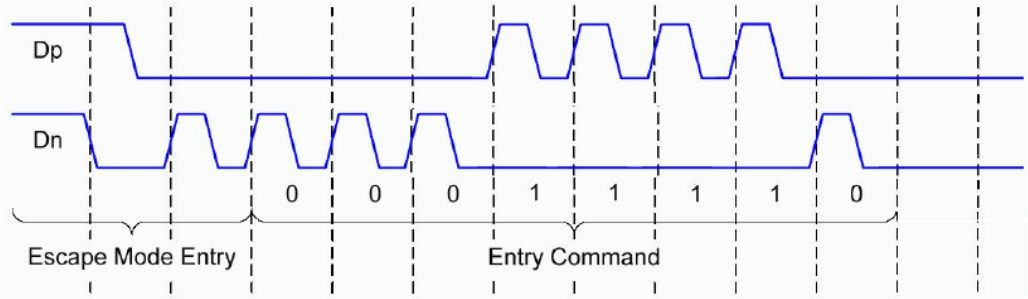


Figure 4-3: MIPI D-PHY Capacitive Load test fixture from UNH-IOL

Waveform requirements

Group 1 test cases require the DUT to source a MIPI D-PHY LP data lane ULPS Entry sequence. The figure below shows a typical ULPS Entry sequence waveform. It consists of:

- (a) Escape Mode Entry: LP-11>10>00>01>00
- (b) Ultra-Low Power State Entry Command Pattern: 00011110



The software requires a pair of waveforms containing (a) and (b) as stated above to measure correctly and perform the test successfully.

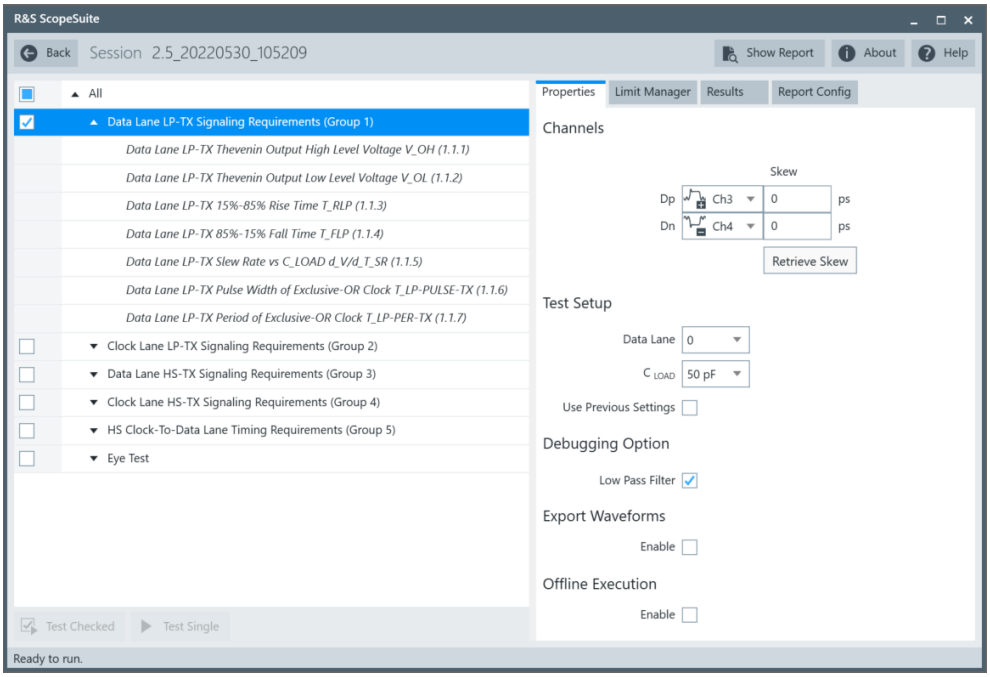
Settings in the "LP Configuration" dialog box

See also: Chapter 4.2, "Test configuration for D-PHY", on page 20.

- **Channels**
  Select the channels for the measurement and set or retrieve the skew.
- **Data Lane**
  If the DUT implements multiple data lanes, select which pair of data lanes is to be tested.
- **C_{LOAD} Requirements**
  Select "C_{LOAD}" to be "50 pF" (which is also the default selection).
  Most of the Group 1 tests require a 50 pF C_{LOAD} test fixture, which is practically used as maximum capacitive load. Some other tests are independent of termination capacitance. For procedural consistency, all tests are performed using a 50 pF C_{LOAD} test fixture.
- **Low Pass Filter**
  Enable the "Low Pass Filter". For details regarding this filter, see Chapter 4.2, "Test configuration for D-PHY", on page 20.

4.3.2 Performing Group 1 test cases

1. Start the test as described in Chapter 4.1, "Starting D-PHY compliance tests", on page 20.
2. Select the test case group: "Data Lane LP-TX Signaling Requirements (Group 1)".



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.

4. Follow the instructions of the step-by step guide.
   This group of tests uses the MIPI D-PHY Capacitive Load ©$_{LOAD}$) test fixture from the UNH-IOL. The C_{LOAD} fixture provides 50 pF capacitive load.
   The data signals can be tapped on the DUT or the C_{LOAD} or even the SMA cables between the DUT and the C_{LOAD}.
   Switch the probes to tap a specific pair of data lanes under test, if the DUT implements multiple data lanes.
   When you have finished all steps, the compliance test runs automatically.

Further steps:

- Chapter 3.3, "Getting test results", on page 16

4.3.3 Measurements

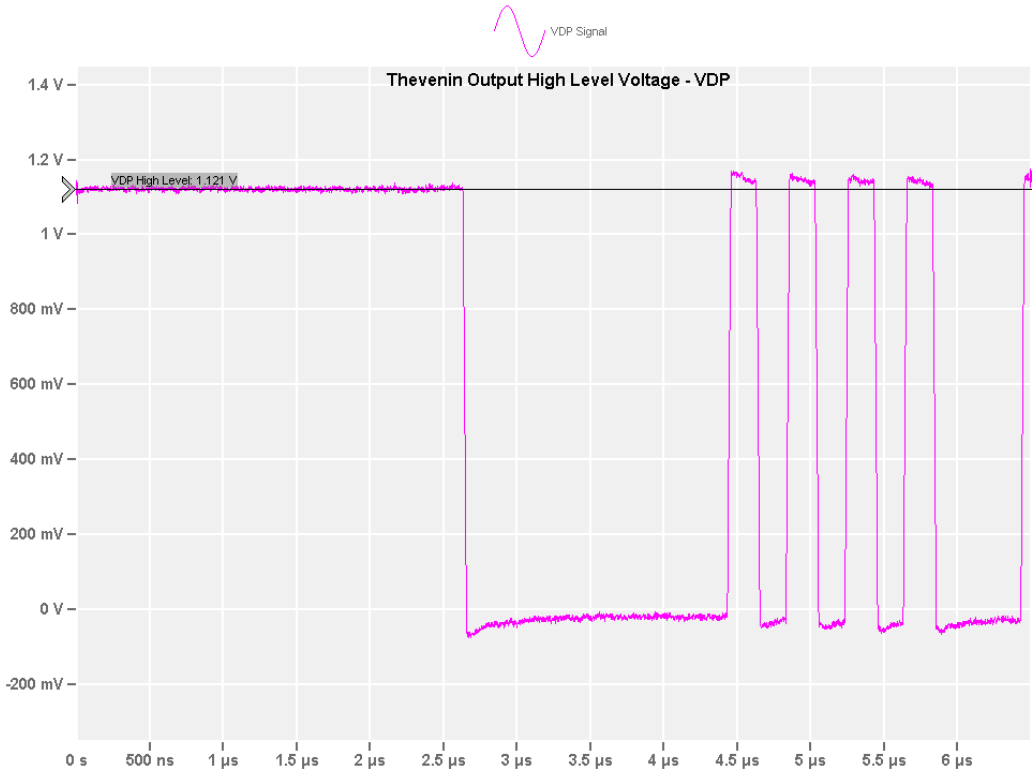
4.3.3.1 Test 1.1.1 – Data Lane LP-TX Thevenin Output High Level Voltage (V_{OH})

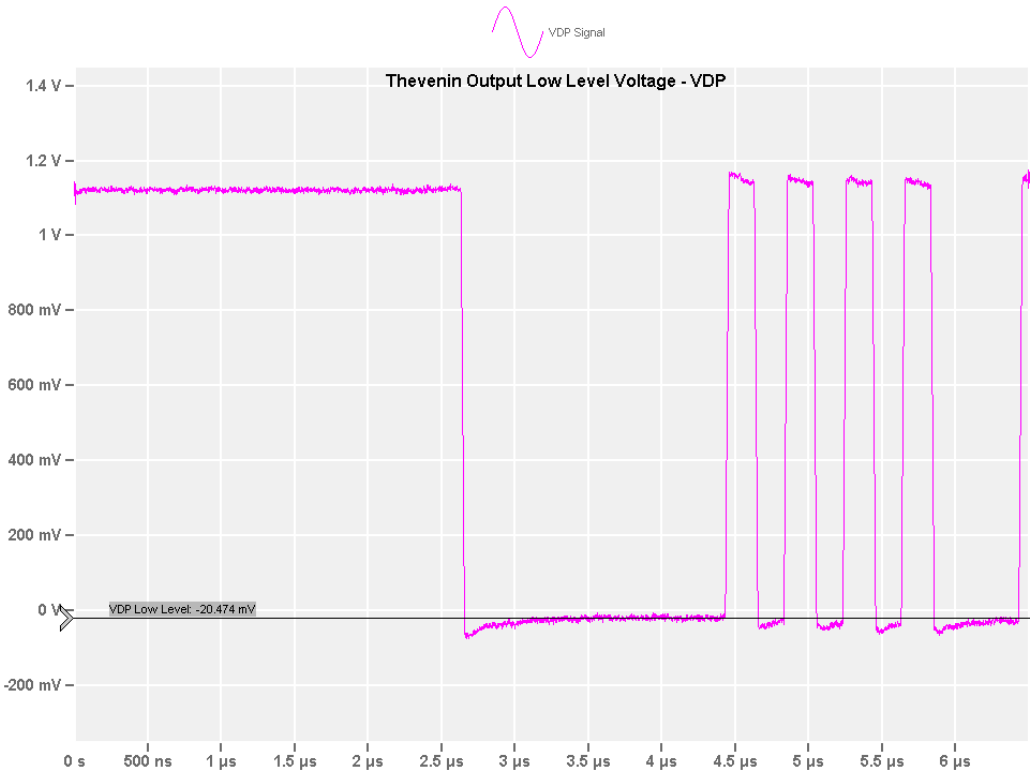
The purpose of this test case is to verify that the Thevenin Output High Level Voltage (V_{OH}) of the DUT's data lane LP transmitter is within the conformance limits. The conformance range for V_{OH} is between 1.1 and 1.3 Volts.

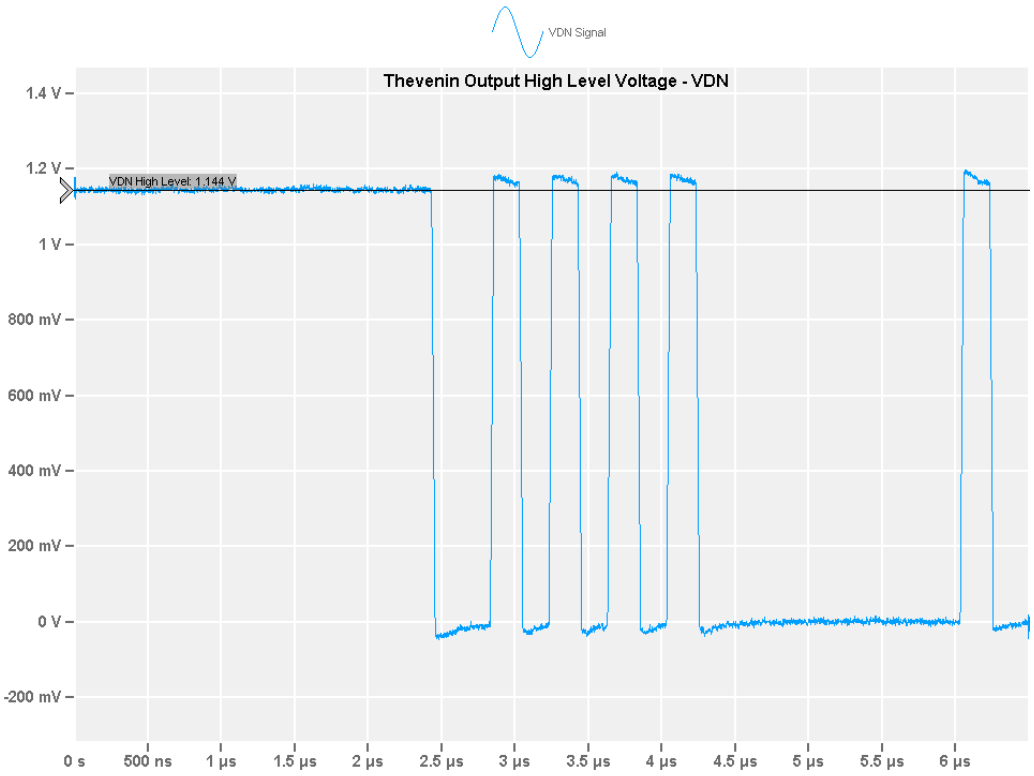
V_{OH} is measured as the mode of all waveform samples, which are greater than 50% of the absolute peak-to-peak V_{DP} and V_{DN} signal amplitudes, and across all LP-1 states in a single LP Escape Mode sequence.

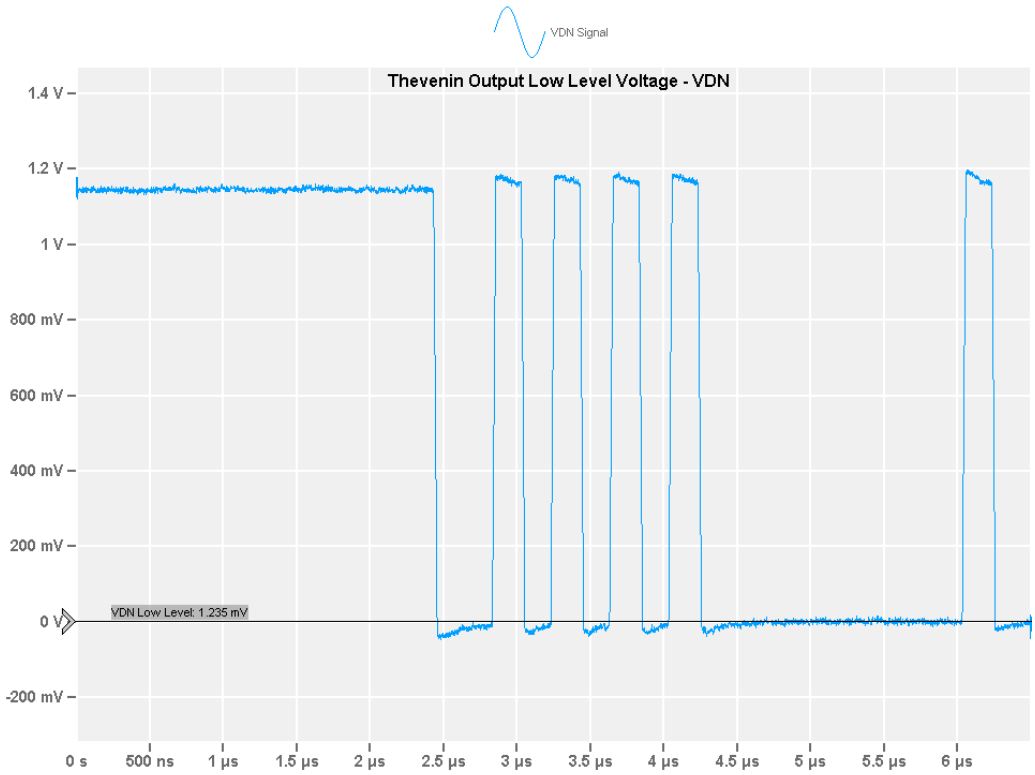
A ULPS Entry sequence is specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} waveforms for each data lane.

An example is shown below.




VDP Signal
Thevenin Output Low Level Voltage - VDP
1.4 V
1.2 V
1 V
800 mV
600 mV
400 mV
200 mV
0 V
-200 mV
VDP Low Level: -20.474 mV
0 s
500 ns
1 µs
1.5 µs
2 µs
2.5 µs
3 µs
3.5 µs
4 µs
4.5 µs
5 µs
5.5 µs
6 µs


VDN Signal
Thevenin Output High Level Voltage - VDN
1.4 V
1.2 V
1 V
800 mV
600 mV
400 mV
200 mV
0 V
-200 mV
VDN High Level: 1.144 V
0 s
500 ns
1 µs
1.5 µs
2 µs
2.5 µs
3 µs
3.5 µs
4 µs
4.5 µs
5 µs
5.5 µs
6 µs



4.3.3.2 Test 1.1.2 – Data Lane LP-TX Thevenin Output Low Level Voltage (V_{OL})

The purpose of this test case is to verify that the Thevenin Output Low Level Voltage (V_{OL}) of the DUT's data lane LP transmitter is within the conformance limits. The conformance range for V_{OL} is between -50 and +50 mV.

V_{OL} is measured as the mode of all waveform samples, which are less than 50% of the absolute peak-to-peak V_{DP} and V_{DN} signal amplitudes, and across all LP-0 states in a single LP Escape Mode sequence.

A ULPS Entry sequence is specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} waveforms for each data lane.

An example is shown below.

4.3.3.3 Test 1.1.3 – Data Lane LP-TX 15%-85% Rise Time (T_{RLP})

The purpose of this test case is to verify that the 15%-85% Rise Time (T_{RLP}) of the DUT's data lane LP transmitter is within the conformance limits. The conformance range for TRLP is less than 25 ns.

Using the measured V_{OH} and V_{OL} LP-TX Thevenin Output Voltage Levels as references, the 15%-85% Rise Time (T_{RLP}) is measured for each rising edge of the V_{DP} and V_{DN} waveforms. The mean value across all observed rising edges are computed to produce the final T_{RLP} result.

A ULPS Entry sequence is specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} waveforms for each data lane.

An example is shown in Figure 4-4

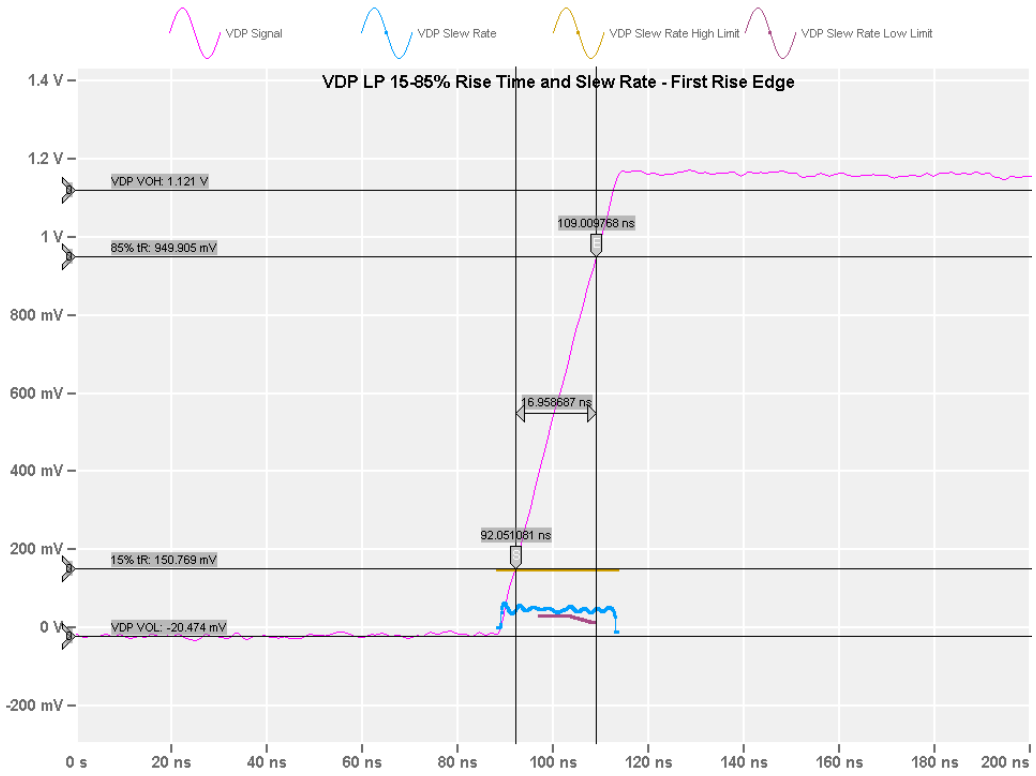


Figure 4-4: Typical result of a data lane LP-TX 15%-85% rise time measurement for V_DP

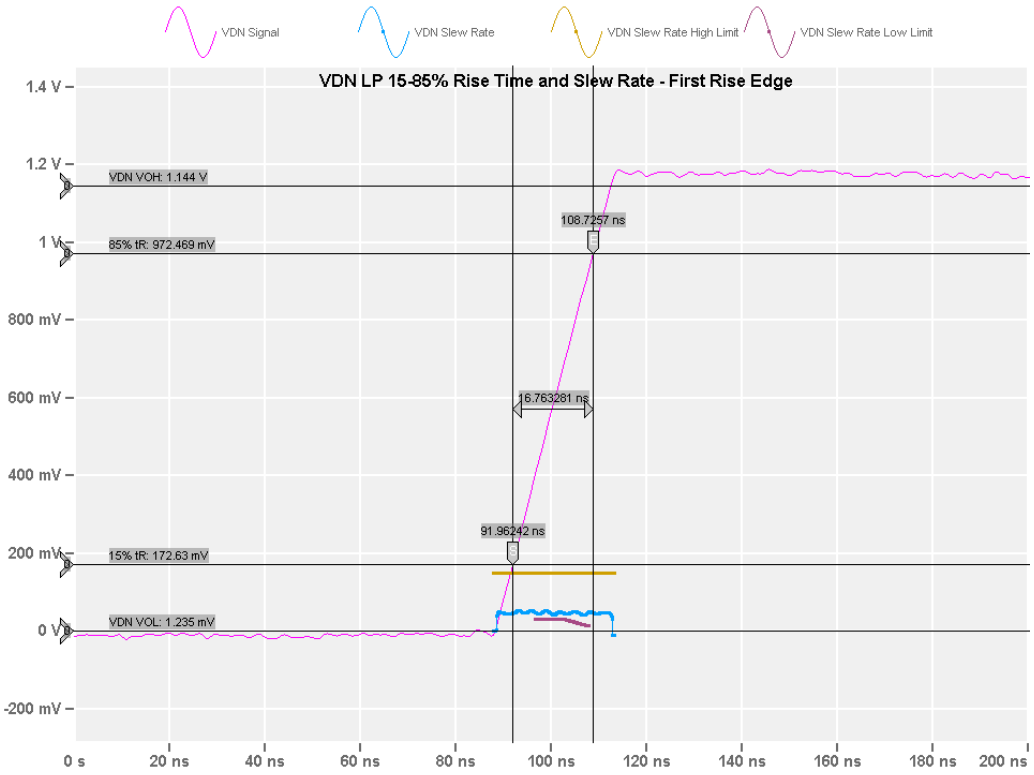


Figure 4-5: Typical result of a data lane LP-TX 15%-85% rise time measurement for V_DN

4.3.3.4 Test 1.1.4 – Data Lane LP-TX 85%-15% Fall Time (T_{FLP})

The purpose of this test case is to verify that the 85%-15% Fall Time (T_{FLP}) of the DUT's data lane LP transmitter is within the conformance limits. The conformance range for T_{FLP} is less than 25 ns.

Using the measured V_{OH} and V_{OL} LP-TX Thevenin Output Voltage Levels as references, the 85%-15% Fall Time (T_{FLP}) is measured for each falling edge of the V_{DP} and V_{DN} waveforms. The mean value across all observed falling edges are computed to produce the final T_{FLP} result.

A ULPS Entry sequence is specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} waveforms for each data lane.

An example is shown in Figure 4-6.

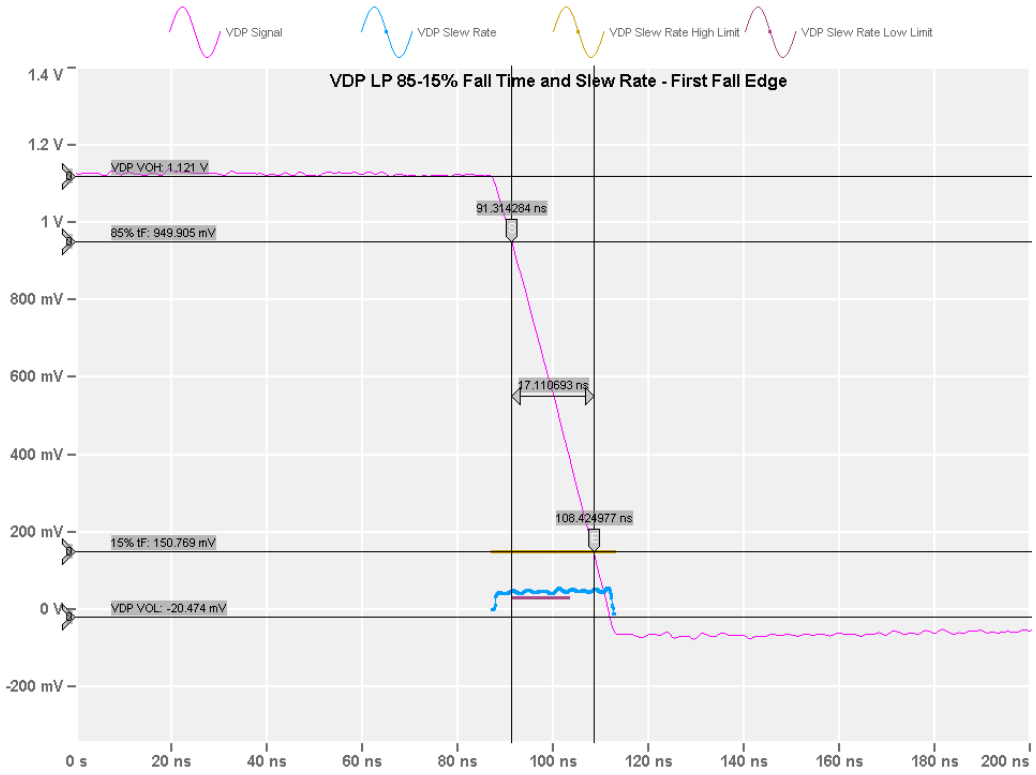


Figure 4-6: Typical result of a data lane LP-TX 85%-15% Fall time and slew rate measurement for V_DP

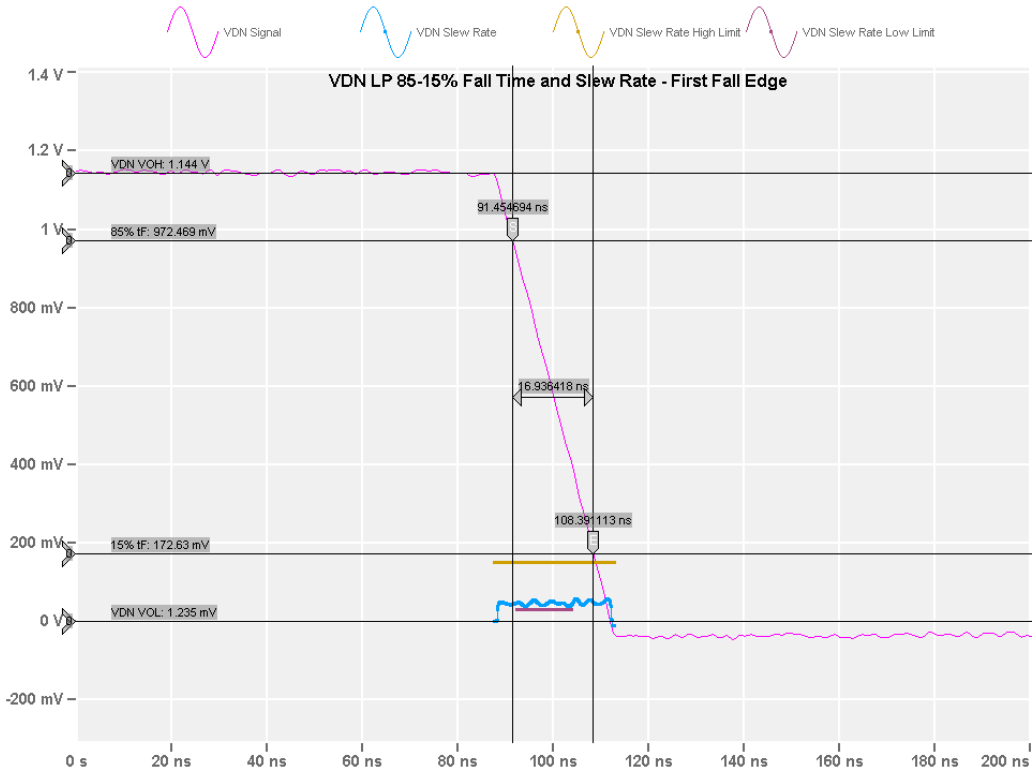


Figure 4-7: Typical result of a data lane LP-TX 85%-15% Fall time and slew rate measurement for V_DN

4.3.3.5 Test 1.1.5 – Data Lane LP-TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$)

The purpose of this test case is to verify that the Slew Rate ($\delta V/\delta t_{SR}$) of the DUT's data lane LP transmitter is within the conformance limits, for specific capacitive loading conditions. The conformance ranges are specified below, in the lists for falling and rising edges.

The Slew Rate is computed and measured independently for each edge of the V_{DP} and V_{DN} signals using a 50 mV vertical window. The Slew Rate curve is computed for a single edge, using the sliding window technique.

For **falling edges**:

- The final averaged maximum $\delta V/\delta t_{SR}$ result is computed over the entire vertical edge region. The conformance range is less than 150 V/µs.
- The final averaged minimum $\delta V/\delta t_{SR}$ result is computed over 400-930 mV region. The conformance range is greater than 30 V/µs.

For **rising edges**:

- The final averaged maximum $\delta V/\delta t_{SR}$ result is computed over the entire vertical edge region. The conformance range is less than 150 V/µs.
- The final averaged minimum $\delta V/\delta t_{SR}$ result is computed over 400-700 mV region. The conformance range is greater than 30 V/µs.

- The final averaged minimum $\delta V/\delta t_{SR}$ margin result is computed over 700-930 mV region. The minimum limit is defined by the equation 30 - 0.075·(V_{O-INST} - 700). The conformance range is greater than 0 V/µs.

A ULPS Entry sequence is specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} waveforms for each data lane.

Examples are shown in Figure 4-6, Figure 4-5, Figure 4-4, and Figure 4-7.

4.3.3.6 Test 1.1.6 – Data Lane LP-TX Pulse Width of Exclusive-OR Clock ($T_{LP-PULSE-TX}$)

The purpose of this test case is to verify that the pulse width ($T_{LP-PULSE-TX}$) of the DUT's data lane LP transmitter Exclusive-OR (XOR) clock is within the conformance limits. The $T_{LP-PULSE-TX}$ conformance range is composed of two parts:

- The first LP XOR clock pulse after a Stop state is wider than 40 ns.
- The minimum of all other LP XOR clock pulses is wider than 20 ns.

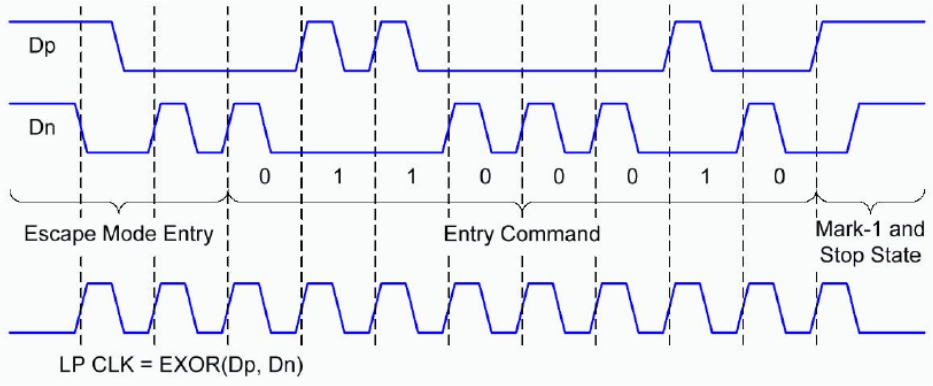


Figure 4-8: Graphical example of XOR clock generation according to the specification

The LP XOR clock is computed separately, using the maximum trip-level threshold voltage of 930 mV and the minimum trip-level threshold voltage of 500 mV.

A ULPS Entry sequence is specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} waveforms for each data lane.

An example is shown in Figure 4-9.

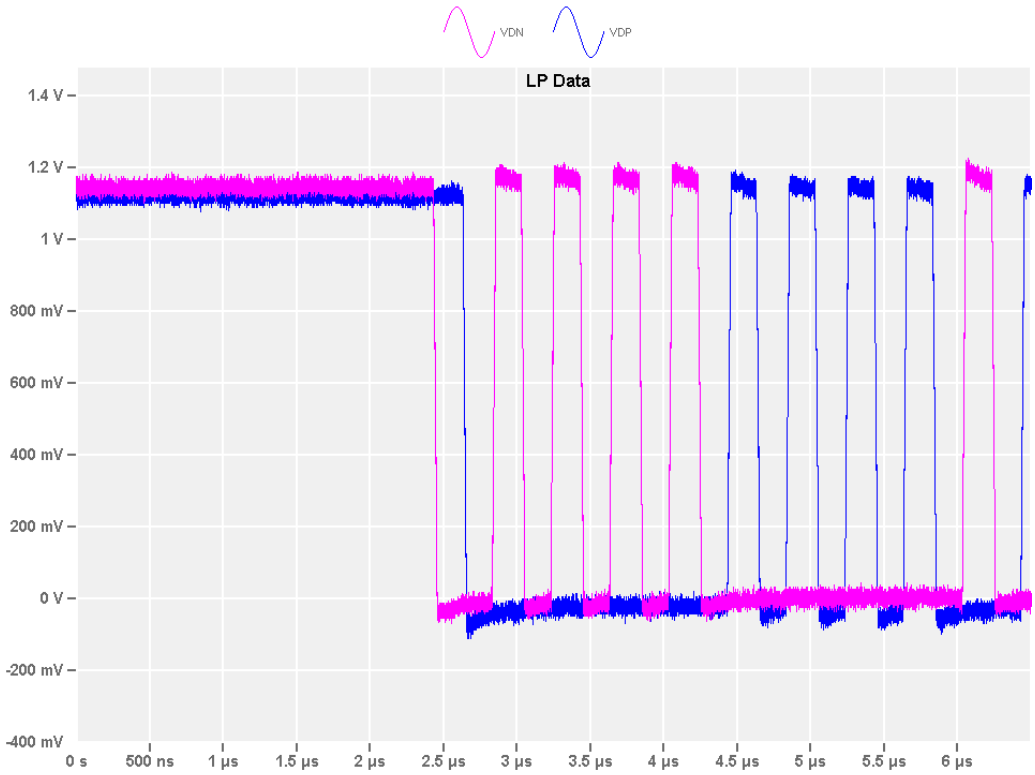


Figure 4-9: Typical result of a data lane LP-TX pulse width of XOR clock measurement

4.3.3.7 Test 1.1.7 – Data Lane LP-TX Period of Exclusive-OR Clock ($T_{LP\text{-}PER\text{-}TX}$)

The purpose of this test case is to verify that the pulse width ($T_{LP\text{-}PER\text{-}TX}$) of the DUT's data lane LP transmitter XOR clock is within the conformance limits. The $T_{LP\text{-}PER\text{-}TX}$ conformance range is composed of two parts:

- Minimum $T_{LP\text{-}PER\text{-}TX}$ rising-edge-to-rising-edge period is greater than 90 ns.
- Minimum $T_{LP\text{-}PER\text{-}TX}$ falling-edge-to-falling-edge period is greater than 90 ns.

For a graphical example of XOR clock generation, see Figure 4-8.

The LP XOR clock is computed separately using the maximum trip-level threshold voltage of 930 mV and the minimum trip-level threshold voltage of 500 mV.

A ULPS Entry sequence is specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} waveforms for each data lane.

An example is shown in Figure 4-9.

4.4 Clock lane LP-TX signaling requirements (Group 2)

The purpose of Group 2 test cases is to verify various requirements specific to clock lane low power (LP) signaling.

Group 2 consists of five test cases, described in Chapter 4.4.3, "Measurements", on page 39. They perform related LP-TX measurements on a single clock lane LP transmit waveform sequence.

The software is intended to facilitate the execution of a set of LP-TX measurements on a pair of captured LP clock lane waveforms with ULPS Entry and Exit sequence.

These test cases are typically performed on CSI-2 and DSI Master devices, only.

4.4.1 Test setup

Table 4-3: Equipment for Group 2 Clock Lane LP-TX Signaling Requirements test

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 / RTP with 4 channels and at least 4 GHz bandwidth	1
Probes	Differential probes: at least 4 GHz bandwidth, or Single-ended probes: at least 4 GHz bandwidth	2 (*)
Test fixture	UNH-IOL MIPI D-PHY Capacitive Load $©_{LOAD}$)[1]	1
DUT	Any MIPI D-PHY CSI-2 or DSI device	1
* In this group of tests, sampling the signals requires 2 probes: either single-ended, or differential used in single-ended mode.		
[1] We recommend to use a MIPI D-PHY Capacitive Load $©_{LOAD}$) test fixture from the University of New Hampshire InterOperability Laboratory (UNH-IOL). Refer to https://www.iol.unh.edu/services/testing/mipi/fixtures.php for details.		

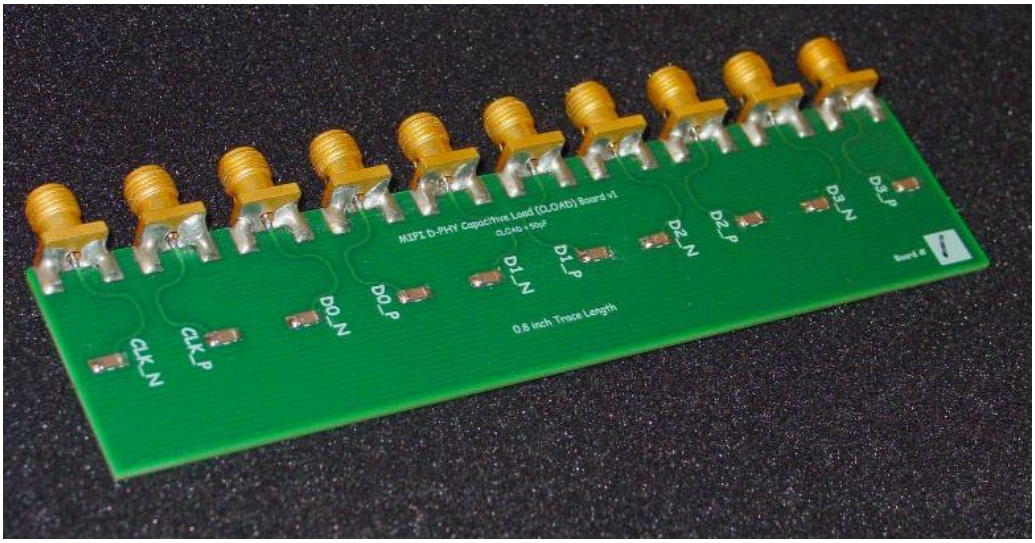


Figure 4-10: MIPI D-PHY Capacitive Load test fixture from UNH-IOL

Waveform requirements

Group 2 test cases require the DUT to source a MIPI D-PHY LP data lane ULPS Entry sequence and an Exit sequence on the clock lane.

- A typical ULPS Entry sequence waveform consists of: LP-11>10>00
- A typical ULPS Exit sequence waveform consists of: LP-00>10>11

The software requires 2 pairs of waveforms containing ULPS Entry and Exit sequences as stated above to measure correctly and perform the test successfully.

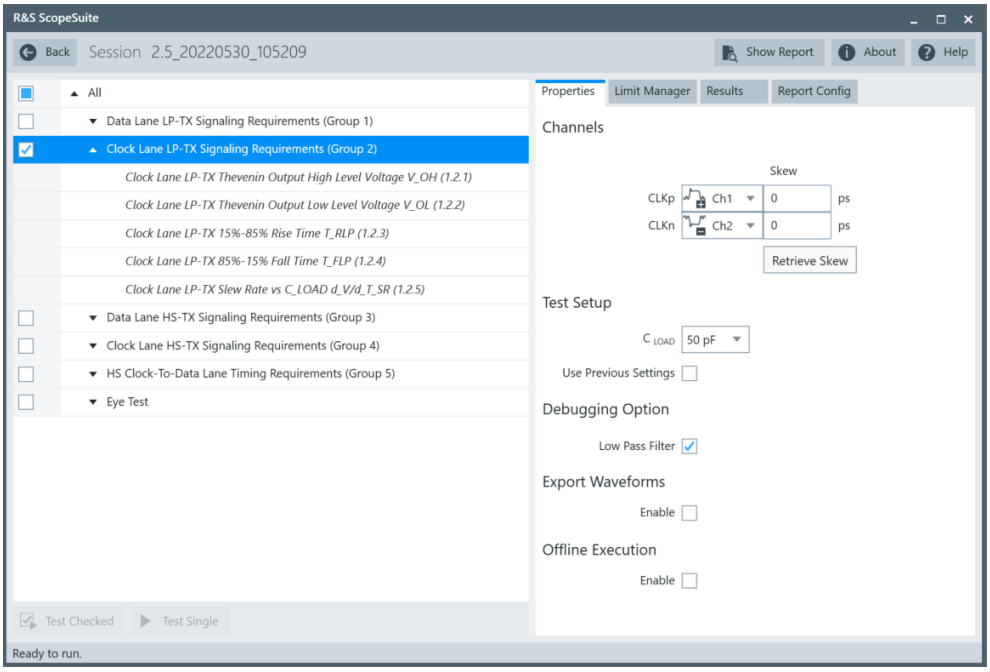
Settings in the "LP Configuration" dialog box

See also: Chapter 4.2, "Test configuration for D-PHY", on page 20.

- **Channels**
  Select the channels for the measurement and set or retrieve the skew.
- **C_{LOAD} Requirements**
  Select "C_{LOAD}" to be "50 pF" (which is also the default selection).
  Most of the Group 2 tests require a 50 pF C_{LOAD} test fixture, which is practically used as maximum capacitive load. Some other tests are independent of termination capacitance. For procedural consistency, all tests are performed using a 50 pF C_{LOAD} test fixture.
- **Low Pass Filter**
  Enable the "Low Pass Filter". For details regarding this filter, see Chapter 4.2, "Test configuration for D-PHY", on page 20.

4.4.2 Performing Group 2 test cases

1. Start running the tests as described in Chapter 4.1, "Starting D-PHY compliance tests", on page 20.
2. Select "Clock Lane LP-TX Signaling Requirements (Group 2)".



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.

4. Follow the instructions of the step-by step guide.
   This group of tests uses the MIPI D-PHY Capacitive Load ©$_{LOAD}$) test fixture from the UNH-IOL. The C_{LOAD} fixture provides 50 pF capacitive load.
   The clock signals can be tapped on the DUT or the C_{LOAD} or even the SMA cables between the DUT and the C_{LOAD}. The Group 2 test cases do not require data signals.
   When you have finished all steps, the compliance test runs automatically.

Further steps:

- Chapter 3.3, "Getting test results", on page 16

4.4.3 Measurements

4.4.3.1 Test 1.2.1 – Clock Lane LP-TX Thevenin Output High Level Voltage (V_{OH})

The purpose of this test case is to verify that the Thevenin Output High Level Voltage (V_{OH}) of the DUT's clock lane LP transmitter is within the conformance limits. The conformance range for V_{OH} is between 1.1 and 1.3 Volts.

V_{OH} is measured as the mode of all waveform samples that are greater than 50% of the absolute peak-to-peak V_{DP} and V_{DN} signal amplitudes, and across all LP-1 states in a single LP Escape Mode sequence.

A ULPS Entry sequence is specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} clock lane waveforms.

An example is shown in the figures below.

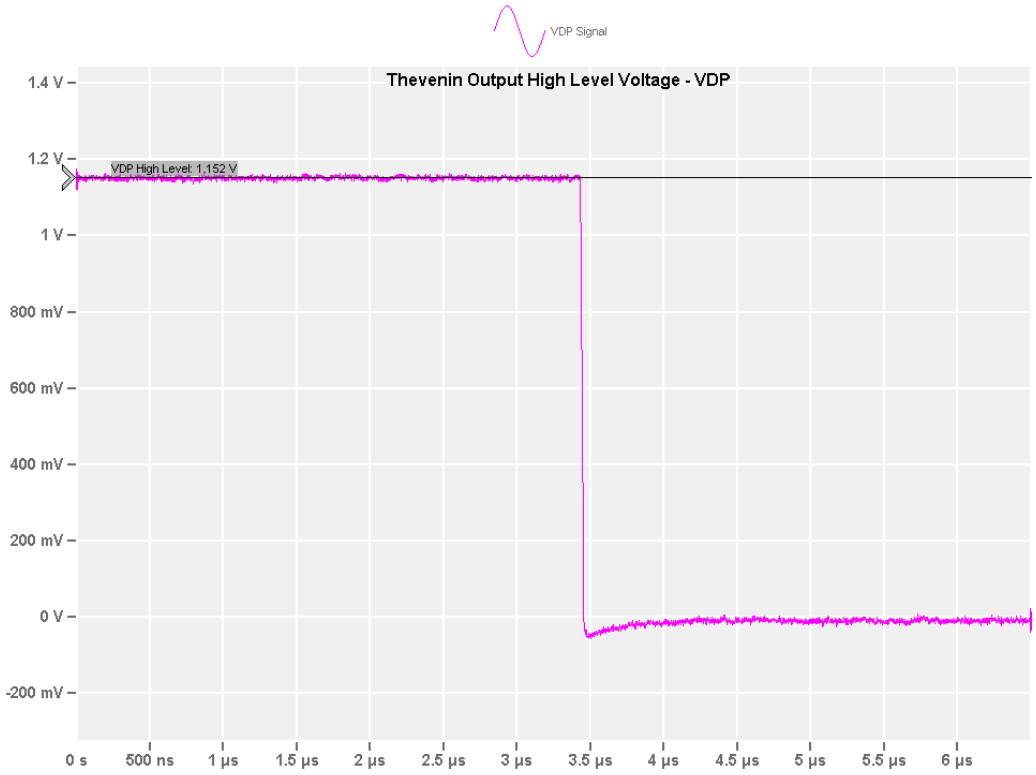


Figure 4-11: Typical result of a clock lane LP-TX Thevenin output High Level measured for VDP

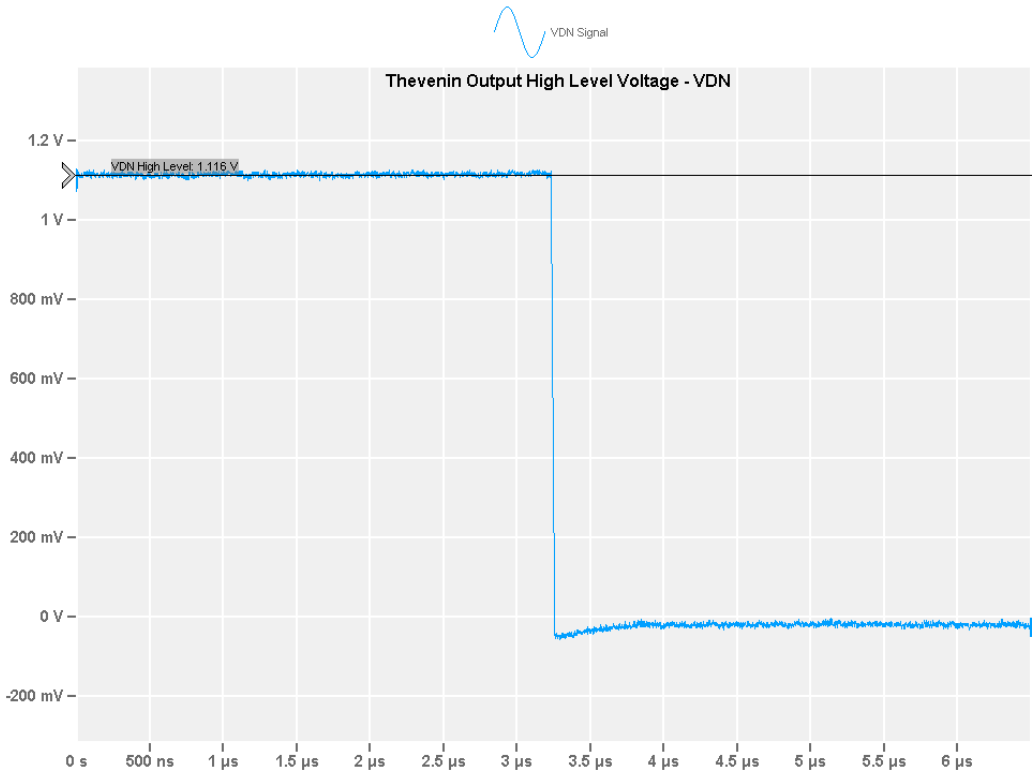


Figure 4-12: Typical result of a clock lane LP-TX Thevenin output High Level measured for VDN

4.4.3.2 Test 1.2.2 – Clock Lane LP-TX Thevenin Output Low Level Voltage (V_{OL})

The purpose of this test case is to verify that the Thevenin Output Low Level Voltage (V_{OL}) of the DUT's clock lane LP transmitter is within the conformance limits. The conformance range for V_{OL} is between -50 and +50 mV.

V_{OL} is measured as the mode of all waveform samples that are less than 50% of the absolute peak-to-peak V_{DP} and V_{DN} signal amplitudes, and across all LP-0 states in a single LP Escape Mode sequence.

A ULPS Entry sequence is specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} clock waveforms.

An example is shown in Figure 4-11.

4.4.3.3 Test 1.2.3 – Clock Lane LP-TX 15%-85% Rise Time (T_{RLP})

The purpose of this test case is to verify the 15%-85% Rise Time (T_{RLP}) of the DUT's clock lane LP transmitter is within the conformance limits. The conformance range for T_{RLP} is less than 25 ns.

Using the measured V_{OH} and V_{OL} LP-TX Thevenin Output Voltage Levels as references, the 15%-85% rise time (T_{RLP}) is measured independently for the rising edges of

the V_{DP} and V_{DN} waveforms. A ULPS Exit sequence is specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} clock lane waveforms.

Examples are shown in Figure 4-13 and Figure 4-14.

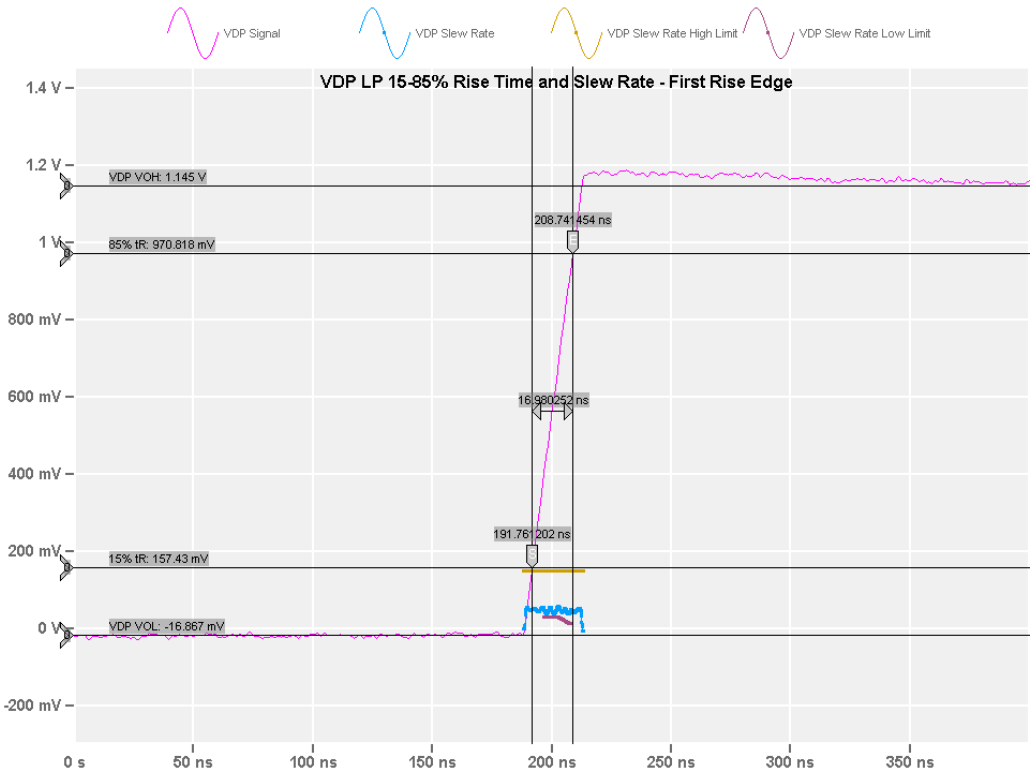


Figure 4-13: Typical result of a clock lane LP-TX 15%-85% rise time and slew rate measurement for V_DP

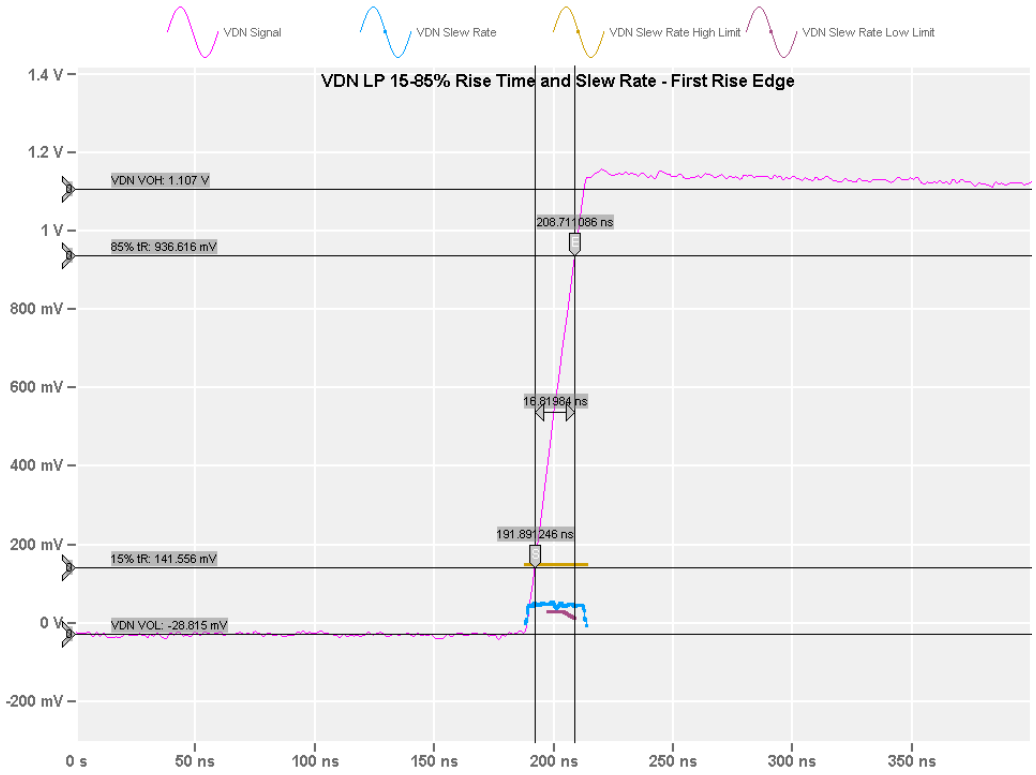


Figure 4-14: Typical result of a clock lane LP-TX 15%-85% rise time and slew rate measurement for V_DN

4.4.3.4 Test 1.2.4 – Clock Lane LP-TX 85%-15% Fall Time (T_{FLP})

The purpose of this test case is to verify the 85%-15% Fall Time (T_{FLP}) of the DUT's clock lane LP transmitter is within the conformance limits. The conformance range for T_{FLP} is less than 25 ns.

Using the measured V_{OH} and V_{OL} LP-TX Thevenin Output Voltage Levels as references, the 85%-15% fall time (T_{FLP}) is measured independently for the falling edges of the V_{DP} and V_{DN} waveforms.

A ULPS Entry sequence is specified for this test. The measurement is performed separately on both VDP and VDN Clock Lane waveforms.

Examples are shown in Figure 4-15 and Figure 4-16.

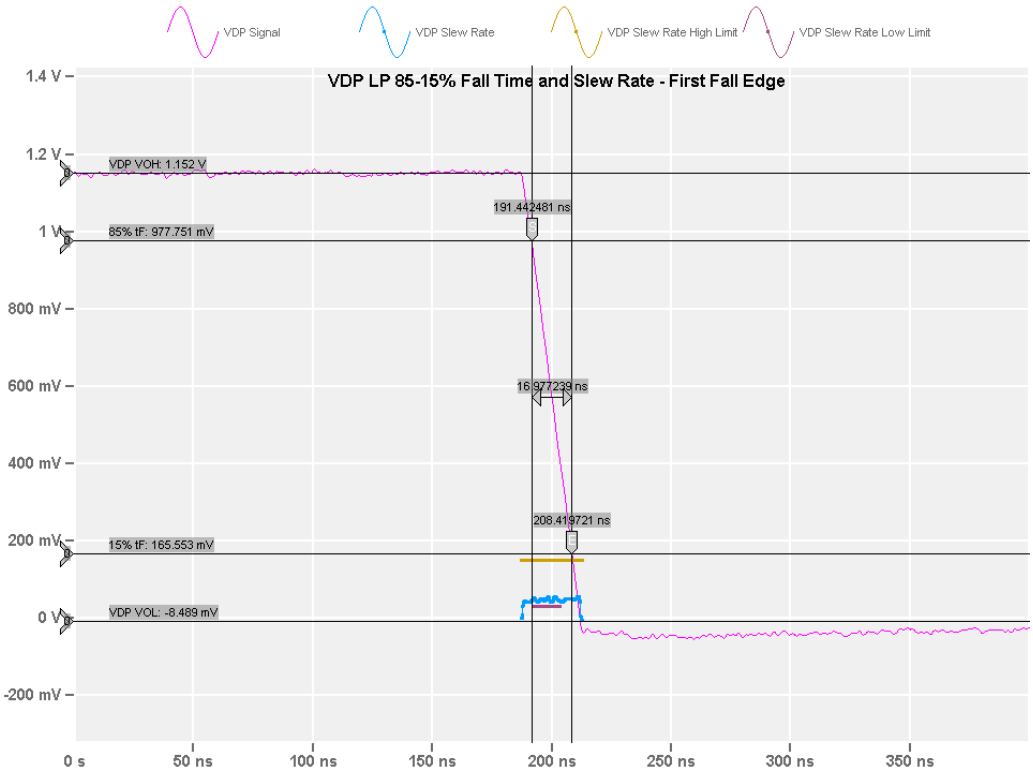


Figure 4-15: Typical result of a clock lane LP-TX 85%-15% fall time and slew rate measurement for V_DP

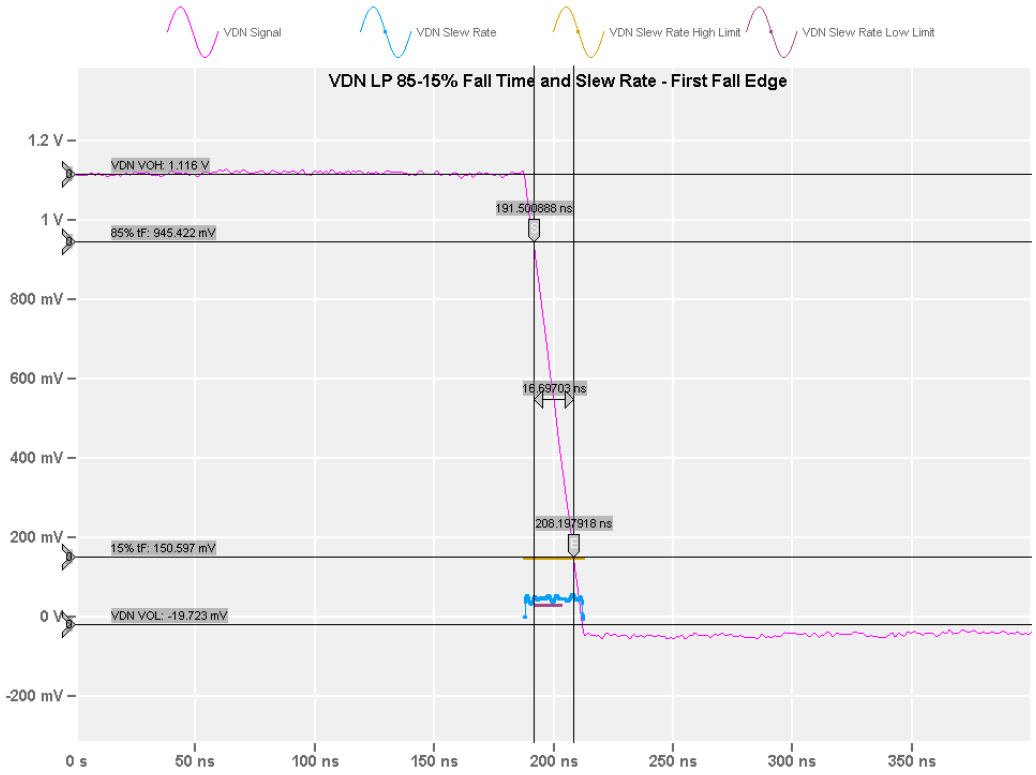


Figure 4-16: Typical result of a clock lane LP-TX 85%-15% fall time and slew rate measurement for V_DN

4.4.3.5 Test 1.2.5 – Clock Lane LP-TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$)

The purpose of this test case is to verify the slew rate ($\delta V/\delta t_{SR}$) of the DUT's clock lane LP transmitter is within the conformance limits, for specific capacitive loading conditions. Various conformance ranges apply, as detailed below.

The slew rate is computed and measured independently for each edge of the V_{DP} and V_{DN} signals using a 50 mV vertical window. The slew rate curve is computed for a single edge using the sliding window technique.

For falling edges:

1. The final averaged maximum $\delta V/\delta t_{SR}$ result is computed over the entire vertical edge region. The conformance range is less than 150 V/µs.
2. The final averaged minimum $\delta V/\delta t_{SR}$ result is computed over the 400-930 mV region. The conformance range is greater than 30 V/µs.

For rising edges:

1. The final averaged maximum $\delta V/\delta t_{SR}$ result is computed over the entire vertical edge region. The conformance range is less than 150 V/µs.

2. The final averaged minimum $\delta V/\delta t_{SR}$ result is computed over the 400-700 mV region. The conformance range is greater than 30 V/µs.
3. The final averaged minimum $\delta V/\delta t_{SR}$ margin result is computed over the 700-930 mV region. The minimum limit is defined by the equation 30-0.075·($V_{O\text{-}INST}$ - 700). The conformance range is greater than 0 V/µs.

Both a ULPS Entry sequence and an Exit sequence are specified for this test. The measurement is performed separately on both V_{DP} and V_{DN} clock lane waveforms.

Examples are shown in Figure 4-13, Figure 4-14, Figure 4-15 and Figure 4-16.

4.5 Data lane HS-TX signaling requirements (Group 3)

The purpose of Group 3 test cases is to verify the various transmission requirements specific to data lane high speed (HS) burst signaling.

Group 3 consists of 16 test cases, described in Chapter 4.5.3, "Measurements", on page 51. They include LP Exit and Entry sequences occurring before and after the HS burst sequence.

The software is intended to facilitate the execution of a set of several HS-TX measurements on a set of captured HS burst waveforms. This version of the R&S ScopeSuite MIPI D-PHY compliance test software only processes data burst waveforms (also known as non-continuous data waveforms). It does not support partial data burst (where HS Entry and HS Exit are captured separately) or continuous data. However, the software supports clock burst, partial clock burst, and continuous clock.

These test cases are applicable to master devices, only.

4.5.1 Test setup

Table 4-4: Equipment for Group 3 Data Lane HS-TX Signaling Requirements test

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 / RTP with 4 channels and at least 4 GHz bandwidth	1
Probes	Differential probes: at least 4 GHz bandwidth, or Single-ended probes: at least 4 GHz bandwidth	2/3/4 (*)
Test fixture	UNH-IOL MIPI D-PHY Reference Termination Board (RTB)[1]	1
DUT	Any MIPI D-PHY CSI-2 or DSI device	1

Item	Description, model	Quantity
* Regarding the selection of probes, there are three different configuration scenarios: • *No clock*: If in the HS configuration dialog, "Z_{ID}" has been selected to be "80 ohms" or "125 ohms", **2** probes are required (either single-ended, or differential in single-ended mode). • *Differential clock*: If in the HS configuration dialog, the "Probe Config" is set to "< 4", **3** probes are required: 1 differential probe and 2 additional probes (the latter 2 either single-ended, or differential in single-ended mode). • *Single-ended clock*: If in the HS configuration dialog, the "Probe Config" is set to "4", **4** probes are required (either single-ended, or differential in single-ended mode).		
[1] We recommend to use a MIPI D-PHY Reference Termination Board (RTB) test fixture from the University of New Hampshire InterOperability Laboratory (UNH-IOL). Refer to https://www.iol.unh.edu/services/testing/mipi/fixtures.php for details.		

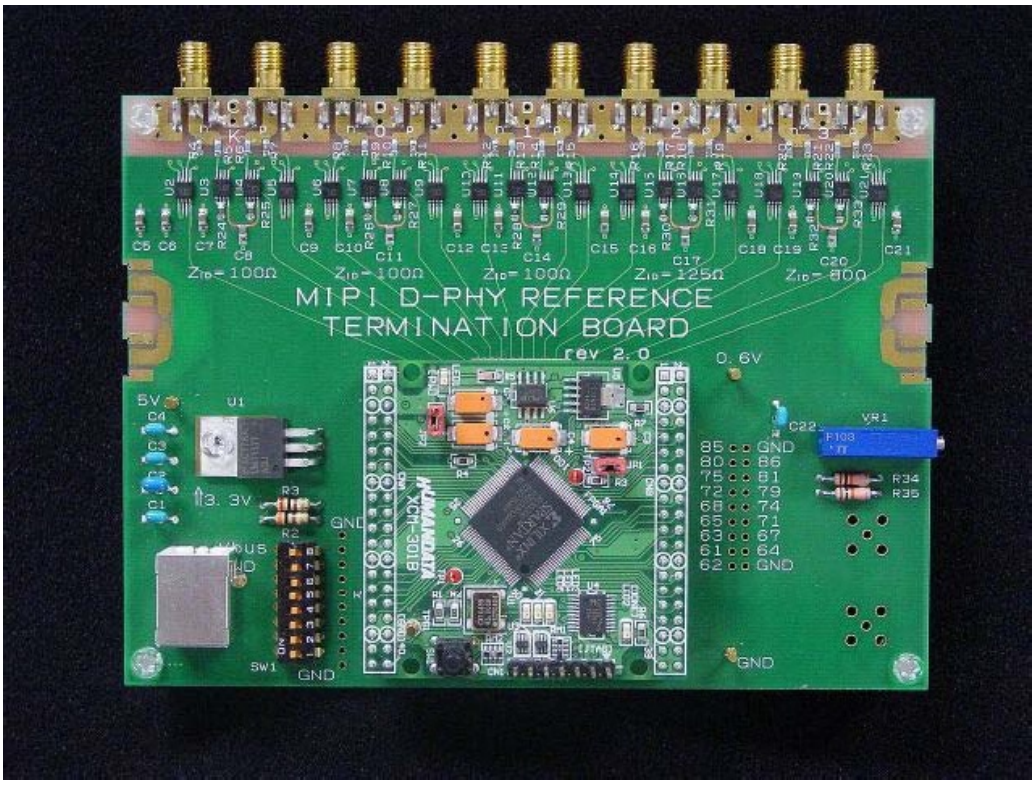


Figure 4-17: MIPI D-PHY Reference Termination Board test fixture from UNH-IOL

Waveform requirements

Group 3 test cases require the DUT to transmit HS data burst waveforms, as shown in Figure 4-18, consisting of:

- (a) LP-11 (HS Entry)
- (b) LP-01
- ©) LP-00
- (d) HS-ZERO
- (e) HS-SYNC
- (f) HS-PAYLOAD

- (g) HS-TRAIL
- (h) LP-11 (HS Exit)

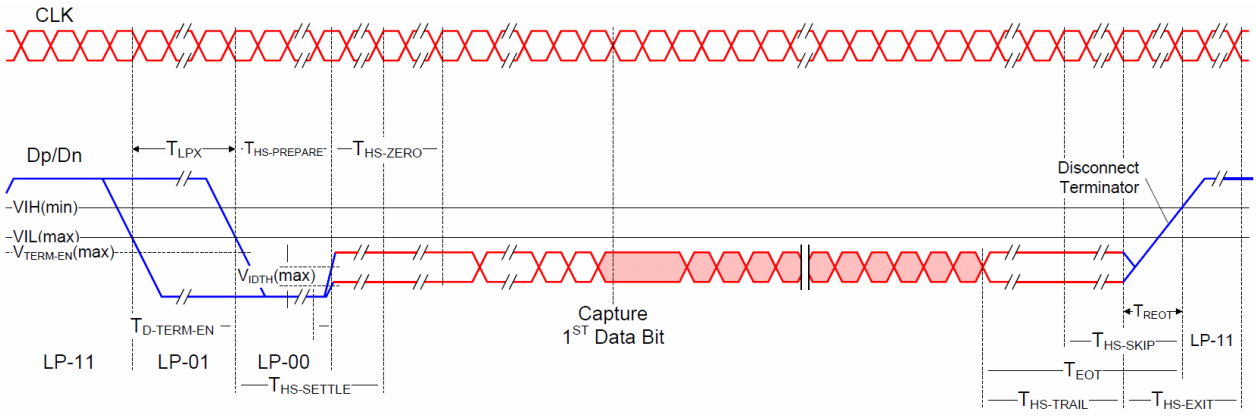


Figure 4-18: A typical MIPI D-PHY HS data burst waveform (courtesy of MIPI Alliance Specification for D-PHY version 1.1)

The software requires at least one set of complete data burst waveforms for correct processing, to perform the test successfully.

Payload requirements

More than half of the Group 3 test cases are analyzing the data in the HS transmission. Therefore, it is important for the HS-PAYLOAD to contain at least:

- (a) 5000 occurrences of '1'
- (b) 5000 occurrences of '0'
- ©) 128 occurrences of '100000'
- (d) 128 occurrences of '0111111'
- (e) 128 occurrences of '111000'
- (f) 128 occurrences of '000111'

If the HS-PAYLOAD does not meet these minimum requirements, the software does still process the waveforms, but the measurements may not be accurate, and the test results may be invalid.

It is recommended to use reference HS test patterns or images. UNH-IOL has created a "PATGUI" utility, which can be used to generate test patterns and images for various resolutions and formats. For members of the MIPI Alliance, this utility can be obtained free of charge from the MIPI Testing Resources page on the MIPI Alliance website (https://members.mipi.org/mipi-testing/workspace/Test_Vehicle_Board_Resources).

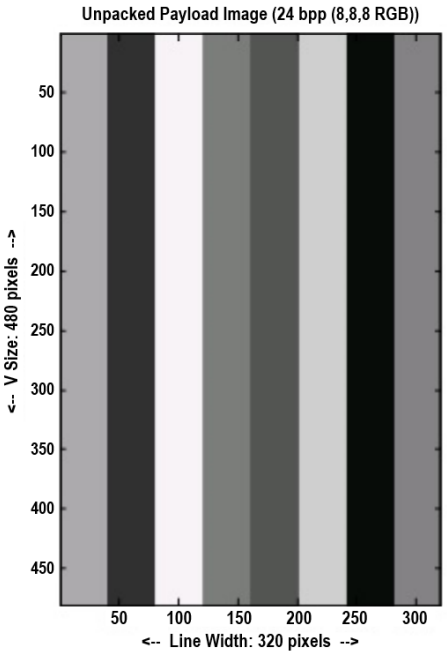


Figure 4-19: Example reference HS test pattern, RGB888 format (courtesy: MIPI Alliance, D-PHY specs)

Settings in the "HS Configuration" dialog box

See also: Chapter 4.2, "Test configuration for D-PHY", on page 20.

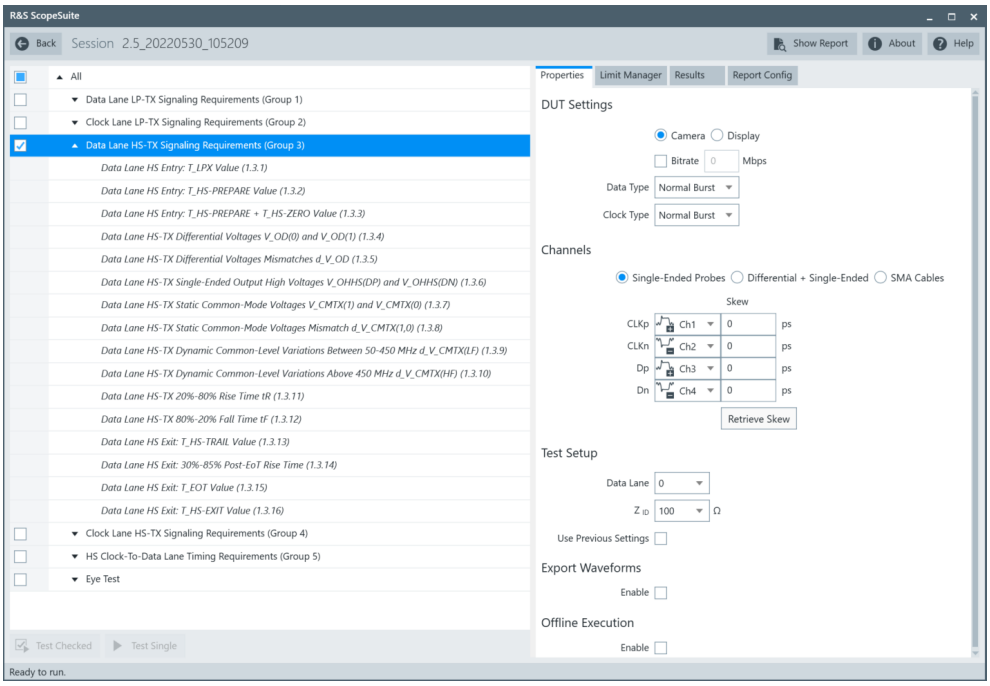
- **DUT Settings**
  Select if the DUT is a "Camera" or a "Display".
  You can also set the "Data type" and "Clock type" according to your device.
- **Channels**
  This setting depends on the probes that are used to capture the clock signals .
  Select the channels for the measurement and set or retrieve the skew.
- **Data Lane Under Test**
  If the DUT implements multiple data lanes, select which pair of data lanes is to be tested.
- **Z_{ID}**
  Each lane of the RTB board has a specific termination value. According to your test requirements, connect your DUTs to the lane with the corresponding Z_{ID} value.
  For more information about the RTB board, refer to its datasheet.
  - If Z_{ID} is 100 ohms, the pair of data lanes under test (dat_p and dat_n) and the pair of clock lanes (clk_p and clk_n) have to be terminated with the 100 ohms loads on the RTB. This can be done on the lanes Data0 or Data1 of the RTB board.

The data signal (two probes: single-ended, or differential in single-ended mode) and the clock signal (either two single-ended or one differential probe) are captured by the oscilloscope and processed by the software.

– If Z_{ID} is 80 or 125 ohms, the pair of data lanes under test have to be terminated with the 80 or 125 ohms loads on the RTB, whereas the pair of clock lanes have to be terminated with the 100 ohms loads on the RTB.
Data2 lane of the RTB board has a Z_{ID} of 125 ohms and Data3 lane has a Z_{ID} of 80 ohms.
Only the data signal (two probes: single-ended, or differential in single-ended mode) is captured by the oscilloscope. The clock signal is recovered from the data signal by the software.

4.5.2 Performing Group 3 test cases

1. Start running the tests as described in Chapter 4.1, "Starting D-PHY compliance tests", on page 20.
2. Select "Data Lane HS-TX Signaling Requirements (Group 3)".



3. Click "Test Single" to run only the selected test case.
Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
This group of tests uses the MIPI D-PHY Reference Termination Board (RTB) test fixture from the UNH-IOL.
The data and clock signals can be tapped either on the DUT or RTB, or even on the SMA cables between the DUT and the RTB.

The connections may differ slightly depending on the clock format and the terminations which are applied to the DUT.
When you have finished all steps, the compliance test runs automatically.

Further steps:

- Chapter 3.3, "Getting test results", on page 16

4.5.3 Measurements

4.5.3.1 Test 1.3.1 – Data Lane HS Entry: Data Lane T_{LPX} Value

The purpose of this test case is to verify that the duration of the last LP-01 state immediately before HS transmission is at least 50 ns.

The software measures the duration of the last LP-01 state that occurs immediately before an HS transmission. This duration is labeled T_{LPX}.

The duration is measured

- Starting at the time when the V_{DP} falling edge crosses below the maximum logic 0 input voltage, $V_{IL,MAX}$ (550 mV)
- Ending at the time when the V_{DN} falling edge crosses below the same logic 0 input voltage $V_{IL,MAX}$

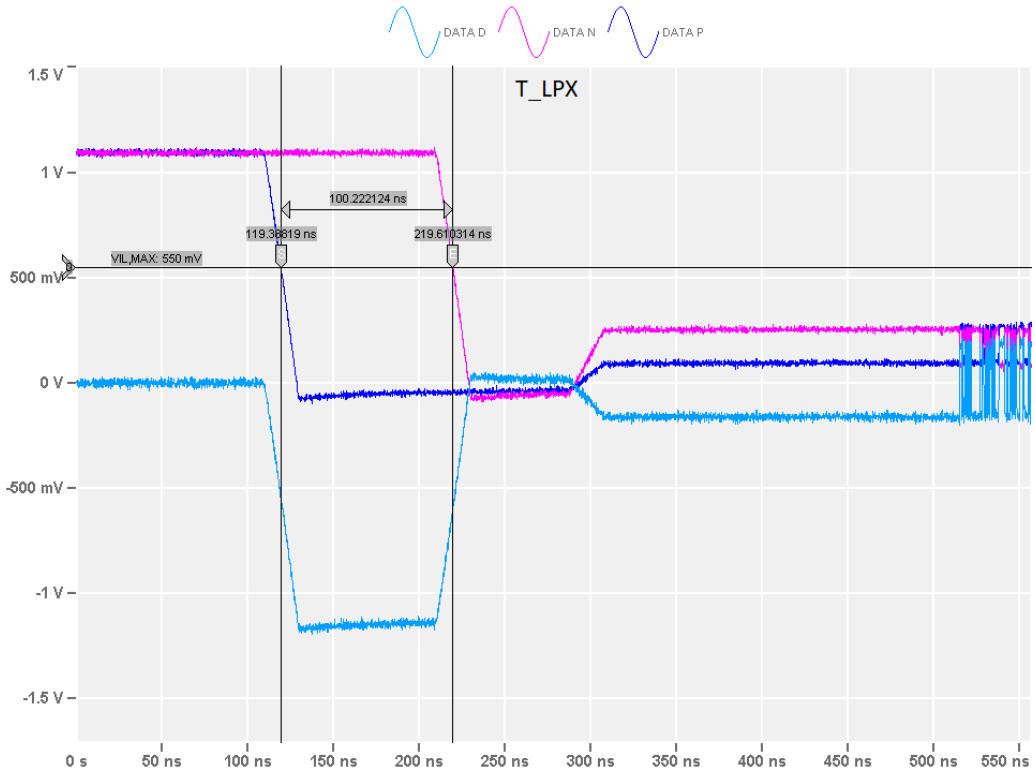


Figure 4-20: Typical result of a data lane T_LPX measurement. This figure shows a failure case: T_LPX < 50 ns

Datp = Waveform of Data+ (V_{DP})
Datn = Waveform of Data- (V_{DN})
Datd = Differential waveform, V_{DP} - V_{DN}
T_LPX = Duration of last LP-01 state immediately before HS transmission

This test case is tested for Z_{ID} = 100 ohms, only, and for all data lanes.

4.5.3.2 Test 1.3.2 – Data Lane HS Entry: Data Lane $T_{HS-PREPARE}$ Value

The purpose of this test case is to verify that the duration of the last LP-00 state immediately before HS transmission is between (40 ns + 4·UI) and (85 ns + 6·UI), with UI = Unit Interval, which is the symbol duration time.

The software measures the duration of the last LP-00 state that occurs immediately before an HS transmission. This duration is labeled $T_{HS-PREPARE}$.

The duration is measured

- Starting at the time when the V_{DN} falling edge crosses below the maximum logic 0 input voltage, $V_{IL,MAX}$ (550 mV)
- Ending at the time when the differential waveform crosses below the minimum differential input low threshold, V_{IDTL} (-70 mV for D-PHY 1.1; -40 mV for D-PHY≥ 1.2)

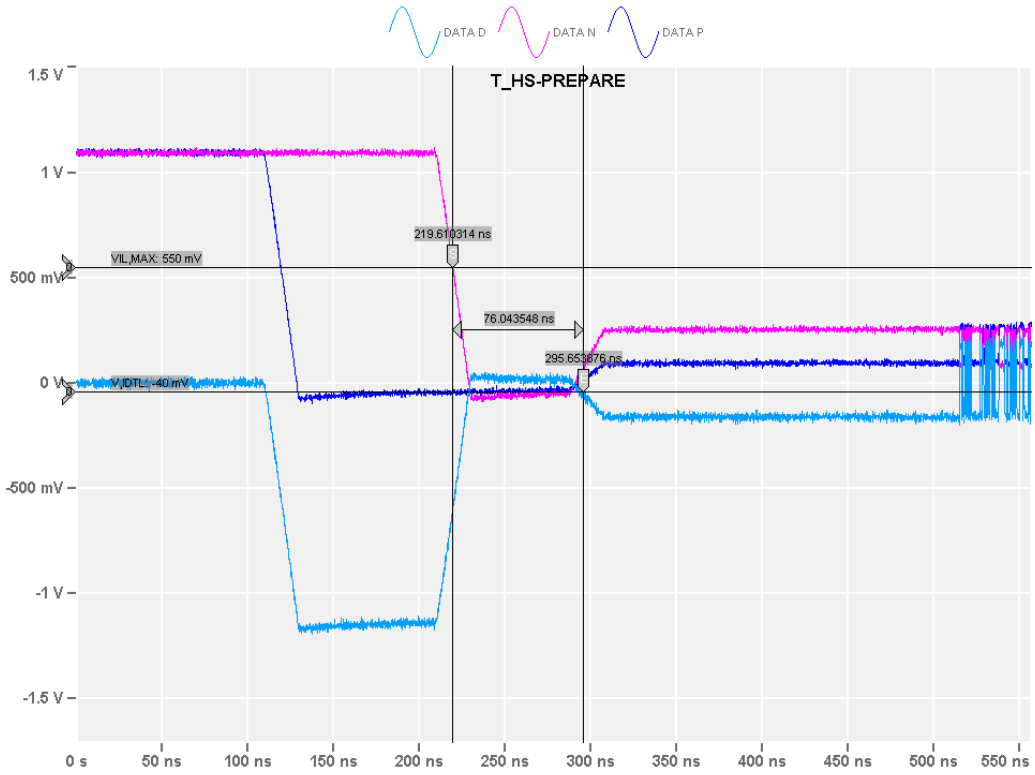


Figure 4-21: Typical result of a data lane T_HS-PREPARE measurement

Datp = Waveform of Data+ (V_{DP})
Datn = Waveform of Data- (V_{DN})
Datd = Differential waveform, V_{DP} - V_{DN}
T_HS-PREPARE = Duration of last LP-00 state immediately before HS transmission

This test case is tested for Z_{ID} = 100 ohms, only, and for all data lanes.

4.5.3.3 Test 1.3.3 – Data Lane HS Entry: Data Lane $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ Value

The purpose of this test case is to verify that the combined value of $T_{HS-PREPARE}$ and the duration of the HS-ZERO state that occurs immediately before an HS transmission, is at least (145 ns + 10·UI).

The software measures the duration of the HS-ZERO state that occurs immediately before an HS transmission. This duration is labeled $T_{HS-ZERO}$.

- Starting at the time when the differential waveform crosses below the minimum differential input low threshold, V_{IDTL} (-70 mV for D-PHY 1.1; -40 mV for D-PHY≥ 1.2).
- Ending at the start of HS-SYNC state
  However, the HS-SYNC sequence begins with a ‘0001’ and so there will be no visible delineation between the end of the HS-ZERO state and the start of the HS-SYNC state. Therefore, the start of the HS-SYNC state is defined at 3 bit-times before the differential waveform crosses the maximum differential input high threshold, V_{IDTH} (70 mV).

The software then computes the combined value of $T_{HS\text{-}PREPARE}$ (see Chapter 4.5.3.2, "Test 1.3.2 – Data Lane HS Entry: Data Lane $T_{HS\text{-}PREPARE}$ Value", on page 52) and $T_{HS\text{-}ZERO}$.

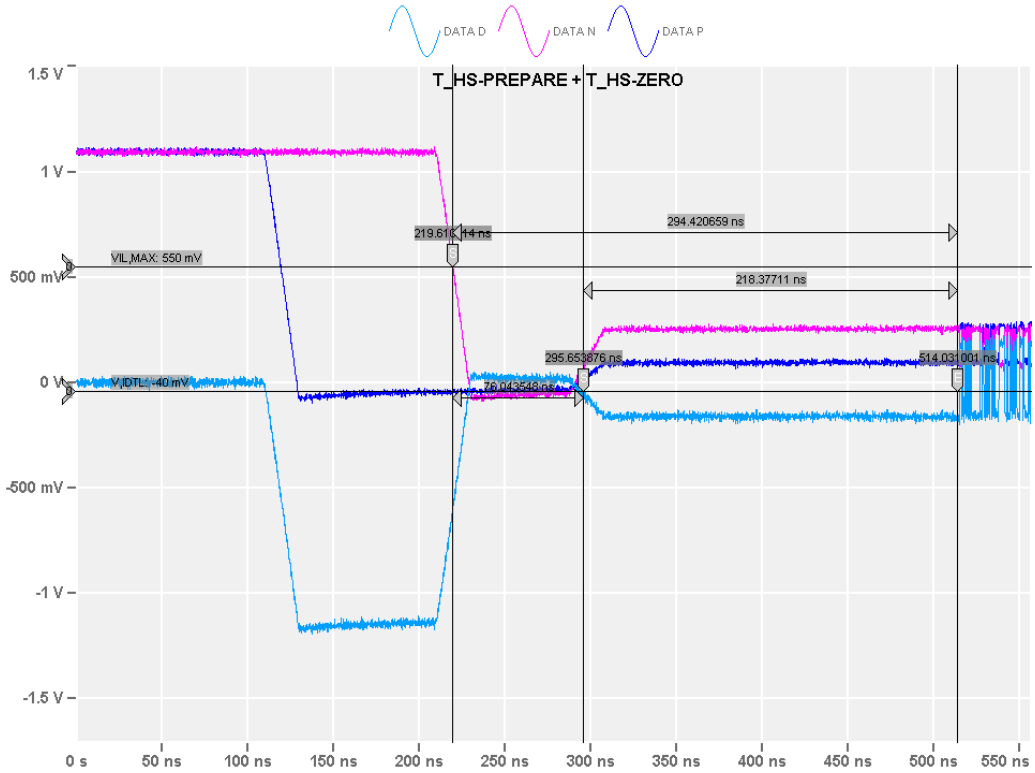


Figure 4-22: Typical result of a data lane T_HS-PREPARE + T_HS-ZERO measurement

Datp = Waveform of Data+ (V_{DP})
Datn = Waveform of Data- (V_{DN})
Datd = Differential waveform, V_{DP} - V_{DN}
T_HS-PREPARE = Duration of last LP-00 state immediately before HS transmission
T_HS-ZERO = Duration of HS-ZERO state immediately before HS transmission

This test case is tested for Z_{ID} = 100 ohms, only, and for all data lanes.

4.5.3.4 Test 1.3.4 – Data Lane HS-TX Differential Voltages $V_{OD(0)}$ and $V_{OD(1)}$

The purpose of this test case is to verify, that:

- The HS transmit differential-0 voltage ($V_{OD(0)}$) is between -140 mV and -270 mV, and
- The HS transmit differential-1 voltage ($V_{OD(1)}$) is between 140 mV and 270 mV.

$V_{OD(0)}$: To measure the HS transmit differential-0 voltage, the software searches for reference waveforms with the data pattern ‘100000’ in the HS transmission differential data signal. Three cases are to be distinguished:

- If there is no occurrence of ‘100000’, the software marks $V_{OD(0)}$ as "indeterminable" and proceeds with the next measurement ($V_{OD(1)}$).

- If there are fewer than 128 occurrences of ‘100000’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to use a different test pattern, and then redo the test.
- If there are 128 or more occurrences of ‘100000’, the software processes the last 128 reference waveforms.

The reason for this procedure is this: In some cases, transient effects introduced by some high impedance probes can introduce a small error in the HS common-mode level at the beginning of the transmission. This error can be significant enough to affect the test result. Therefore, an average waveform is constructed by horizontally aligning 128 (or less) reference waveforms to a common anchor point, which is the zero crossing time of the first transition.

The value of $V_{OD(0)}$ is then determined from that average waveform: it is the mean of all voltage amplitude samples that fall between the centers of the fourth and fifth ‘0’ bit in the ‘100000’ data pattern.

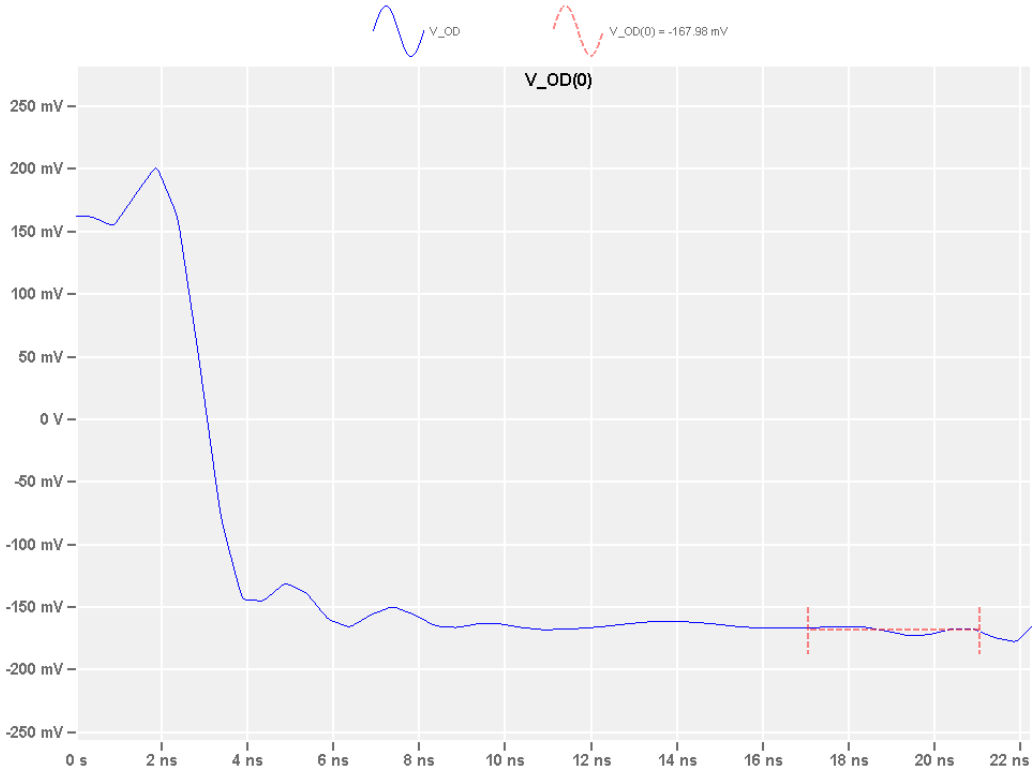


Figure 4-23: Typical result of an HS transmit differential-0 voltage measurement

$V_{OD(1)}$: The software measures the HS transmit differential-1 voltage in a similar way as $V_{OD(0)}$. Two exceptions are:

- It searches for reference waveforms with the data pattern ‘0111111’ (instead of ‘100000’).
- The value of $V_{OD(1)}$ is then determined from that average waveform: it is the mean of all voltage amplitude samples that fall between the centers of the fourth and fifth ‘1’ bit in the ‘0111111’ data pattern (instead of 4^{th}-5^{th} ‘0’ bit in the ‘100000’ data pattern).

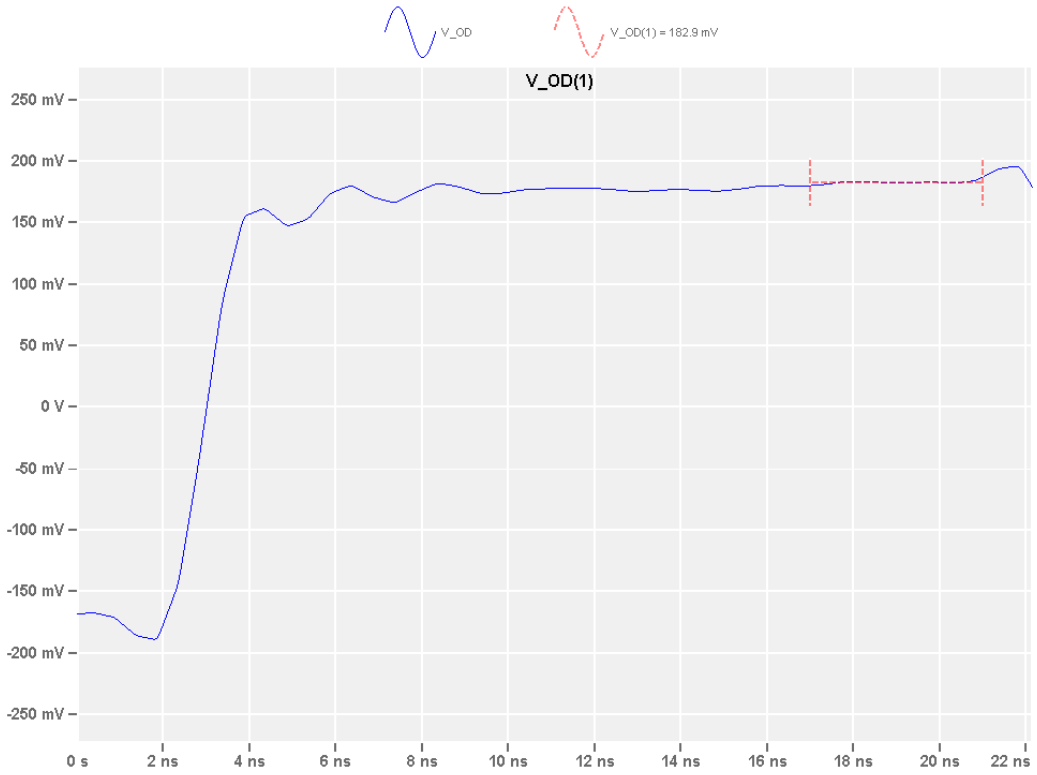


Figure 4-24: Typical result of an HS transmit differential-1 voltage measurement

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all data lanes.

4.5.3.5 Test 1.3.5 – Data Lane HS-TX Differential Voltage Mismatch ΔV_{OD}

The purpose of this test case is to verify that the HS transmit differential voltage mismatch (ΔV_{OD}) is between +14 mV and -14 mV.

Using the values obtained in Chapter 4.5.3.4, "Test 1.3.4 – Data Lane HS-TX Differential Voltages $V_{OD(0)}$ and $V_{OD(1)}$", on page 54, the software computes the HS transmit differential voltage mismatch according to this formula:

$\Delta V_{OD} = |V_{OD(1)}| - |V_{OD(0)}|$

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all data lanes.

4.5.3.6 Test 1.3.6 – Data Lane HS-TX Single-Ended Output Voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$

The purpose of this test case is to verify that the single-ended HS output high voltage is not more than 360 mV.

$V_{OHHS(DP)}$: To measure the D_P HS output high voltage, the software searches for reference waveforms with the data pattern ‘011111’ in the HS transmission differential data signal.

Although – in this context – it is referring to the single-ended signal, ‘011111’ on the differential signal means the same pattern on the D_P single-ended signal.

Three cases are to be distinguished:

- If there is no occurrence of ‘011111’, the software marks $V_{OHHS(DP)}$ as "indeterminable" and proceeds with the next measurement ($V_{OHHS(DN)}$).
- If there are less than 128 occurrences of ‘011111’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to use a different test pattern, and then redo the test.
- If there are 128 or more occurrences of ‘011111’, the software processes the last 128 reference waveforms.

An average waveform is then constructed by horizontally aligning 128 (or less) reference waveforms to a common anchor point, which is the zero crossing time of the first transition.

The value of $V_{OHHS(DP)}$ is then determined from that average waveform: it is the mean of all voltage amplitude samples that fall between the centers of the fourth and fifth ‘1’ bit in the ‘011111’ data pattern.

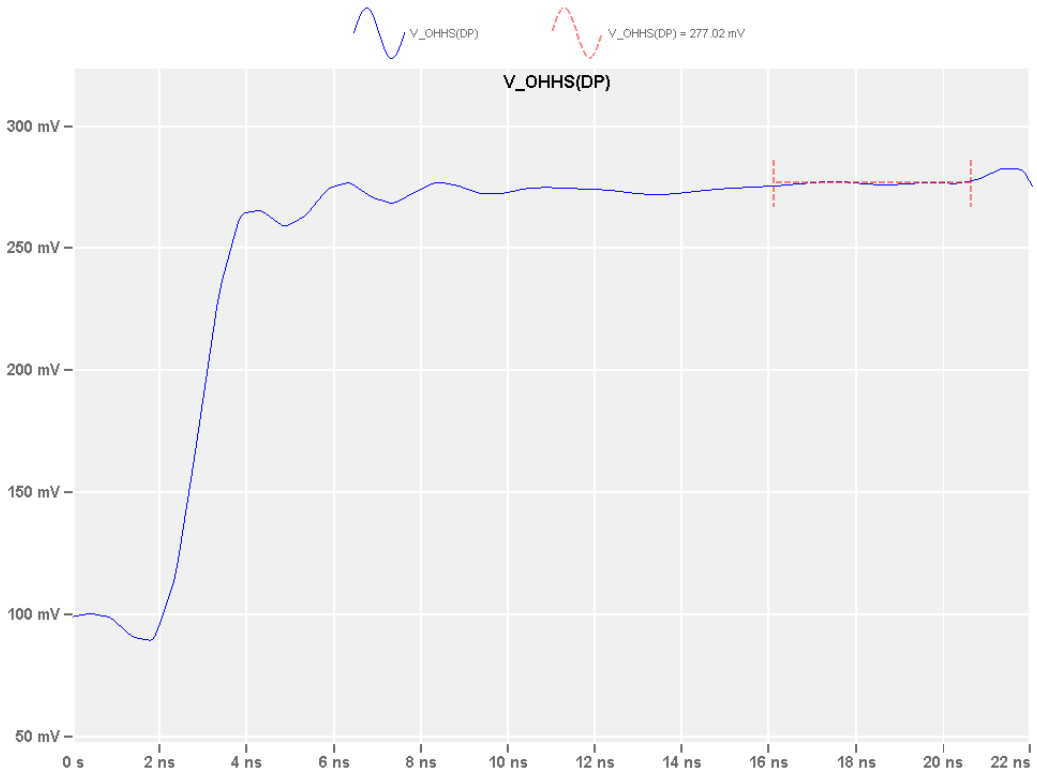


Figure 4-25: Typical result of a D+ HS single-ended output high voltage measurement

V_OHHS = High speed output high voltage
DP = Data positive (D+)

$V_{OHHS(DN)}$: The software measures the D_N HS output high voltage in a similar way as $V_{OHHS(DP)}$. One exception is:

- It searches for reference waveforms with the data pattern '100000' (instead of '011111'), because '100000' on the differential signal corresponds with '011111' on the D_N single-ended signal.

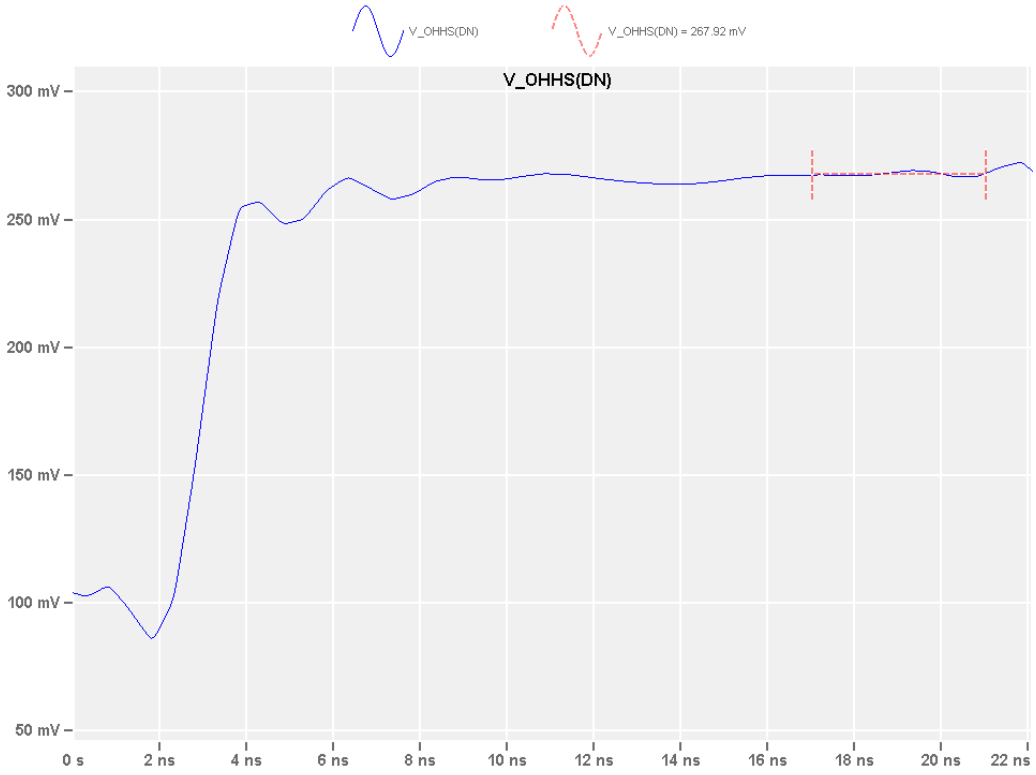


Figure 4-26: Typical result of a D- HS single-ended output high voltage measurement

V_OHHS = High speed output high voltage
DN = Data negative (D-)

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all data lanes.

4.5.3.7 Test 1.3.7 – Data Lane HS-TX Static Common-Mode Voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$

The purpose of this test case is to verify that the HS transmit static common-mode voltages ($V_{CMTX(1)}$ and $V_{CMTX(0)}$) are between 150 mV and 250 mV.

The HS transmit static common-mode voltage is defined in the specification as the arithmetic mean of the value of the voltages at D_P and D_N:

$V_{CMTX} = (V_{DP} + V_{DN})/2$

$V_{CMTX(1)}$: The software measures the HS transmit differential-1 static common-mode voltage, by searching for all occurrences of bit '1' in the HS transmission differential data signal. Two cases are to be distinguished:

- If there are less than 5000 occurrences of '1', the software does still process the bits. However, the test results may be invalid; it is recommended to use a different test pattern, and then redo the test.
- If there are 5000 or more occurrences of '1', the software processes all of them.

For every occurrence of '1' that the software can find in the differential signal, it computes the HS transmitter static common-mode voltage according to the formula mentioned above. The voltages (V_{DP} and V_{DN}) of all the '1' bits are taken at the corresponding clock zero crossings. The value of $V_{CMTX(1)}$ is measured as the average of these common-mode voltages.

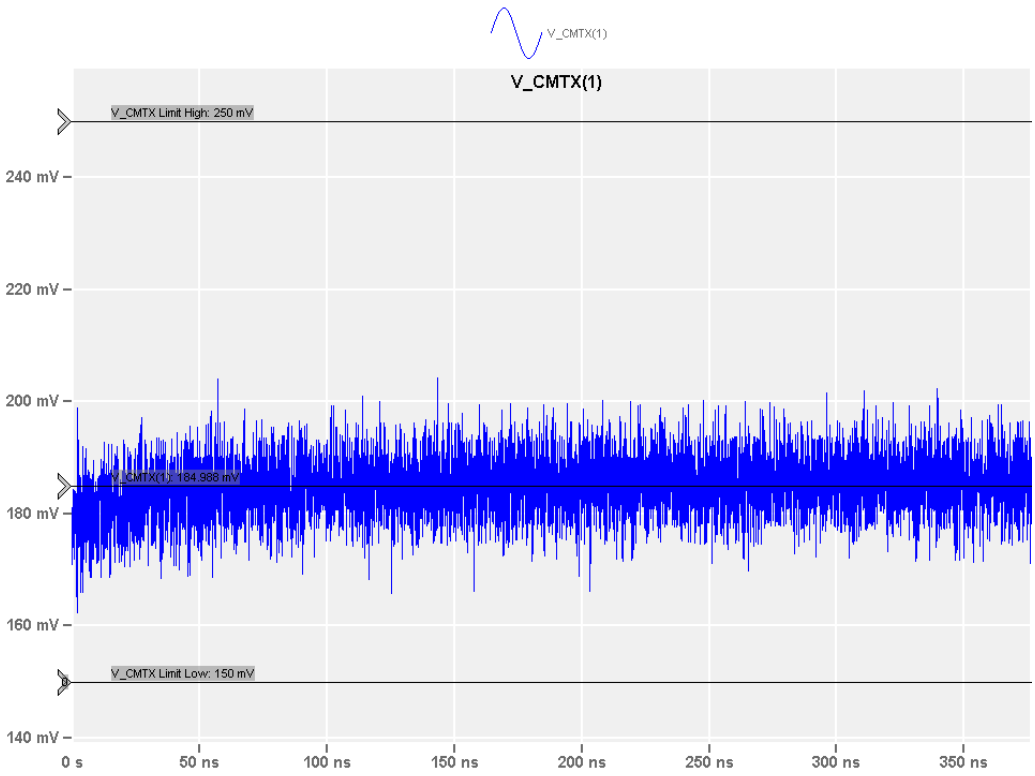


Figure 4-27: Typical result of a data lane HS transmit differential-1 static common-mode voltage measurement, V_CMTX(1)

$V_{CMTX(0)}$: The software measures the HS transmit differential-0 static common-mode voltage in a similar way as $V_{CMTX(1)}$. One exception is:

- It searches for all occurrences of bit '0' instead of bit '1'.

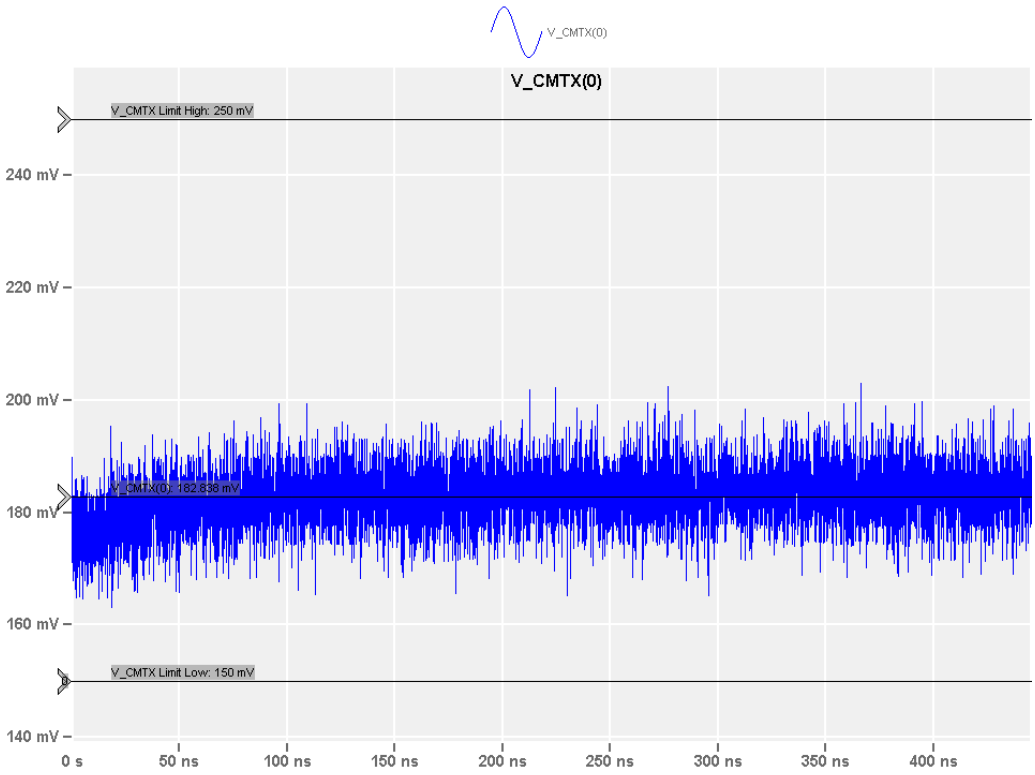


Figure 4-28: Typical result of a data lane HS transmit differential-0 static common-mode voltage measurement, V_CMTX(0)

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all data lanes.

4.5.3.8 Test 1.3.8 – Data Lane HS-TX Static Common-Mode Voltage Mismatch $\Delta V_{CMTX(1,0)}$

The purpose of this test is to verify that the HS transmit static common-mode voltage mismatch is between +5 mV and -5 mV.

Using the values obtained in Chapter 4.5.3.7, "Test 1.3.7 – Data Lane HS-TX Static Common-Mode Voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$", on page 58, the software computes the HS transmit static common-mode voltage mismatch $\Delta V_{CMTX(1,0)}$ according to this formula:

$$\Delta V_{CMTX(1,0)} = (\Delta V_{CMTX(1)} - \Delta V_{CMTX(0)})/2$$

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all data lanes.

4.5.3.9 Test 1.3.9 – Data Lane HS-TX Dynamic Common-Level Variations Between 50-450 MHz $\Delta V_{CMTX(LF)}$

The purpose of this test case is to verify that the common-level variation between 50-450 MHz is not more than 25 mV_{PEAK}.

The common-level variation between 50-450 MHz $\Delta V_{CMTX(LF)}$ is measured as follows:

The software compiles a list of HS transmit static common-voltage voltages for every zero crossing of the clock signal, using the formula stated in Chapter 4.5.3.7, "Test 1.3.7 – Data Lane HS-TX Static Common-Mode Voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$", on page 58. This list will be used as the input to an 8th order Butterworth bandpass filter with cutoff frequencies of 50 MHz and 450 MHz, respectively. The value of $\Delta V_{CMTX(LF)}$ is measured as the absolute peak voltage at the output of the bandpass filter.

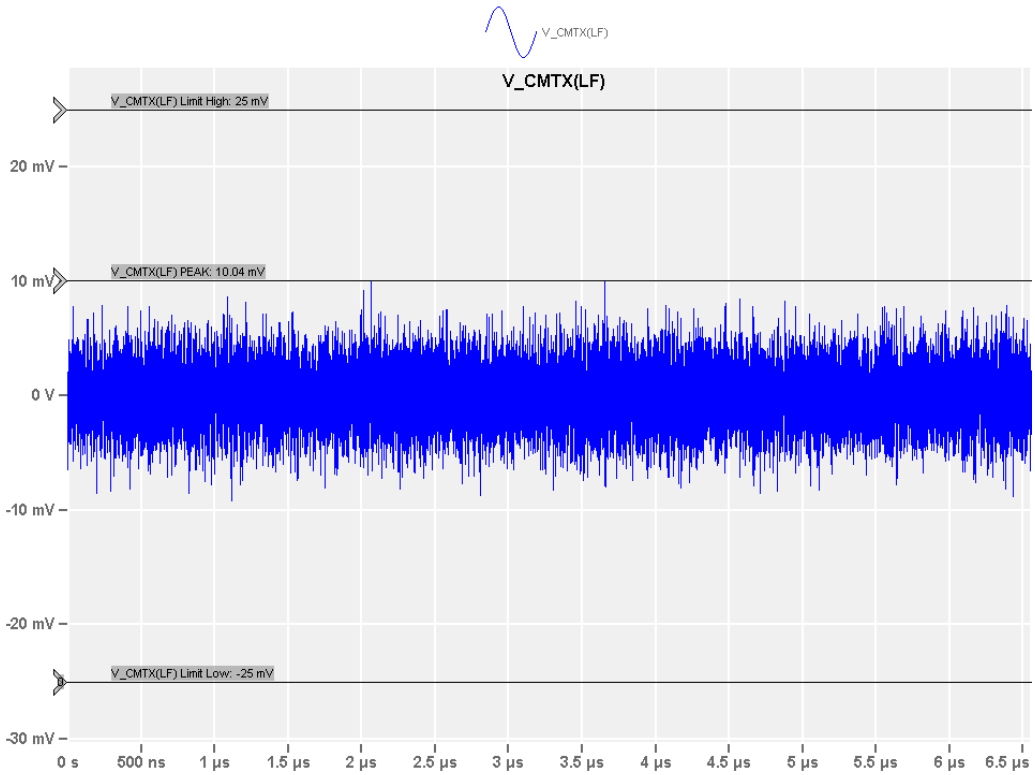


Figure 4-29: Typical result of a data lane HS transmit dynamic common-level variations measurement at low frequencies, V_CMTX(LF)

This test case is tested for Z_{ID} = 100 ohms, only, and for all data lanes.

4.5.3.10 Test 1.3.10 – Data Lane HS-TX Dynamic Common-Level Variations Above 450 MHz $\Delta V_{CMTX(HF)}$

The purpose of this test case is to verify that the common-level variation above 450 MHz is not more than 15 mV_{RMS}.

The common-level variation above 450 MHz $\Delta V_{CMTX(HF)}$ is measured as follows:

The software uses the same list of HS transmit static common-voltage voltages from Chapter 4.5.3.9, "Test 1.3.9 – Data Lane HS-TX Dynamic Common-Level Variations Between 50-450 MHz $\Delta V_{CMTX(LF)}$", on page 60 as the input to an 8th order Butterworth

highpass filter with a cutoff frequency of 450 MHz. The value of $\Delta V_{CMTX(HF)}$ is measured as the RMS voltage at the output of the highpass filter.

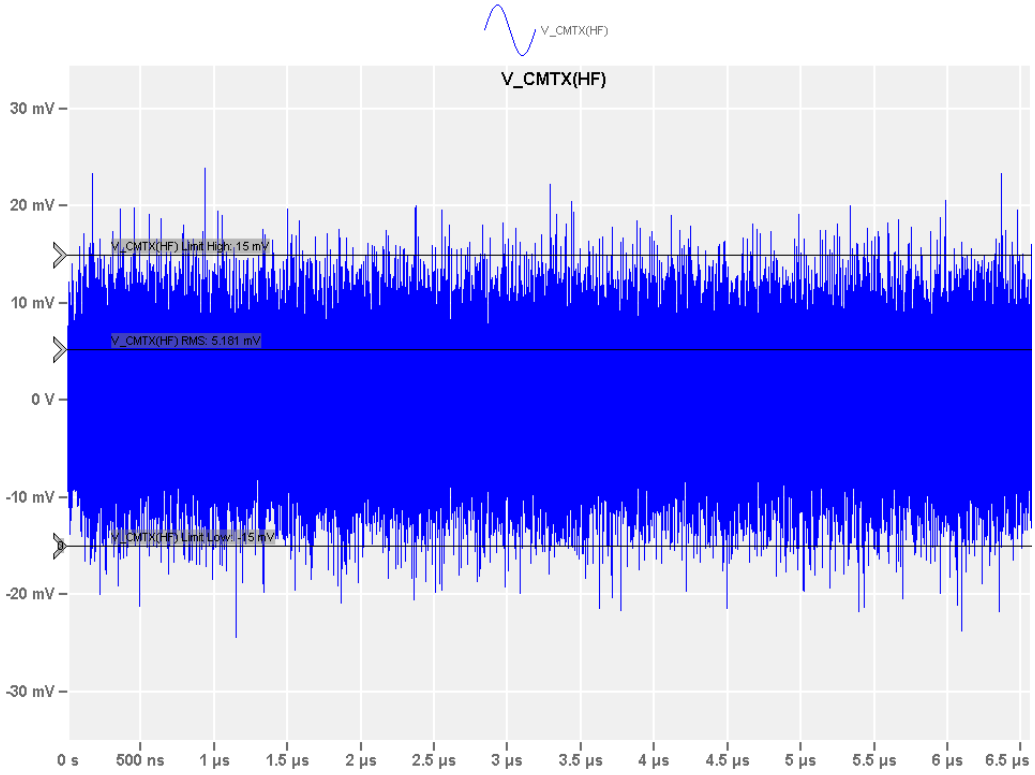


Figure 4-30: Typical result of a data lane HS transmit dynamic common-level variations measurement at high frequencies, V_CMTX(HF)

This test case is tested for Z_{ID} = 100 ohms, only, and for all data lanes.

4.5.3.11 Test 1.3.11 – Data Lane HS-TX 20%-80% Rise Time t_R

The purpose of this test case is to verify that the 20%-80% rise time is:

- Between 150 ps and 0.3·UI when operating at HS bit rates up to 1 Gbps.
- Between 100 ps and 0.35·UI when operating at HS bit rates greater than 1 Gbps.

To measure the 20%-80% rise time t_R, the software searches for reference waveforms with the data pattern ‘000111’ in the HS transmission differential data signal. Three cases are to be distinguished:

- If there is no occurrence of ‘000111’, the software marks t_R as "indeterminable" and proceeds with the next test case.
- If there are less than 128 occurrences of ‘000111’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to use a different test pattern, and then redo the test.
- If there are 128 or more occurrences of ‘000111’, the software processes the last 128 reference waveforms.

An average waveform is then constructed by horizontally aligning 128 (or less) reference waveforms to a common anchor point, which is the zero crossing time of the first transition.

Once the average waveform is obtained, the value of t_R is measured as the time taken for the waveform to rise from $[V_{OD(0)} + 0.2 \cdot \{V_{OD(1)} - V_{OD(0)}\}]$ to $[V_{OD(0)} + 0.8 \cdot \{V_{OD(1)} - V_{OD(0)}\}]$.

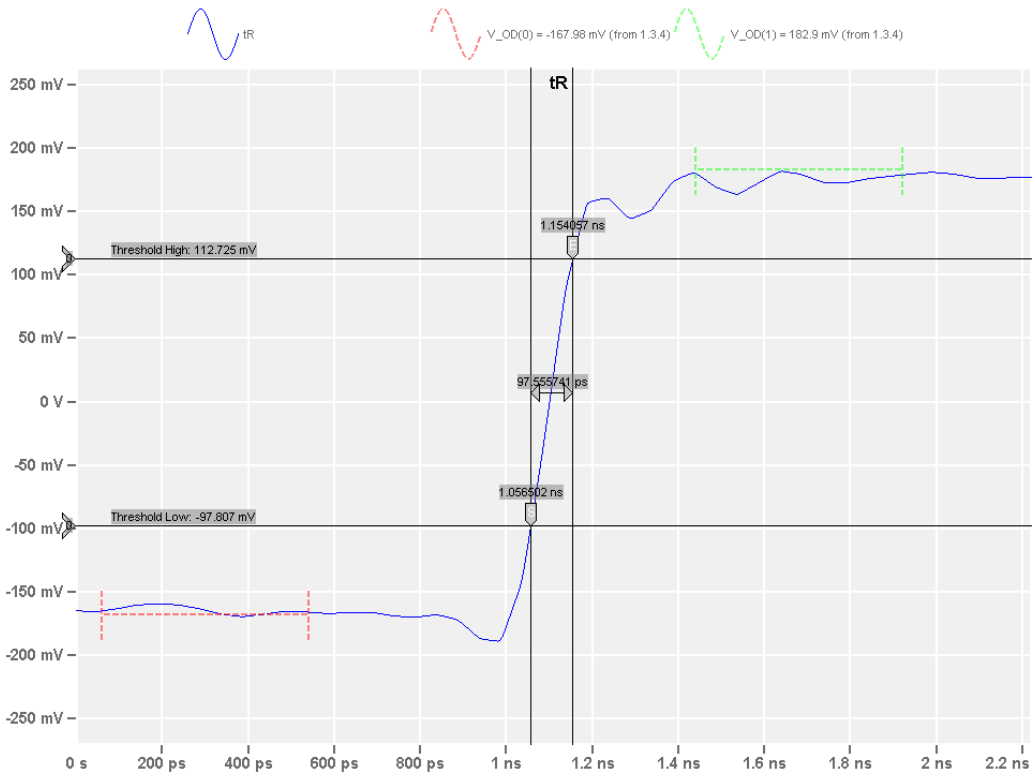


Figure 4-31: Typical result of a data lane HS transmit 20%-80% rise time measurement

V_{OD} = High speed transmission differential data signal
$V_{OD(0)}$ = HS transmit differential-0 voltage
$V_{OD(1)}$ = HS transmit differential-1 voltage
t_R = Rise time

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all data lanes.

4.5.3.12 Test 1.3.12 – Data Lane HS-TX 80%-20% Fall Time t_F

The purpose of this test case is to verify that the 80%-20% fall time is:

- Between 150 ps and 0.3·UI when operating at HS bit rates up to 1 Gbps.
- Between 100 ps and 0.35·UI when operating at HS bit rates greater than 1 Gbps.

To measure the 80%-20% fall time t_F, the software searches for reference waveforms with the data pattern ‘111000’ in the HS transmission differential data signal. Three cases are to be distinguished:

- If there is no occurrence of ‘111000’, the software marks t_F as "indeterminable" and proceeds with the next test case.
- If there are less than 128 occurrences of ‘111000’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to use a different test pattern, and then redo the test.
- If there are 128 or more occurrences of ‘111000’, the software processes the last 128 reference waveforms.

An average waveform is then constructed by horizontally aligning 128 (or less) reference waveforms to a common anchor point, which is the zero crossing time of the first transition.

Once the average waveform is obtained, the value of t_F is measured as the time taken for the waveform to fall from $[V_{OD(0)} + 0.8 \cdot \{V_{OD(1)} - V_{OD(0)}\}]$ to $[V_{OD(0)} + 0.2 \cdot \{V_{OD(1)} - V_{OD(0)}\}]$.

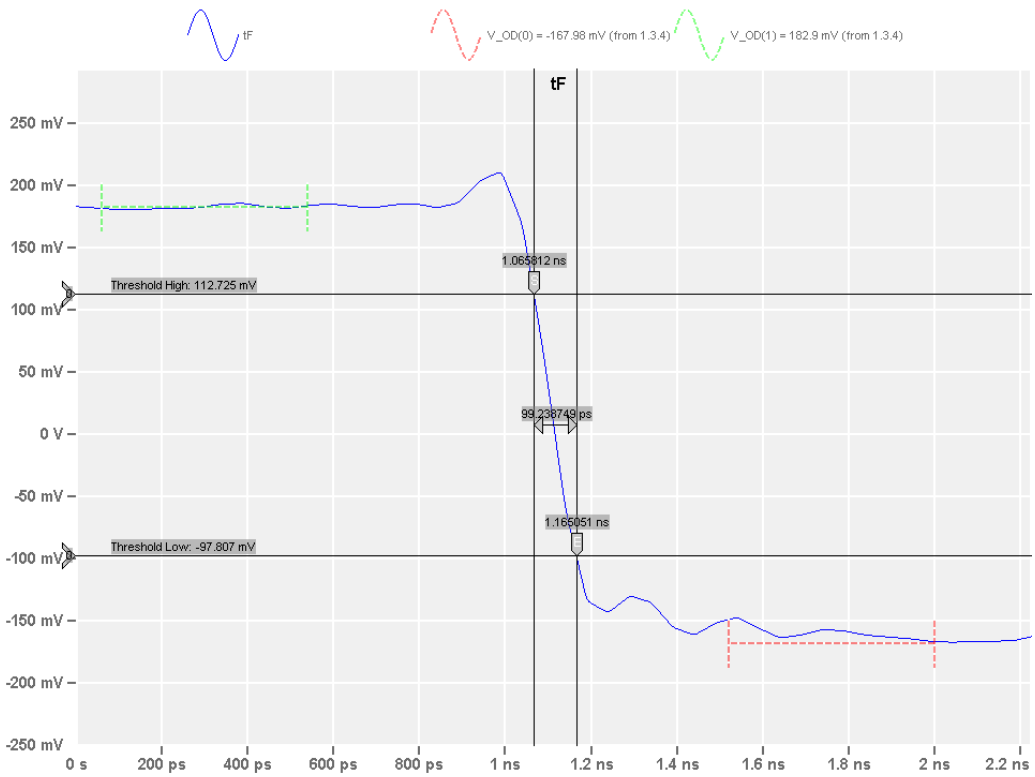


Figure 4-32: Typical result of a data lane HS transmit 80%-20% fall time measurement

V_{OD} = High speed transmission differential data signal
$V_{OD(1)}$ = HS transmit differential-1 voltage
$V_{OD(0)}$ = HS transmit differential-0 voltage
t_F = Fall time

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all data lanes.

4.5.3.13 Test 1.3.13 – Data Lane HS Exit: $T_{HS-TRAIL}$ Value

The purpose of this test case is to verify that the duration of the HS-TRAIL state, that occurs immediately after an HS transmission, is at least (60 ns + 4·UI).

In the measurement of the duration $T_{HS-TRAIL}$ of this state, the software distinguishes two cases:

- If the last bit in the HS-PAYLOAD is a '0', then the HS-TRAIL state is a differential-1 state.
  - The start of the state is defined at the time when the differential waveform crosses above the maximum differential input high threshold, V_{IDTH} (70 mV).
  - The end of the state is defined at the time when the differential waveform crosses below the maximum differential input high threshold, V_{IDTH} (70 mV).
- If the last bit in the HS-PAYLOAD is a '1', then the HS-TRAIL state is a differential-0 state.
  - The start of the state is defined at the time when the differential waveform crosses below the minimum differential input low threshold, V_{IDTL} (-70 mV for D-PHY 1.1; -40 mV for D-PHY≥ 1.2).
  - The end of the state is defined at the time when the differential waveform crosses above the minimum differential input low threshold, V_{IDTL} (-70 mV for D-PHY 1.1; -40 mV for D-PHY≥ 1.2).

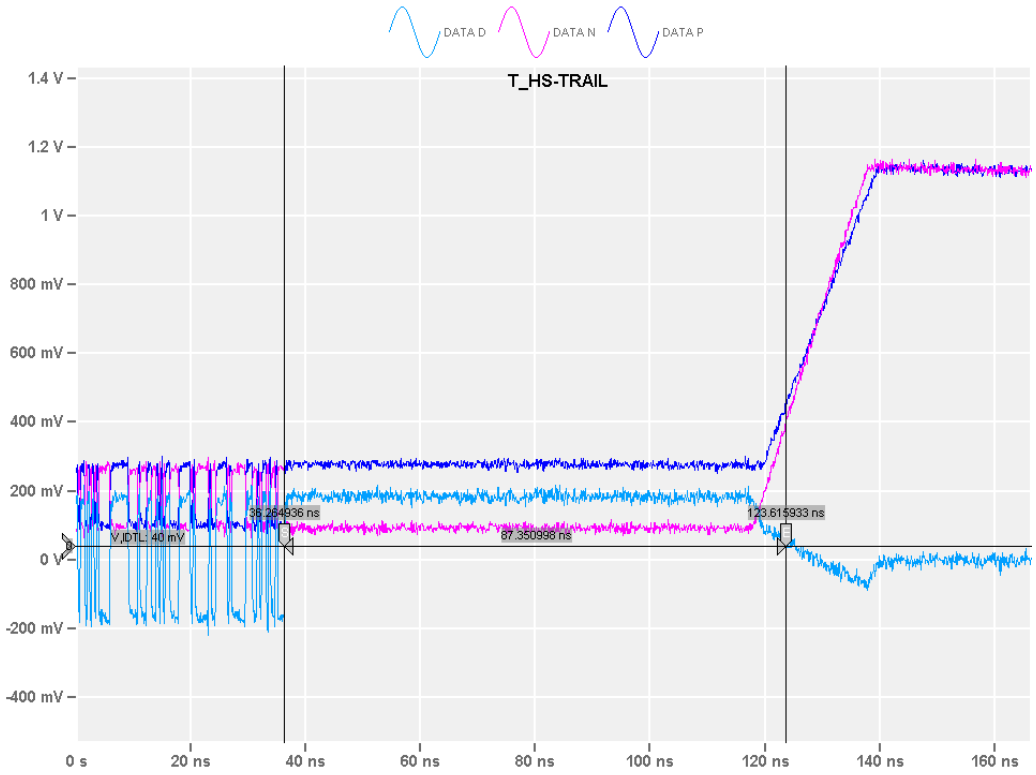


Figure 4-33: Typical result of an HS-TRAIL state duration measurement. This figure shows a failure case: T_HS-TRAIL < (60 ns + 4·UI)

Datp = Waveform of Data+ (V_{DP})
Datn = Waveform of Data- (V_{DN})
Datd = Differential waveform, V_{DP} - V_{DN}
T_HS-TRAIL = Duration of the HS-TRAIL state immediately after an HS transmission

This test case is tested for Z_{ID} = 100 ohms, only, and for all data lanes.

4.5.3.14 Test 1.3.14 – Data Lane HS Exit: 30%-85% Post-EoT Rise Time T_{REOT}

The purpose of this test case is to verify that the 30%-85% post-EoT rise time, T_{REOT} is not more than 35 ns.

To compute the 30%-85% Post-EoT Rise Time T_{REOT}, the software measures the rise time starting at the end of the HS-TRAIL state, and ending at the time when the V_{DP} rising edge crosses above the minimum logic 1 input voltage, $V_{IH,MIN}$ (880 mV).

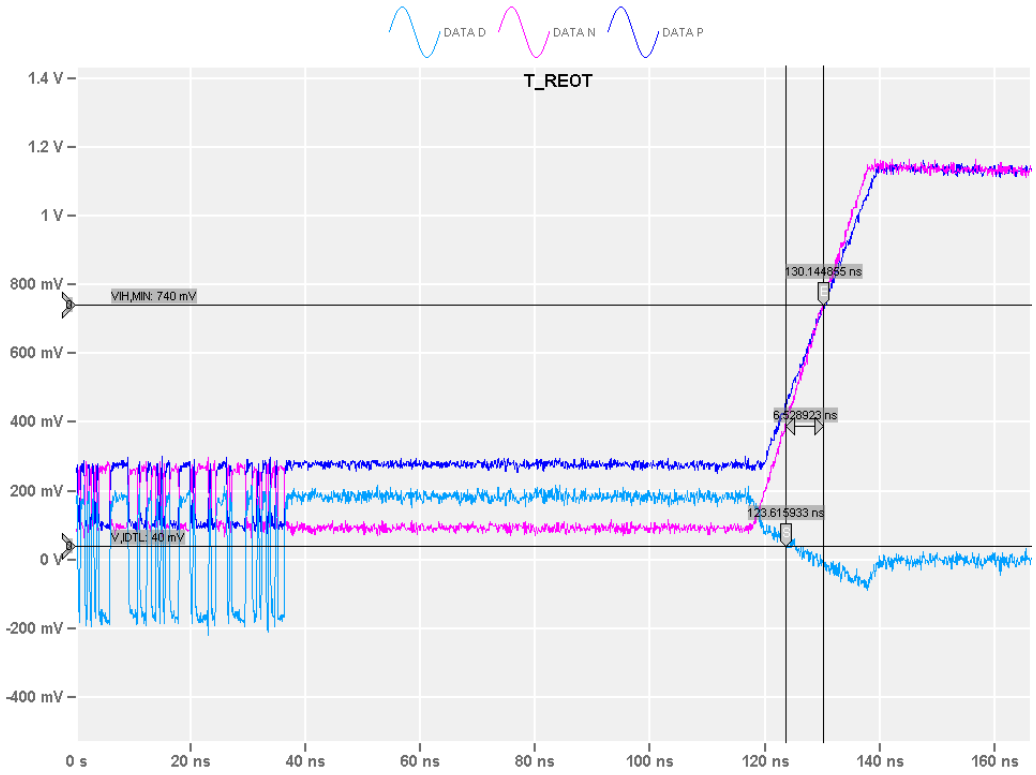


Figure 4-34: Typical result of a 30%-85% post-EoT rise time measurement

Datp = Waveform of Data+ (V_{DP})
Datn = Waveform of Data- (V_{DN})
Datd = Differential waveform, V_{DP} - V_{DN}
T_REOT = Duration of the 30%-85% post-EoT rise time

This test case is tested for Z_{ID} = 100 ohms, only, and for all data lanes.

4.5.3.15 Test 1.3.15 – Data Lane HS Exit: T_{EOT} Value

The purpose of this test case is to verify that the combined value of $T_{HS-TRAIL}$ and T_{REOT} is not more than (105 ns + 12·UI).

The software computes the combined value of $T_{HS-TRAIL}$ and T_{REOT}, as obtained according to Chapter 4.5.3.13, "Test 1.3.13 – Data Lane HS Exit: $T_{HS-TRAIL}$ Value", on page 65 and Chapter 4.5.3.14, "Test 1.3.14 – Data Lane HS Exit: 30%-85% Post-EoT Rise Time T_{REOT}", on page 66.

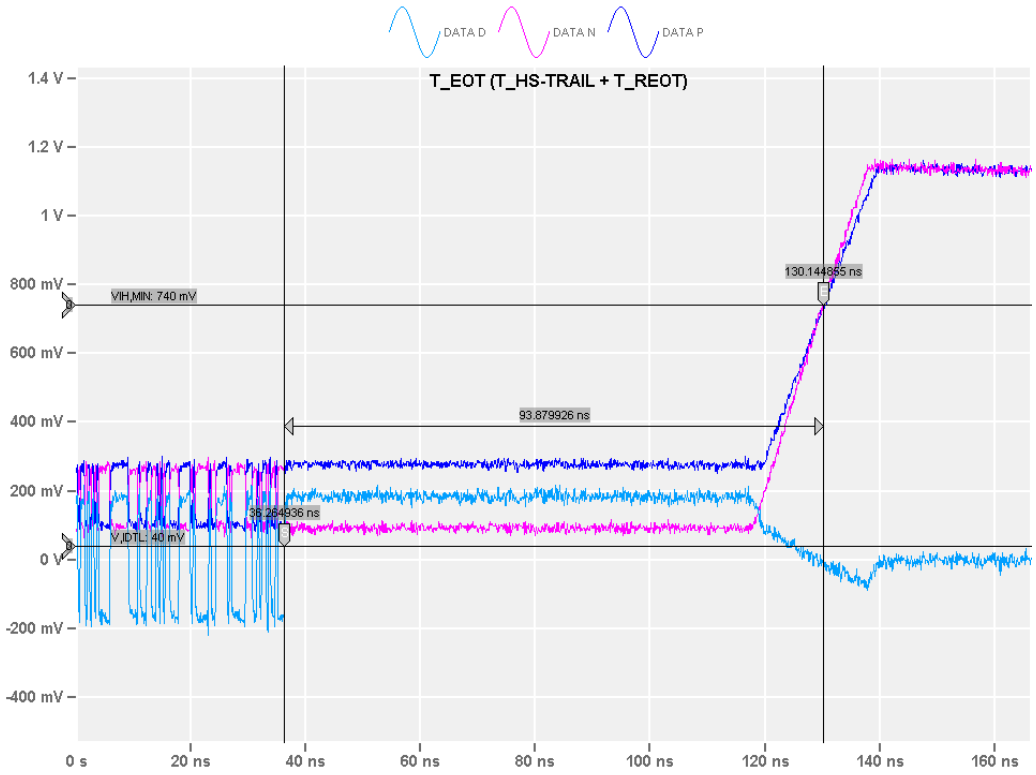


Figure 4-35: Typical result of a measurement of the combined value of T

Datp = Waveform of Data+ (V_{DP})
Datn = Waveform of Data- (V_{DN})
Datd = Differential waveform, V_{DP} - V_{DN}
T_EOT = T_HS-TRAIL + T_REOT

This test case is tested for Z_{ID} = 100 ohms, only, and for all data lanes.

4.5.3.16 Test 1.3.16 – Data Lane HS Exit: $T_{HS-EXIT}$ Value

The purpose of this test case is to verify that the duration of the LP-11 state, that occurs immediately after an HS transmission, is at least 100 ns.

The software measures $T_{HS-EXIT}$, the duration of the last LP-11 state that occurs immediately after an HS transmission, as follows:

The state is measured starting at the end of the HS-TRAIL state, and ending at the time when the V_{DP} falling edge crosses below the maximum logic 0 input voltage, $V_{IL,MAX}$ (550 mV). For the end of the HS-TRAIL state, two cases have to be distinguished:

- If HS-TRAIL is a differential-1 state, the end of the state will be defined at the time when the differential waveform crosses below the minimum differential input low threshold, V_{IDTL} (-70 mV for D-PHY 1.1; -40 mV for D-PHY≥ 1.2)
- If HS-TRAIL is a differential-0 state, the end of the state will be defined at the time when the differential waveform crosses above the maximum differential input high threshold, V_{IDTH} (70 mV for D-PHY 1.1; 40 mV for D-PHY≥ 1.2).

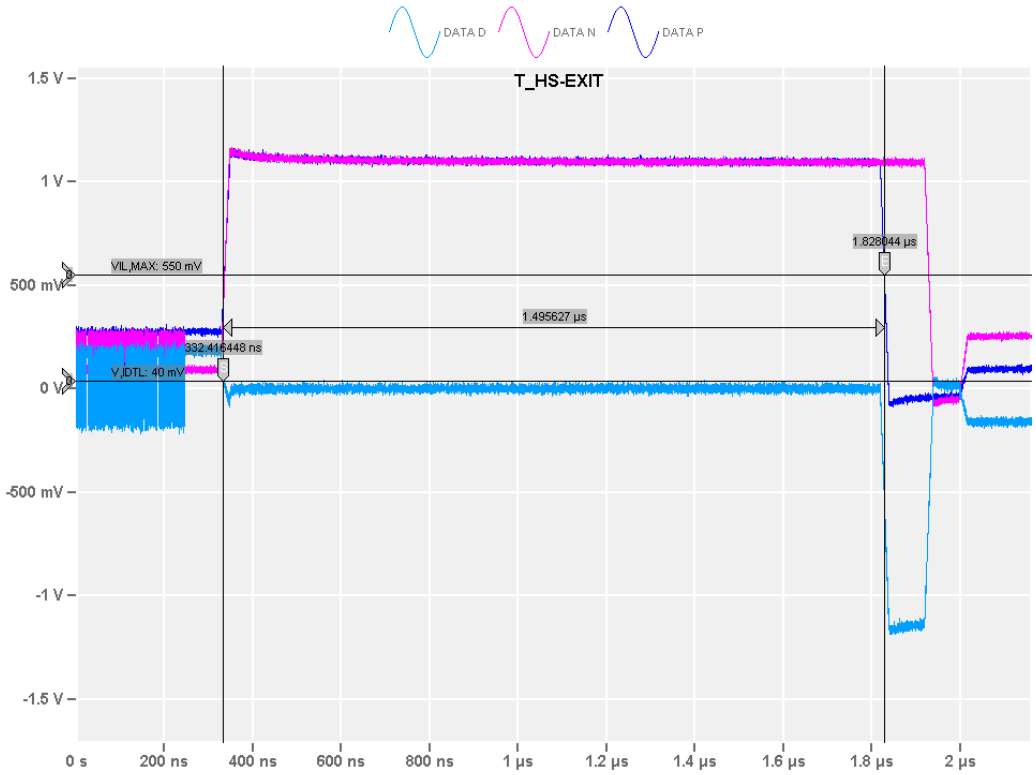


Figure 4-36: Typical result of a measurement of the duration of the LP-11 state immediately after an HS transmission

Datp = Waveform of Data+ (V_{DP})
Datn = Waveform of Data- (V_{DN})
T_HS-EXIT = duration of last LP-11 state after HS transmission

This test case is tested for Z_{ID} = 100 ohms, only, and for all data lanes.

4.6 Clock lane HS-TX signaling requirements (Group 4)

The purpose of Group 4 test cases is to verify the various transmission requirements specific to clock lane high speed (HS) signaling.

Group 4 consists of 18 test cases, described in Chapter 4.6.3, "Measurements", on page 74. A single captured HS-TX clock lane signaling sequence is measured, including LP exit and LP entry sequences that occur before and after the HS burst sequence. There are also test cases to measure the Unit Interval (UI, symbol duration time).

Particularly within the Group 4 test cases, the software can process three different clock types:

- Clock burst (non-continuous clock)
- Partial clock burst (where HS entry and HS exit are captured separately)
- Continuous clock

Therefore, various DUT configurations are required, to generate signals with these three clock types.

This group of test cases is only applicable to master devices.

4.6.1 Test setup

Table 4-5: Equipment for Group 4 Clock Lane HS-TX Signaling Requirements test

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 / RTP with 4 channels and at least 4 GHz bandwidth	1
Probes	Differential probes: at least 4 GHz bandwidth, or Single-ended probes: at least 4 GHz bandwidth	2 (*)
Test fixture	UNH-IOL MIPI D-PHY Reference Termination Board (RTB)[1]	1
DUT	Any MIPI D-PHY CSI-2 or DSI device	1
* In this group of tests, sampling the signals requires 2 probes: either single-ended, or differential used in single-ended mode.		
[1] We recommend to use a MIPI D-PHY Reference Termination Board (RTB) test fixture from the University of New Hampshire InterOperability Laboratory (UNH-IOL). Refer to https://www.iol.unh.edu/services/testing/mipi/fixtures.php.		

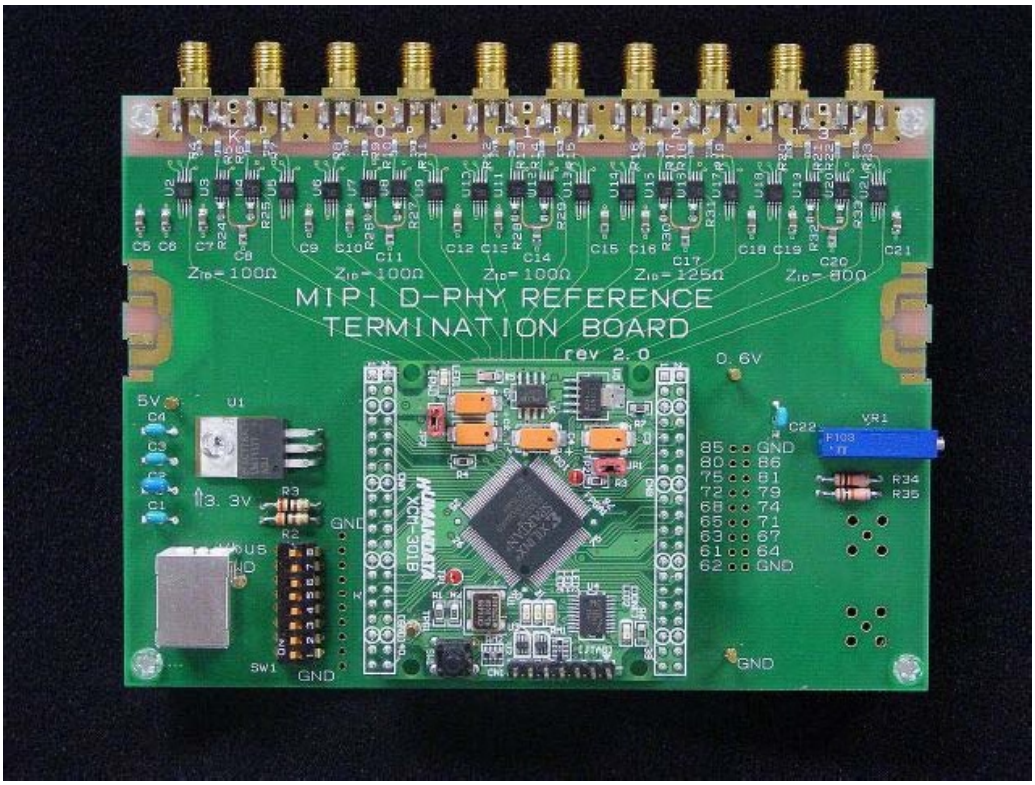


Figure 4-37: MIPI D-PHY Reference Termination Board test fixture from UNH-IOL

Waveform requirements

Group 4 test cases require the DUT to transmit HS clock burst waveforms, as shown in Figure 4-38, consisting of:

- (a) CLK-ZERO
- (b) CLK_PRE
- (c) Toggling HS-0/HS-1
- (d) CLK-TRAIL

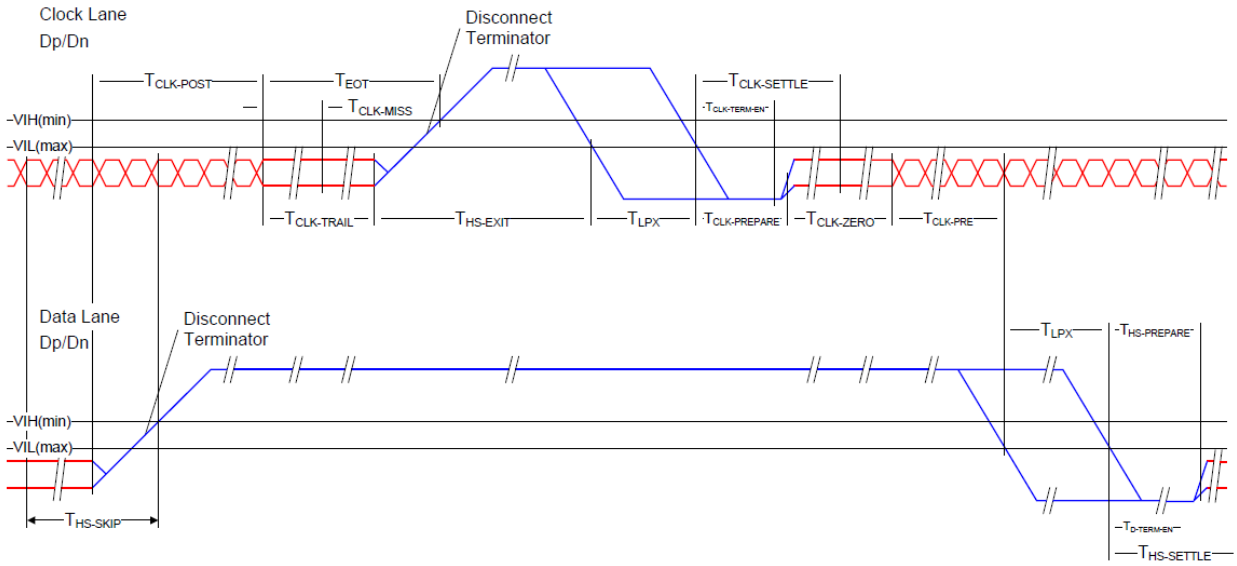


Figure 4-38: A typical MIPI D-PHY HS clock burst waveform (courtesy of MIPI Alliance Specification for D-PHY version 1.1)

The software requires at least one set of complete clock burst waveforms for correct processing, to perform the test successfully.

HS Clock transmission requirements

More than half of the Group 4 test cases are analyzing the clock signal in HS clock transmission. Therefore, it is important for the CLK-Toggling HS-0/HS-1 to contain at least:

- (a) 128 occurrences of '01'
- (b) 128 occurrences of '10'

If the CLK-Toggling HS-0/HS-1 does not meet these minimum requirements, the software does still process the waveforms, but the measurements may not be accurate, and test results may be invalid.

It is recommended to use reference HS test patterns or images. UNH-IOL has created a "PATGUI" utility, which can be used to generate test patterns and images for various resolutions and formats. For members of the MIPI Alliance, this utility can be obtained free of charge from the MIPI Testing Resources page on the MIPI Alliance website (https://members.mipi.org/mipi-testing/workspace/Test_Vehicle_Board_Resources).

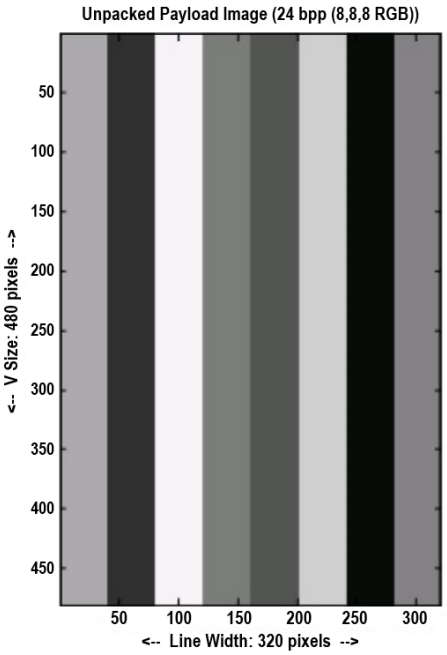


Figure 4-39: Example reference HS test pattern, RGB888 format (courtesy: MIPI Alliance, D-PHY specs)

Settings in the "HS Configuration" dialog box

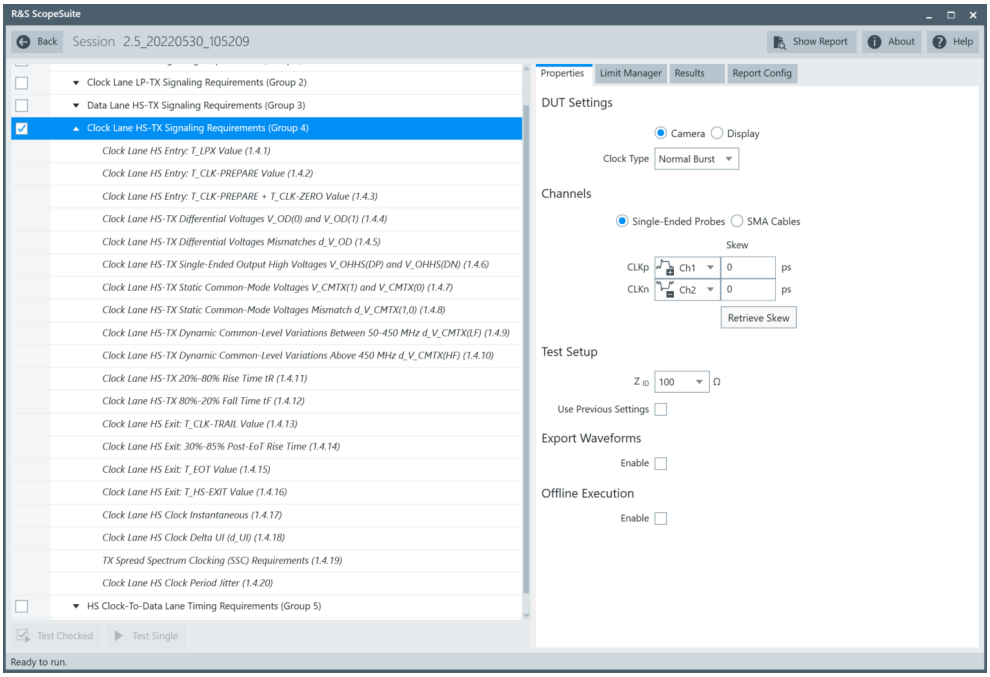
See also: Chapter 4.2, "Test configuration for D-PHY", on page 20.

- **DUT Settings**
  Select if the DUT is a "Camera" or a "Display".
  You can also set the "Clock type" according to your device.
- **Channels**
  This setting depends on the probes that are used to capture the clock signals .
  Select the channels for the measurement and set or retrieve the skew.
- **Z_{ID}**
  Each lane of the RTB board has a specific termination value. According to your test requirements, connect your DUTs to the lane with the corresponding Z_{ID} value.
  For more information about the RTB board, refer to its datasheet.
  - If Z_{ID} is 100 ohms, the pair of clock lanes (clk_p and clk_n) has to be terminated with the 100 ohms loads on the RTB. This can be done on the lanes Data0 or Data1 of the RTB board.
  - If Z_{ID} is 80 ohms or 125 ohms, the pair of clock lanes under test have to be terminated with the 80 ohms or 125 ohms loads on the RTB.

Data2 lane of the RTB board has a Z_{ID} of 125 ohms and Data3 lane has a Z_{ID} of 80 ohms.

4.6.2 Performing Group 4 test cases

1. Start running the tests as described in Chapter 4.1, "Starting D-PHY compliance tests", on page 20.
2. Select "Clock Lane HS-TX Signaling Requirements (Group 4)".



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
   This group of tests uses the MIPI D-PHY Reference Termination Board (RTB) test fixture from the UNH-IOL.
   Only two clock signals are required for the test. The clock signals can be tapped either from the DUT or RTB, or even on the SMA cables between the DUT and the RTB.
   When you have finished all steps, the compliance test runs automatically.

Further steps:

- Chapter 3.3, "Getting test results", on page 16

4.6.3 Measurements

4.6.3.1 Test 1.4.1 – Clock Lane HS Entry: T_{LPX} Value

The purpose of this test case is to verify the duration of the last LP-01 state immediately before HS transmission is at least 50 ns.

The software measures the duration of the last LP-01 state that occurs immediately before an HS transmission. This duration is labeled T_{LPX}.

The duration is measured

- Starting at the time when the V_{DP} falling edge crosses below the maximum logic 0 input voltage, $V_{IL,MAX}$ (550 mV)
- Ending at the time when the V_{DN} falling edge crosses below the same logic 0 input voltage $V_{IL,MAX}$

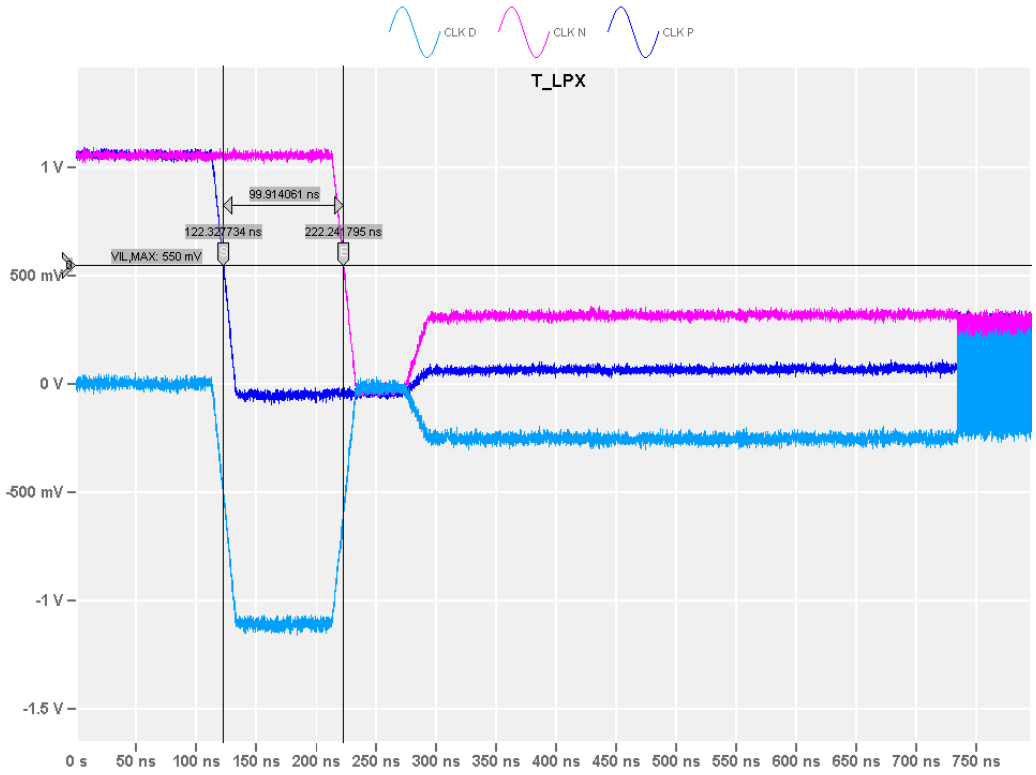


Figure 4-40: Typical result of a clock lane T_LPX measurement

Clkp = Waveform of Clock+ (V_{DP})
Clkn = Waveform of Clock- (V_{DN})
Clkd = Differential waveform, V_{DP} - V_{DN}
T_LPX = Duration of last LP-01 state immediately before HS transmission

This test case is tested for Z_{ID} = 100 ohms, only, and for all clock lanes.

4.6.3.2 Test 1.4.2 – Clock Lane HS Entry: $T_{CLK\text{-}PREPARE}$ Value

The purpose of this test case is to verify that the duration of the last LP-00 state, $T_{CLK\text{-}PREPARE}$, prior to driving $T_{CLK\text{-}ZERO}$ when entering HS mode, is between 38 ns and 95 ns.

The software measures the duration of the last LP-00 state that occurs immediately before an HS transmission. This duration is labeled $T_{CLK\text{-}PREPARE}$

The duration is measured

- Starting at the time when the V_{DN} falling edge crosses below the maximum logic 0 input voltage, $V_{IL,MAX}$ (550 mV)
- Ending at the time when the differential waveform crosses below the minimum differential input low threshold, V_{IDTL} (-70 mV for D-PHY 1.1; -40 mV for D-PHY≥ 1.2).

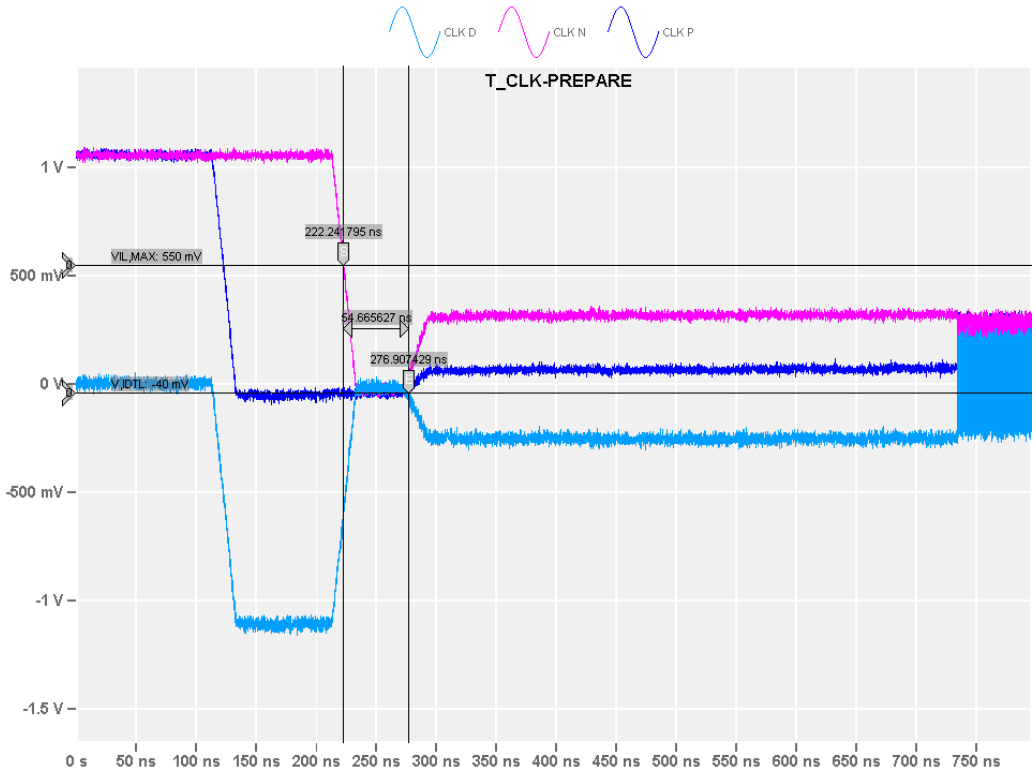


Figure 4-41: Typical result of a clock lane T_LPX measurement

Clkp = Waveform of Clock+ (V_{DP})
Clkn = Waveform of Clock- (V_{DN})
Clkd = Differential waveform, V_{DP} - V_{DN}
T_CLK-PREPARE = Duration of last LP-00 state immediately before HS transmission

This test case is tested for Z_{ID} = 100 ohms, only, and for all clock lanes.

4.6.3.3 Test 1.4.3 – Clock Lane HS Entry: $T_{CLK\text{-}PREPARE}$ + $T_{CLK\text{-}ZERO}$ Value

The purpose of this test case is to verify that the combined value of $T_{CLK\text{-}PREPARE}$ and the duration prior to the clock transmission, $T_{CLK\text{-}ZERO}$, is at least 300 ns.

The duration is measured:

- Starting at the time when the differential waveform crosses below the minimum differential input low threshold, V_{IDTL} (-70 mV for D-PHY 1.1; -40 mV for D-PHY≥ 1.2)
- Ending at the $T_{CLK\text{-}ZERO}$ HS differential state

The software then computes the combined value of $T_{CLK\text{-}PREPARE}$ (see Chapter 4.6.3.2, "Test 1.4.2 – Clock Lane HS Entry: $T_{CLK\text{-}PREPARE}$ Value", on page 75) and $T_{CLK\text{-}ZERO}$.

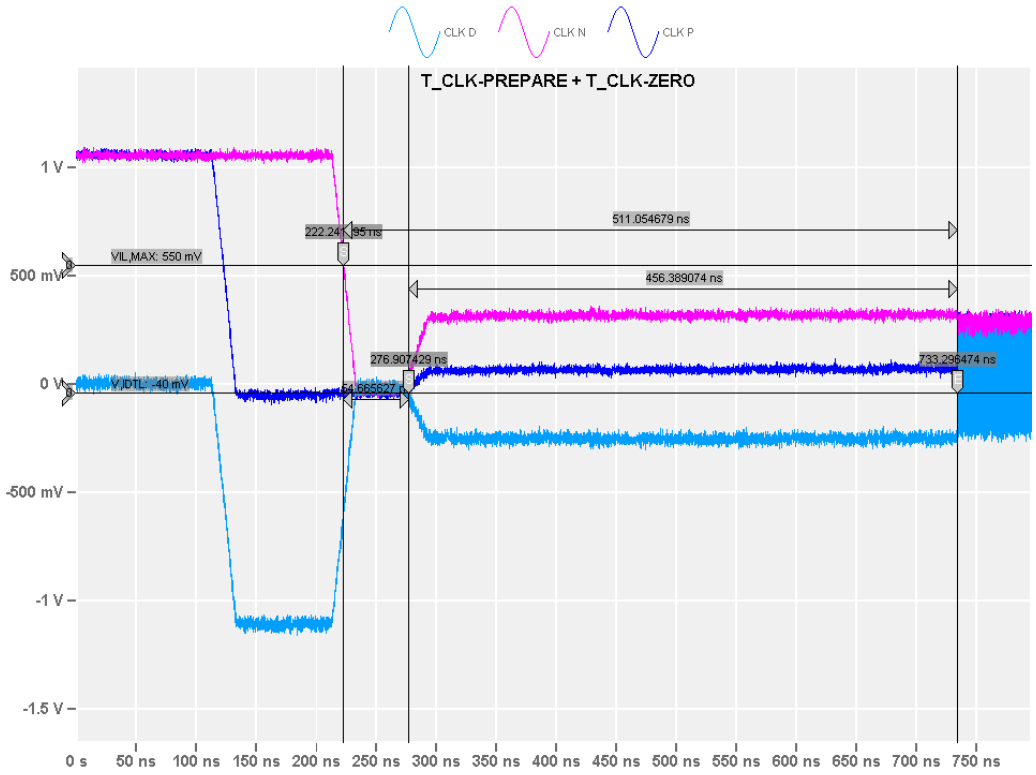


Figure 4-42: Typical result of a clock lane T_CLK-PREPARE + T_CLK-ZERO measurement

Clkp = Waveform of Clock+ (V_{DP})
Clkn = Waveform of Clock- (V_{DN})
Clkd = Differential waveform, V_{DP} - V_{DN}
T_CLK-PREPARE = Duration of last LP-00 state immediately before HS transmission
T_CLK-ZERO = Duration of the CLK-ZERO state immediately before clock transmission

This test case is tested for Z_{ID} = 100 ohms, only, and for all clock lanes.

4.6.3.4 Test 1.4.4 – Clock Lane HS-TX Differential Voltages $V_{OD(0)}$ and $V_{OD(1)}$

The purpose of this test case is to verify, that

- The clock lane HS transmit differential-0 voltage ($V_{OD(0)}$) is between -140 mV and -270 mV
- The clock lane HS transmit differential-1 voltage ($V_{OD(1)}$) is between 140 mV and 270 mV.

$V_{OD(0)}$: To measure the clock transmit differential-0 voltage, the software searches for reference waveforms with the data pattern ‘10’ in the clock transmission differential data signal. Four cases are to be distinguished:

- If there is no occurrence of ‘10’, the software marks $V_{OD(0)}$ as "indeterminable" and proceeds with the next measurement ($V_{OD(1)}$).
- If there are less than 128 occurrences of ‘10’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to use a different test pattern, and then redo the test.

- For the clock type of partial clock burst and continuous clock, if there are less than 128 occurrences of ‘10’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to modify the time base of the oscilloscope to acquire more waveforms, and then redo the test.
- If there are 128 or more occurrences of ‘10’, the software processes the last 128 reference waveforms.

The reason for this procedure is this: In some cases, transient effects introduced by some high impedance probes can introduce a small error in the HS common-mode level at the beginning of the transmission. This error can be significant enough to affect the test result. Therefore, an average waveform is constructed by horizontally aligning 128 (or less) reference waveforms to a common anchor point, which is the zero crossing time of the first transition.

The value of $V_{OD(0)}$ is then determined from that average waveform: it is the mean of all samples that are closest to the center of the second bit, which is the ‘0’ bit.

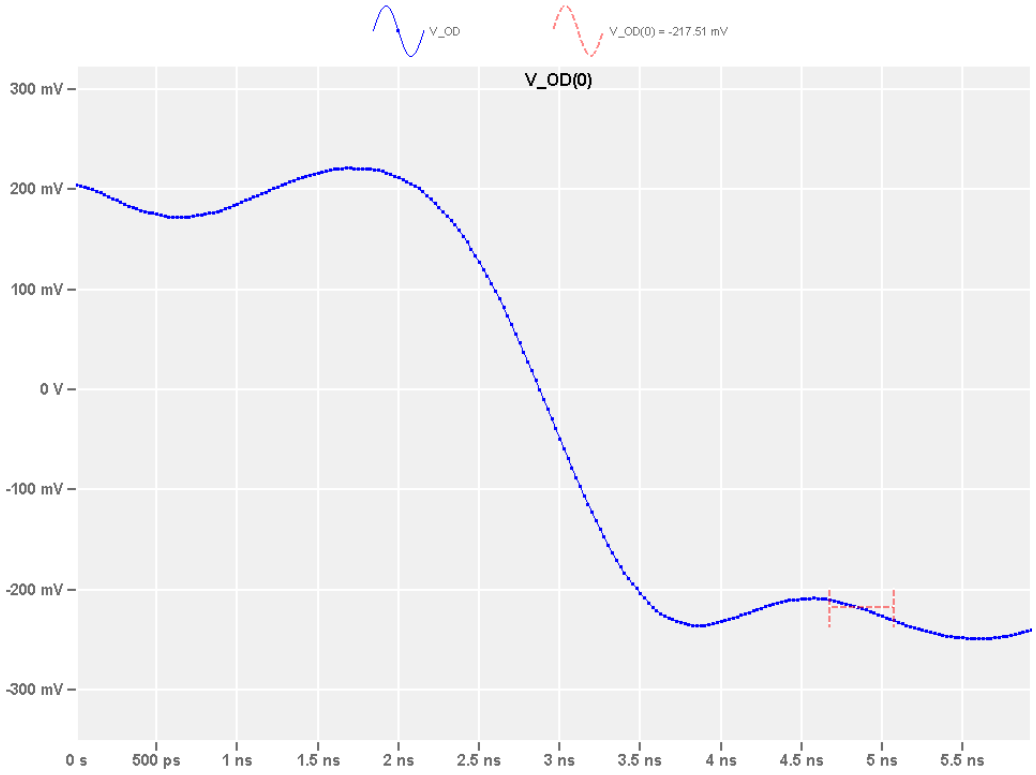


Figure 4-43: Typical result of a clock lane HS transmit differential-0 voltage measurement. This figure shows a failure case: V_OD > -140 mV

$V_{OD(1)}$: The software measures the clock transmit differential-1 voltage in a similar way as $V_{OD(0)}$. Two exceptions are:

- It searches for reference waveforms with the data pattern ‘01’ (instead of ‘10’).
- From the obtained average waveform, the value of $V_{OD(1)}$ is measured as the mean of all samples that are closest to the center of the second bit, which is the ‘1’ bit (instead of ‘0’ bit).

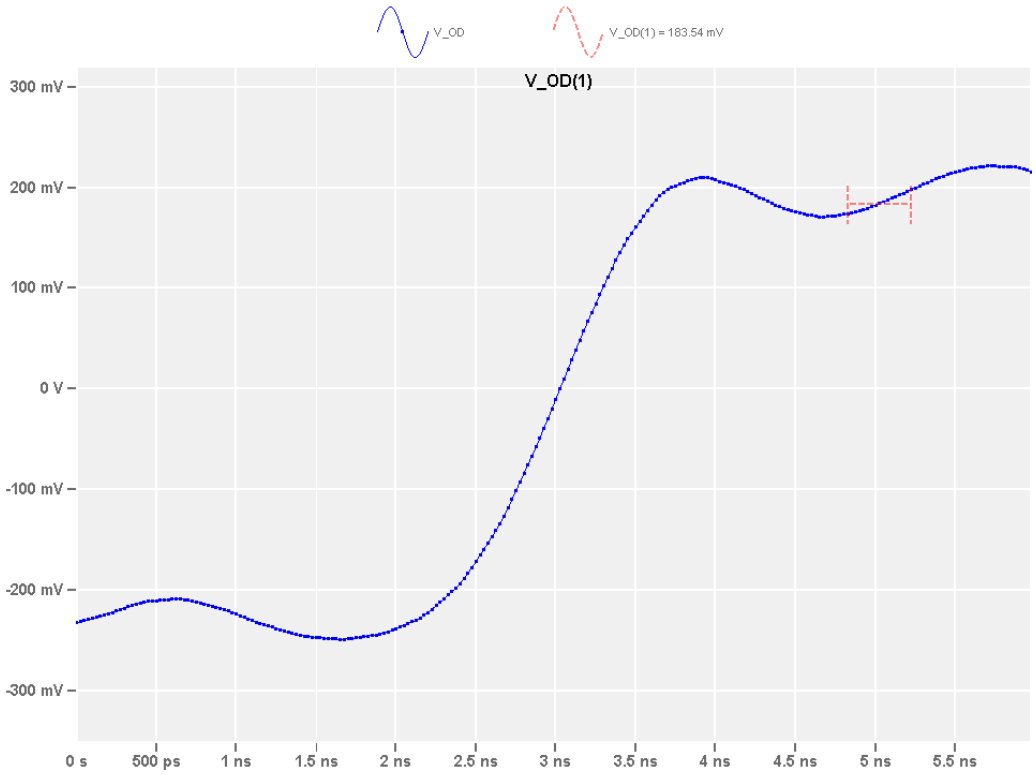


Figure 4-44: Typical result of a clock lane HS transmit differential-1 voltage measurement. This figure shows a failure case: V_OD < 140 mV

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all clock lanes.

4.6.3.5 Test 1.4.5 – Clock Lane HS-TX Differential Voltage Mismatch ΔV_{OD}

The purpose of this test case is to verify that the clock lane HS transmit differential voltage mismatch (ΔV_{OD}) is between +14 mV and -14 mV.

Using the values obtained in Chapter 4.6.3.4, "Test 1.4.4 – Clock Lane HS-TX Differential Voltages $V_{OD(0)}$ and $V_{OD(1)}$", on page 77, the software computes the clock transmit differential voltage mismatch according to this formula:

$\Delta V_{OD} = |V_{OD(1)}| - |V_{OD(0)}|$

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all clock lanes.

4.6.3.6 Test 1.4.6 – Clock Lane HS-TX Single-Ended Output Voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$

The purpose of this test case is to verify that the single-ended HS output high voltage is not more than 360 mV.

$V_{OHHS(DP)}$: To measure the D_P HS output high voltage, the software searches for reference waveforms with the data pattern ‘01’ in the HS transmission differential data signal.

Although – in this context – it is referring to the single-ended signal, ‘01’ on the differential signal means the same pattern on the D_P single-ended signal.

Four cases are to be distinguished:

- If there is no occurrence of ‘01’, the software marks $V_{OHHS(DP)}$ as "indeterminable" and proceeds with the next measurement ($V_{OHHS(DN)}$).
- If there are less than 128 occurrences of ‘01’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to use a different test pattern, and then redo the test.
- For the clock type of partial clock burst and continuous clock, if there are less than 128 occurrences of ‘01’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to modify the time base of the oscilloscope to acquire more waveforms, and then redo the test.
- If there are 128 or more occurrences of ‘01’, the software processes the last 128 reference waveforms.

An average waveform is then constructed by horizontally aligning 128 (or less) reference waveforms to a common anchor point, which is the zero crossing time of the first transition.

The value of $V_{OHHS(DP)}$ is then determined from that average waveform: it is the mean of all samples that are closest to the center of the second bit, which is the ‘1’ bit.

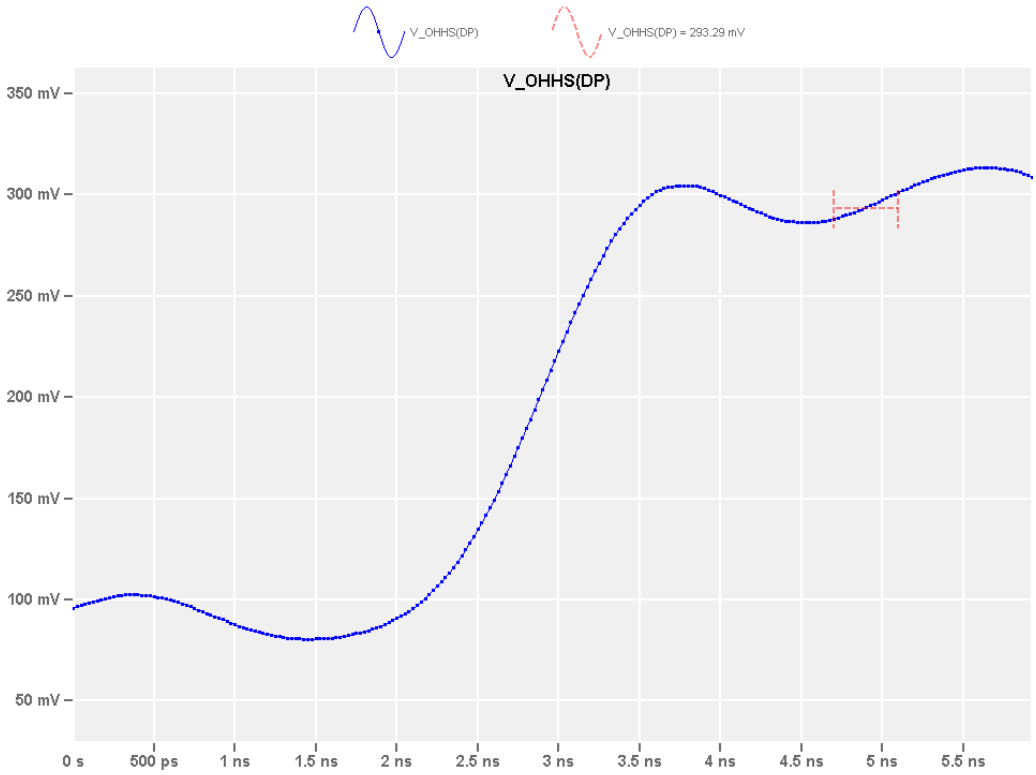


Figure 4-45: Typical result of a clock lane HS single-ended output high voltage measurement

V_OHHS = High speed output high voltage
DP = Data positive (D+)

$V_{OHHS(DN)}$: The software measures the D_N HS output high voltage in a similar way as $V_{OHHS(DP)}$, because the data pattern ‘01’ is also required.

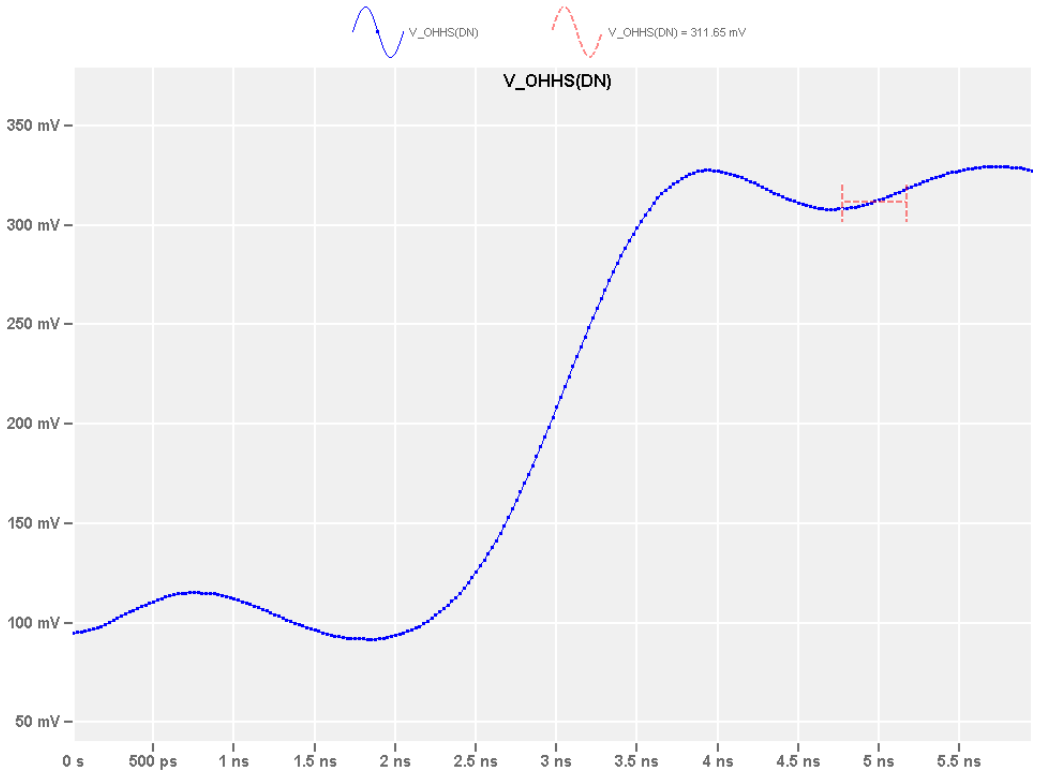


Figure 4-46: Typical result of a clock lane HS single-ended output high voltage measurement

V_OHHS = High speed output high voltage
DN = Data negative (D-)

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all clock lanes.

4.6.3.7 Test 1.4.7 – Clock Lane HS-TX Static Common-Mode Voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$

The purpose of this test case is to verify that the clock lane HS transmit static common-mode voltages ($V_{CMTX(1)}$ and $V_{CMTX(0)}$) are between 150 mV and 250 mV.

The HS transmit static common-mode voltage is defined in the specification as the arithmetic mean of the value of the voltages at D_P and D_N:

$V_{CMTX} = (V_{DP} + V_{DN})/2$

$V_{CMTX(1)}$: The software measures the HS transmit differential-1 static common-mode voltage, by searching for all occurrences of bit ‘1’ in the HS transmission differential data signal. Three cases are to be distinguished:

- If there are less than 5000 occurrences of ‘1’, the software does still process the bits. However, the test results may be invalid; it is recommended to use a different test pattern, and then redo the test.
- For the clock type of partial clock burst and continuous clock, if there are less than 5000 occurrences of ‘1’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to modify

the time base of the oscilloscope to acquire more waveforms, and then redo the test.

- If there are 5000 or more occurrences of '1', the software processes all of them.

For every occurrence of '1' that the software can find in the differential signal, it computes the HS transmitter static common-mode voltage according to the formula mentioned above. The value of $V_{CMTX(1)}$ is measured as the average of these common-mode voltages.

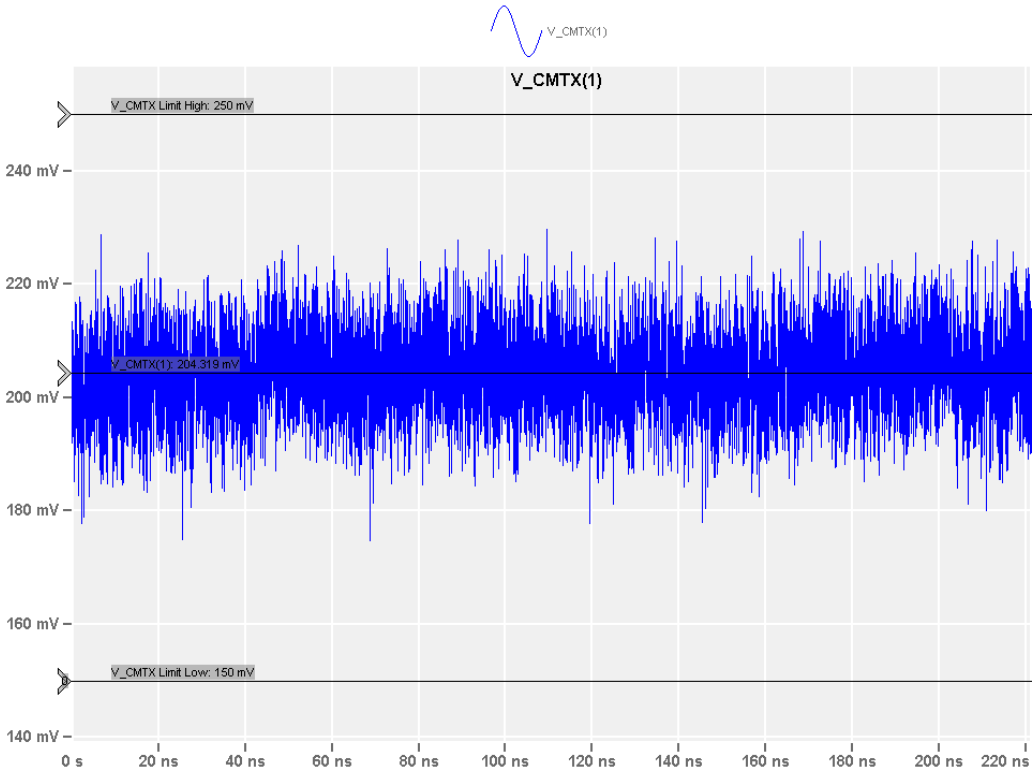


Figure 4-47: Typical result of a clock lane HS transmit differential-1 static common-mode voltage measurement, V_CMTX(1)

$V_{CMTX(0)}$: The software measures the HS transmit differential-0 static common-mode voltage in a similar way as $V_{CMTX(1)}$. One exception is:

- It searches for all occurrences of bit '0' instead of bit '1'.

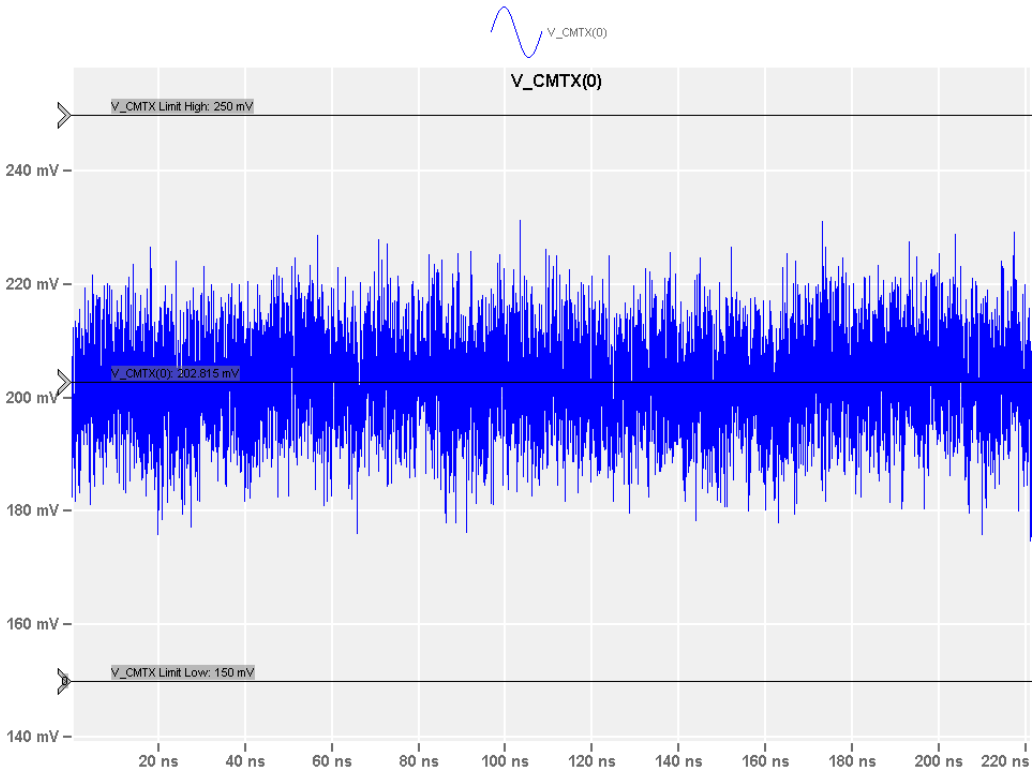


Figure 4-48: Typical result of a clock lane HS transmit differential-0 static common-mode voltage measurement, V_CMTX(0)

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all clock lanes.

4.6.3.8 Test 1.4.8 – Clock Lane HS-TX Static Common-Mode Voltage Mismatch $\Delta V_{CMTX(1,0)}$

The purpose of this test is to verify that the clock lane HS transmit static common-mode voltage mismatch is between +5 mV and -5 mV.

Using the values obtained in Chapter 4.6.3.7, "Test 1.4.7 – Clock Lane HS-TX Static Common-Mode Voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$", on page 82, the software computes the clock lane HS transmit static common-mode voltage mismatch $\Delta V_{CMTX(1,0)}$ according to this formula:

$\Delta V_{CMTX(1,0)} = (\Delta V_{CMTX(1)} - \Delta V_{CMTX(0)})/2$

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all clock lanes.

4.6.3.9 Test 1.4.9 – Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450 MHz $\Delta V_{CMTX(LF)}$

The purpose of this test case is to verify that the common-level variation between 50-450 MHz is not more than 25 mV_{PEAK}.

The common-level variation between 50-450 MHz $\Delta V_{CMTX(LF)}$ is measured as follows:

The software compiles a list of clock lane HS transmit static common-voltage voltages for every zero crossing of the clock signal, using the formula stated in Chapter 4.6.3.7, "Test 1.4.7 – Clock Lane HS-TX Static Common-Mode Voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$", on page 82. This list will be used as the input to an 8th order Butterworth bandpass filter with cutoff frequencies of 50 MHz and 450 MHz, respectively. The value of $\Delta V_{CMTX(LF)}$ is measured as the absolute peak voltage at the output of the bandpass filter.

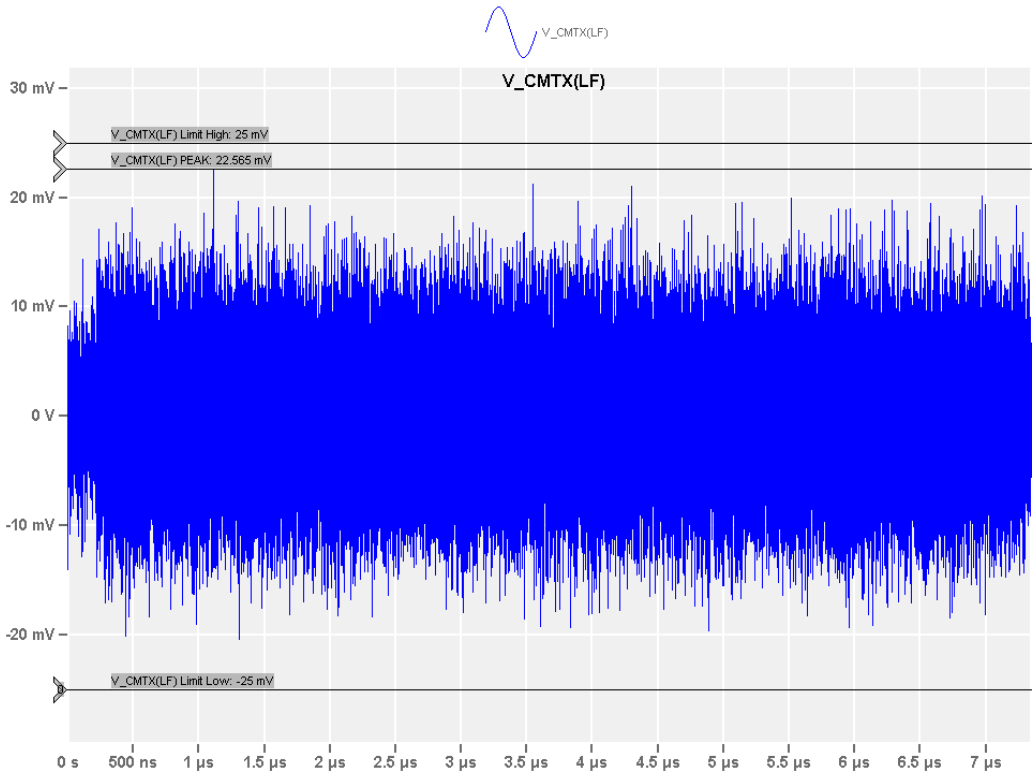


Figure 4-49: Typical result of a clock lane HS transmit dynamic common-level variations measurement at low frequencies, V_CMTX(LF)

This test case is tested for Z_{ID} = 100 ohms, only, and for all clock lanes.

4.6.3.10 Test 1.4.10 – Clock Lane HS-TX Dynamic Common-Level Variations Above 450 MHz $\Delta V_{CMTX(HF)}$

The purpose of this test case is to verify that the common-level variation above 450 MHz is not more than 15 mV_{RMS}.

The common-level variation above 450 MHz $\Delta V_{CMTX(HF)}$ is measured as follows:

The software uses the same list of HS transmit static common-voltage voltages from Chapter 4.6.3.9, "Test 1.4.9 – Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450 MHz $\Delta V_{CMTX(LF)}$", on page 84 as the input to an 8th order Butterworth

highpass filter with a cutoff frequency of 450 MHz. The value of $\Delta V_{CMTX(HF)}$ is measured as the RMS voltage at the output of the highpass filter.

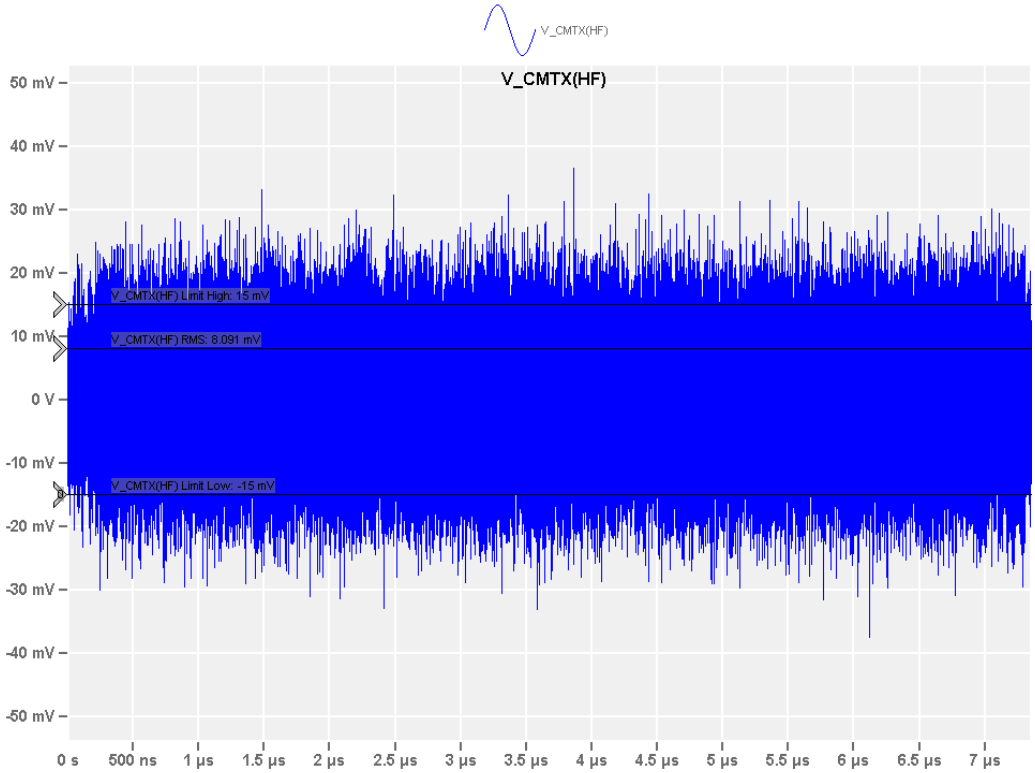


Figure 4-50: Typical result of a clock lane HS transmit dynamic common-level variations measurement at high frequencies, V_CMTX(HF)

This test case is tested for Z_{ID} = 100 ohms, only, and for all clock lanes.

4.6.3.11 Test 1.4.11 – Clock Lane HS-TX 20%-80% Rise Time t_R

The purpose of this test case is to verify that the 20%-80% rise time is:

- Between 150 ps and 0.3·UI when operating at HS bit rates up to 1 Gbps.
- Between 100 ps and 0.35·UI when operating at HS bit rates greater than 1 Gbps.

To measure the 20%-80% rise time t_R, the software searches for reference waveforms with the data pattern ‘01’ in the clock lane HS transmission differential data signal. Four cases are to be distinguished:

- If there is no occurrence of ‘01’, the software marks t_R as "indeterminable" and proceeds with the next test case.
- If there are less than 128 occurrences of ‘01’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to use a different test pattern, and then redo the test.
- For the clock type of partial clock burst and continuous clock, if there are less than 128 occurrences of ‘01’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to modify

the time base of the oscilloscope to acquire more waveforms, and then redo the test.

- If there are 128 or more occurrences of '01', the software processes the last 128 reference waveforms.

An average waveform is then constructed by horizontally aligning 128 (or less) reference waveforms to a common anchor point, which is the zero crossing time of the first transition.

Once the average waveform is obtained, the value of t_R is measured as the time taken for the waveform to rise from $[V_{OD(0)} + 0.2 \cdot \{V_{OD(1)} - V_{OD(0)}\}]$ to $[V_{OD(0)} + 0.8 \cdot \{V_{OD(1)} - V_{OD(0)}\}]$.

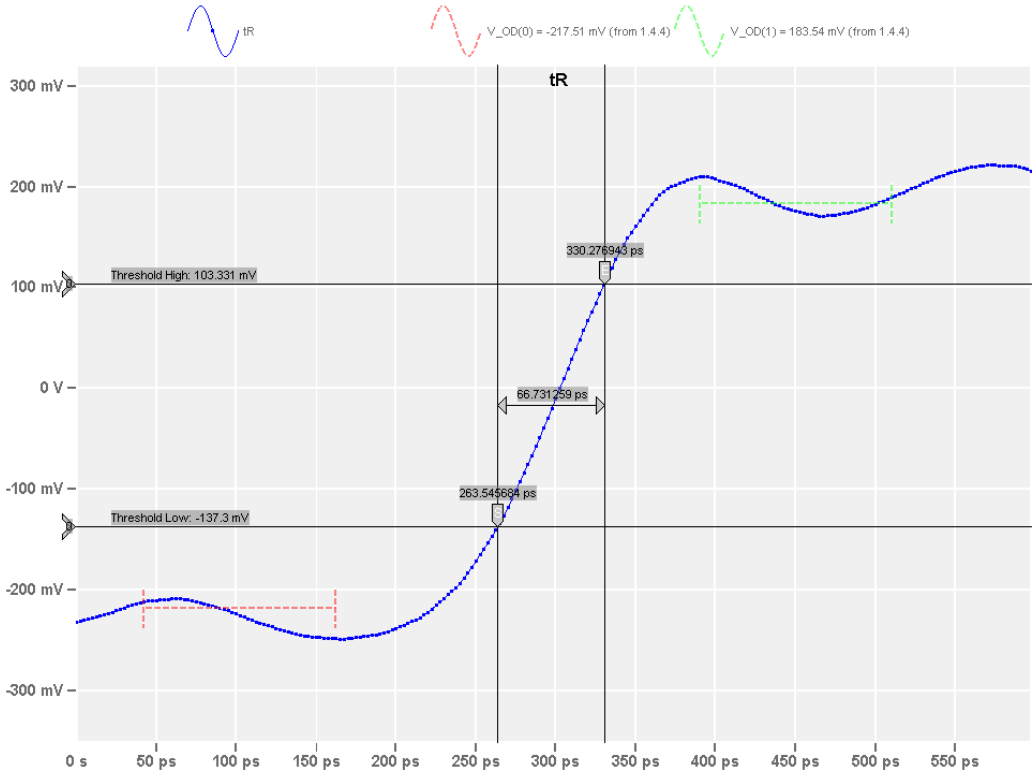


Figure 4-51: Typical result of a clock lane HS transmit 20%-80% rise time measurement

V_{OD} = Clock lane high speed transmission differential data signal
$V_{OD(0)}$ = Clock lane HS transmit differential-0 voltage
$V_{OD(1)}$ = Clock lane HS transmit differential-1 voltage
t_R = Rise time

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all clock lanes.

4.6.3.12 Test 1.4.12 – Clock Lane HS-TX 80%-20% Fall Time t_F

The purpose of this test case is to verify that the 80%-20% fall time is:

- Between 150 ps and 0.3·UI when operating at HS bit rates up to 1 Gbps.

- Between 100 ps and 0.35·UI when operating at HS bit rates greater than 1 Gbps.

To measure the 80%-20% fall time t_F, the software searches for reference waveforms with the data pattern ‘10’ in the clock lane HS transmission differential data signal. Four cases are to be distinguished:

- If there is no occurrence of ‘10’, the software marks t_F as "indeterminable" and proceeds with the next test case.
- If there are less than 128 occurrences of ‘10’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to use a different test pattern, and then redo the test.
- For the clock type of partial clock burst and continuous clock, if there are less than 128 occurrences of ‘10’, the software does still process the reference waveforms. However, the test results may be invalid; in this case, it is recommended to modify the time base of the oscilloscope to acquire more waveforms, and then redo the test.
- If there are 128 or more occurrences of ‘10’, the software processes the last 128 reference waveforms.

An average waveform is then constructed by horizontally aligning 128 (or less) reference waveforms to a common anchor point, which is the zero crossing time of the first transition.

Once the average waveform is obtained, the value of t_F is measured as the time taken for the waveform to fall from $[V_{OD(0)} + 0.8 \cdot \{V_{OD(1)} - V_{OD(0)}\}]$ to $[V_{OD(0)} + 0.2 \cdot \{V_{OD(1)} - V_{OD(0)}\}]$.

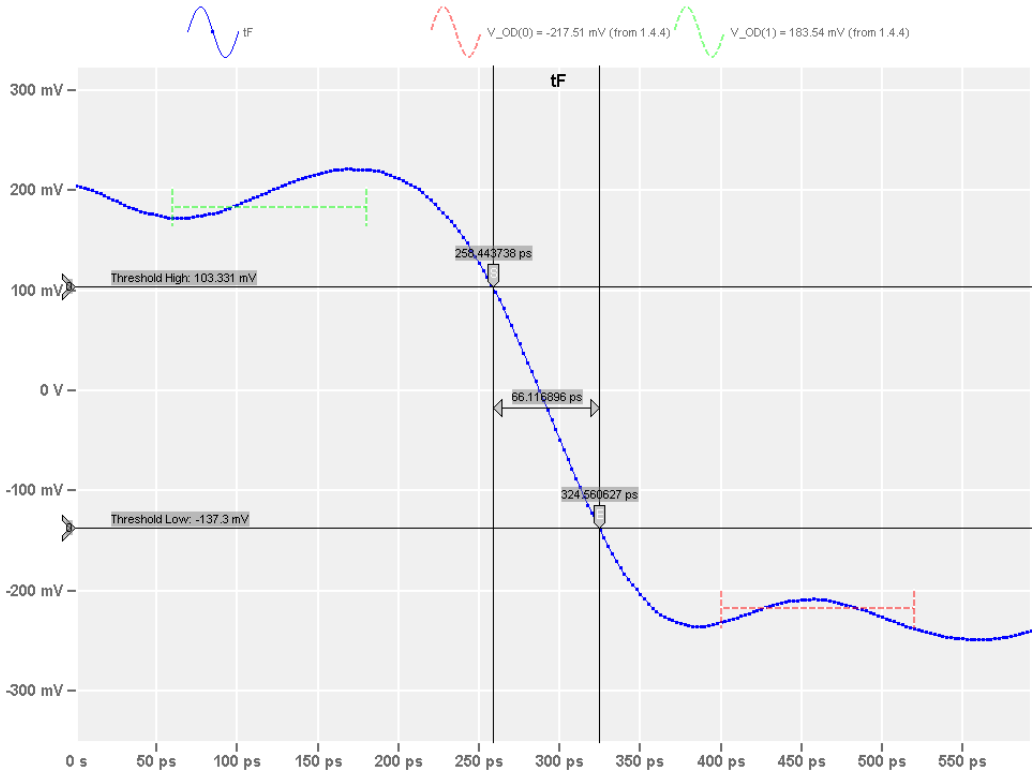


Figure 4-52: Typical result of a clock lane HS transmit 80%-20% fall time measurement

V_{OD} = Clock lane high speed transmission differential data signal
$V_{OD(1)}$ = Clock lane HS transmit differential-1 voltage
$V_{OD(0)}$ = Clock lane HS transmit differential-0 voltage
t_F = Fall time

This test case is executed for all three cases of Z_{ID} (100 ohms, 80 ohms, and 125 ohms), as well as for all clock lanes.

4.6.3.13 Test 1.4.13 – Clock Lane HS Exit: $T_{CLK-TRAIL}$ Value

The purpose of this test case is to verify that the duration of the CLK-TRAIL state, that occurs immediately after a clock lane HS transmission, is at least 60 ns.

In the measurement of the duration $T_{CLK-TRAIL}$ of this state, the software distinguishes two cases:

- If the last bit in the clock lane HS-PAYLOAD is a ‘0’, then the CLK-TRAIL state is a differential-1 state.
  - The start of the state is defined at the time when the differential waveform crosses above the maximum differential input high threshold, V_{IDTH} (70 mV).
  - The end of the state is defined at the time when the differential waveform crosses below the maximum differential input high threshold, V_{IDTH} (70 mV).
- If the last bit in the clock lane HS-PAYLOAD is a ‘1’, then the CLK-TRAIL state is a differential-0 state.
  - The start of the state is defined at the time when the differential waveform crosses below the minimum differential input low threshold, V_{IDTL} (-70 mV).
  - The end of the state is defined at the time when the differential waveform crosses above the minimum differential input low threshold, V_{IDTL} (-70 mV for D-PHY 1.1; -40 mV for D-PHY≥ 1.2).

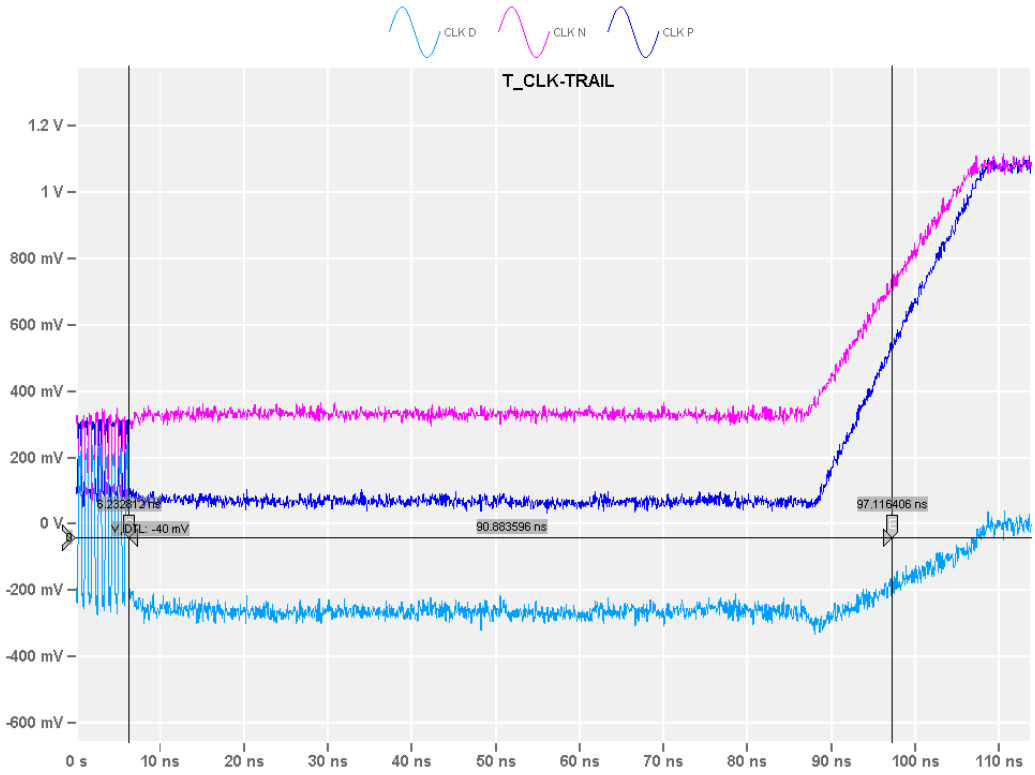


Figure 4-53: Typical result of a CLK-TRAIL state duration measurement

Clkp = Waveform of Clock+ (V_{DP})
Clkn = Waveform of Clock- (V_{DN})
Clkd = Differential waveform, V_{DP} - V_{DN}
T_CLK-TRAIL = Duration of the CLK-TRAIL state immediately after a clock lane HS transmission

This test case is tested for Z_{ID} = 100 ohms, only, and for all clock lanes.

4.6.3.14 Test 1.4.14 – Clock Lane HS Exit: 30%-85% Post-EoT Rise Time T_{REOT}

The purpose of this test case is to verify that the 30%-85% post-EoT rise time, T_{REOT} is not more than 35 ns.

To compute the 30%-85% Post-EoT Rise Time T_{REOT}, the software measures the rise time starting at the end of the CLK-TRAIL state, and ending at the time when the V_{DP} rising edge crosses above the minimum logic 1 input voltage, $V_{IH,MIN}$ (880 mV).

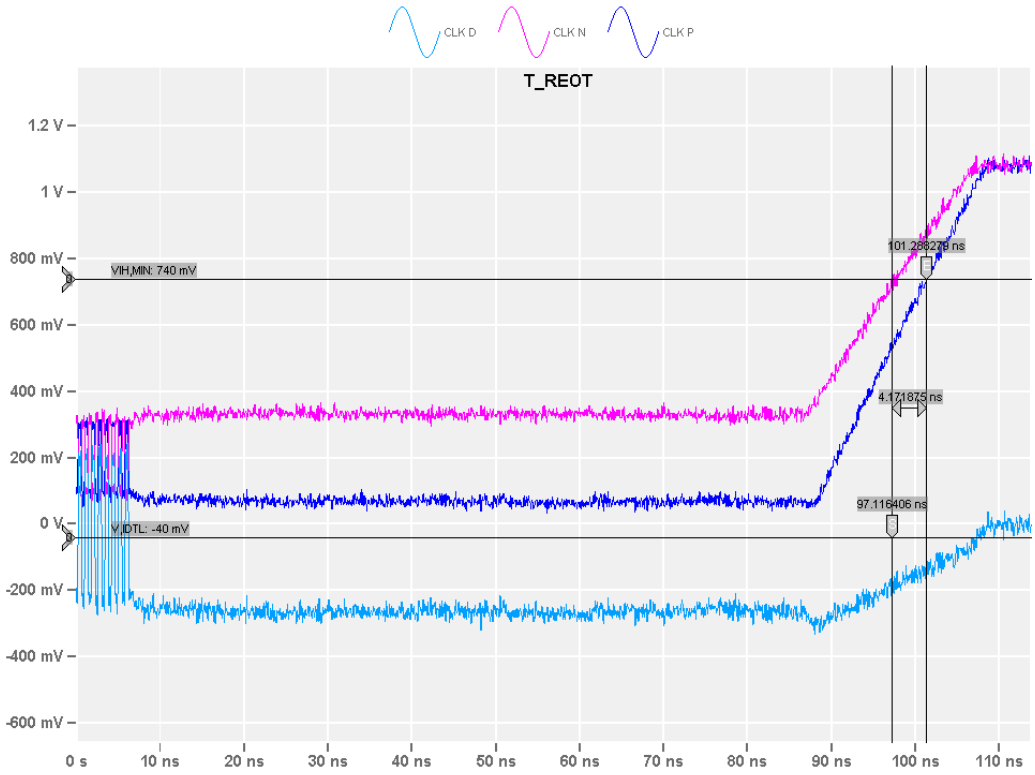


Figure 4-54: Typical result of a 30%-85% post-EoT rise time measurement

Clkp = Waveform of Clock+ (V_{DP})
Clkn = Waveform of Clock- (V_{DN})
Clkd = Differential waveform, V_{DP} - V_{DN}
T_REOT = Duration of the 30%-85% post-EoT rise time

This test case is tested for Z_{ID} = 100 ohms, only, and for all clock lanes.

4.6.3.15 Test 1.4.15 – Clock Lane HS Exit: T_{EOT} Value

The purpose of this test case is to verify that the combined value of $T_{CLK\text{-}TRAIL}$ and T_{REOT} is not more than (105 ns + 12·UI).

The software computes the combined value of $T_{CLK\text{-}TRAIL}$ and T_{REOT}, as obtained according to Chapter 4.6.3.13, "Test 1.4.13 – Clock Lane HS Exit: $T_{CLK\text{-}TRAIL}$ Value", on page 89 and Chapter 4.6.3.14, "Test 1.4.14 – Clock Lane HS Exit: 30%-85% Post-EoT Rise Time T_{REOT}", on page 90.

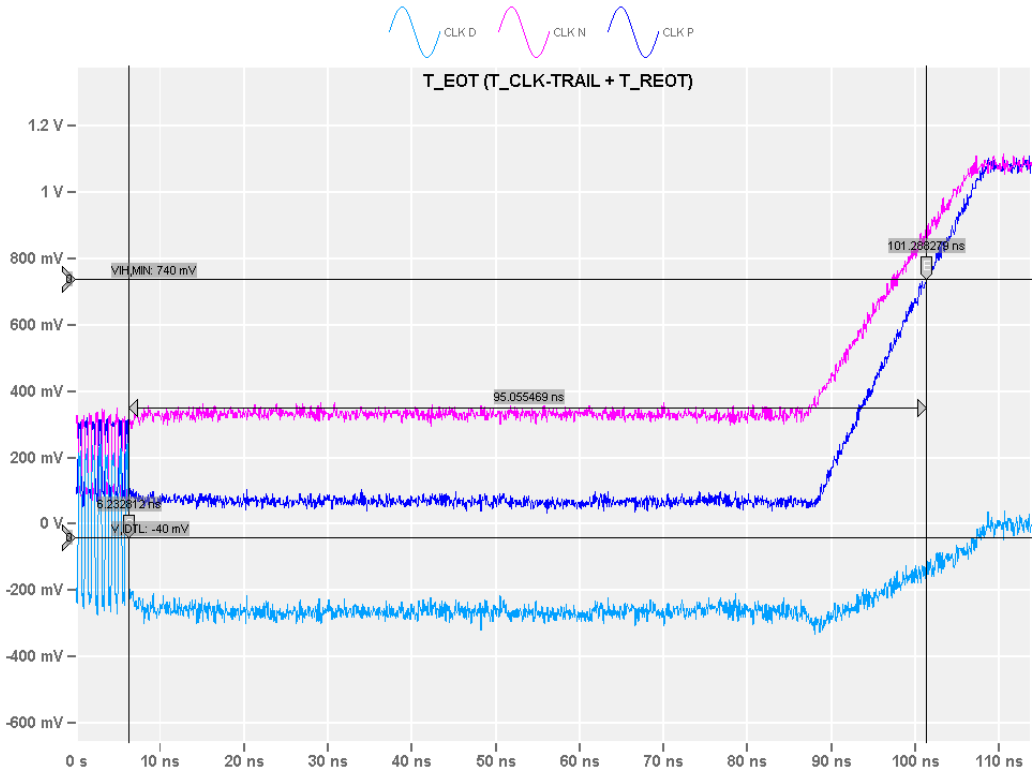


Figure 4-55: Typical result of a measurement of the combined value of T

Clkp = Waveform of Clock+ (V_{DP})
Clkn = Waveform of Clock- (V_{DN})
Clkd = Differential waveform, V_{DP} - V_{DN}
T_EOT = T_CLK-TRAIL + T_REOT

This test case is tested for Z_{ID} = 100 ohms, only, and for all clock lanes.

4.6.3.16 Test 1.4.16 – Clock Lane HS Exit: $T_{HS-EXIT}$ Value

The purpose of this test case is to verify that the duration of the LP-11 state, that occurs immediately after an HS transmission, is at least 100 ns.

The software measures $T_{HS-EXIT}$, the duration of the last LP-11 state that occurs immediately after an HS transmission, as follows:

The state is measured starting at the end of the CLK-TRAIL state, and ending at the time when the V_{DP} falling edge crosses below the maximum logic 0 input voltage, $V_{IL,MAX}$ (550 mV). For the end of the CLK-TRAIL state, two cases have to be distinguished:

- If CLK-TRAIL is a differential-1 state, the end of the state will be defined at the time when the differential waveform crosses below the minimum differential input low threshold, V_{IDTL} (-70 mV for D-PHY 1.1; -40 mV for D-PHY≥ 1.2).
- If CLK-TRAIL is a differential-0 state, the end of the state will be defined at the time when the differential waveform crosses above the maximum differential input high threshold, V_{IDTH} (70 mV for D-PHY 1.1; 40 mV for D-PHY≥ 1.2).

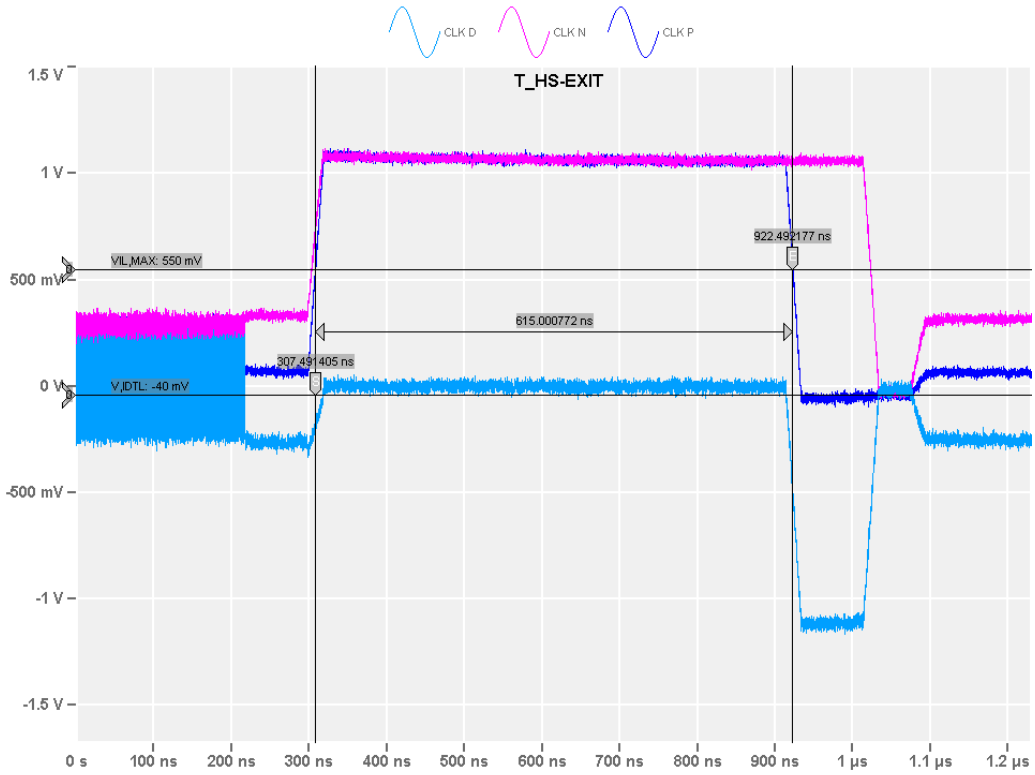


Figure 4-56: Typical result of a measurement of the duration of the LP-11 state immediately after an HS transmission

Clkp = Waveform of Clock+ (V_{DP})
Clkn = Waveform of Clock- (V_{DN})
T_HS-EXIT = duration of last LP-11 state after HS transmission

This test case is tested for Z_{ID} = 100 ohms, only, and for all clock lanes.

4.6.3.17 Test 1.4.17 – Clock Lane HS Clock Instantaneous: UI_{INST} Value

The purpose of this test is to verify that the instantaneous unit interval values, UI_{INST} of the DUT's high speed clock meet the following requirements:

- The calculated maximum UI_{INST} value is less than 12.5 ns
- The calculated minimum UI_{INST} value is greater than or equal to the specified $UI_{INST,MIN}$ value, as obtained from the vendor or from the datasheet

The software measures the instantaneous unit interval values, UI_{INST} as follows:

A sample (with at least 5000 UIs) of the DUT's HS clock signaling is captured.

The difference of the positive and negative single-ended clock lane waveforms (V_{DP}-V_{DN}) is computed, to acquire the differential clock lane waveform.

Based on the difference between successive 0 V crossing times of the differential clock lane waveform, the UI_{INST} are computed.

All acquired HS UIs are processed to determine their maximum, minimum and average values ($UI_{INST,MAX}$, $UI_{INST,MIN}$, and $UI_{INST,AVERAGE}$).

The computed $UI_{INST,MAX}$ must be less than 12.5 ns.

The computed $UI_{INST,AVERAGE}$ must not be less than the specified $UI_{INST,MIN}$ value, as obtained from the vendor or from the datasheet.

This test case is tested for Z_{ID} = 100 ohms, only, and for all clock lanes.

4.6.3.18 Test 1.4.18 – Clock Lane HS Clock Delta UI: (ΔUI) Value

This test case is tested for "Z_{ID}" = 100 Ω only and for all clock lanes.

The purpose of this test is to verify that the Δ UI (ΔUI) values of the DUT' high speed clock meet the following requirement:

- The peak ΔUI is between -5% and +5% of the unit interval (UI) duration at HS bit rates up to 1 Gbps.
- The peak ΔUI is between -10% and +10% of the unit interval (UI) duration at HS bit rates above 1 Gbps.

The software measures the ΔUI values as follows:

A sample of the DUT's HS clock signaling is captured.

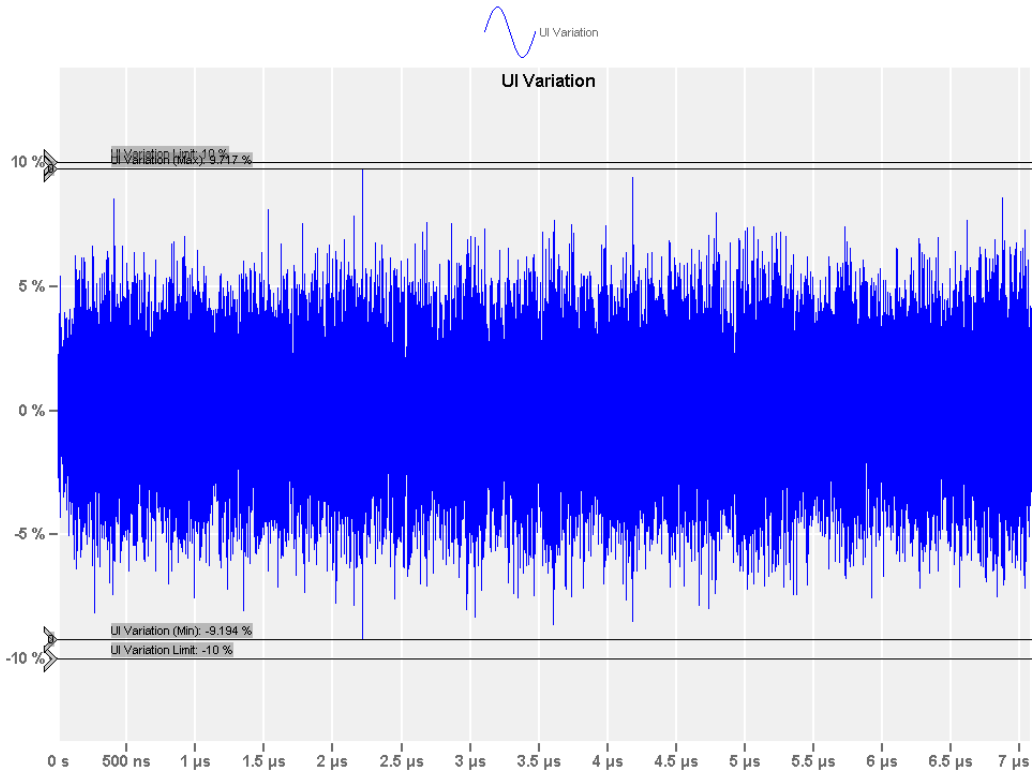
The difference of the positive and negative single-ended clock lane waveforms (V_{DP}-V_{DN}) is computed, to acquire the differential clock lane waveform.

The differences between successive 0 V crossing times of the differential clock lane waveform are measured as UI values.

The instantaneous bitrate of the clock transmitter is determined as the inverse value of the computed UI values. Additionally, a 2nd order Butterworth low pass filter with a cut-off frequency of 2.0 MHz is required to remove high frequency noise from the inverse UI values.

By using the inverse UI values as the input to the filter, the resulting output is converted to units of percent, to generate ΔUI values.

The peak maximum and peak minimum values are identified and compared with each other, to find the greater absolute value. This is reported as the final result of ΔUI.



4.6.3.19 Test 1.4.19 – TX Spread Spectrum Clocking (SSC)

The measurement is available for D-PHY 2.0, 2.1 and 2.5.

For best result, set the DUT to "Clock Type" = "Continuous" mode.

The purpose of this test is to verify that the the transmitter Spread Spectrum Clock (SSC) values (TSSC_MOD_RATE, TSSC_FREQ_DEV, SSCdf/dt) of the DUT HS Clock are within the conformance limits.

- SSC Modulation Rate must be within 30kHz and 33kHz
- SSC Deviation is within 0ppm and -5000ppm.
- SSC df/dt is less than 1250ppm/us.

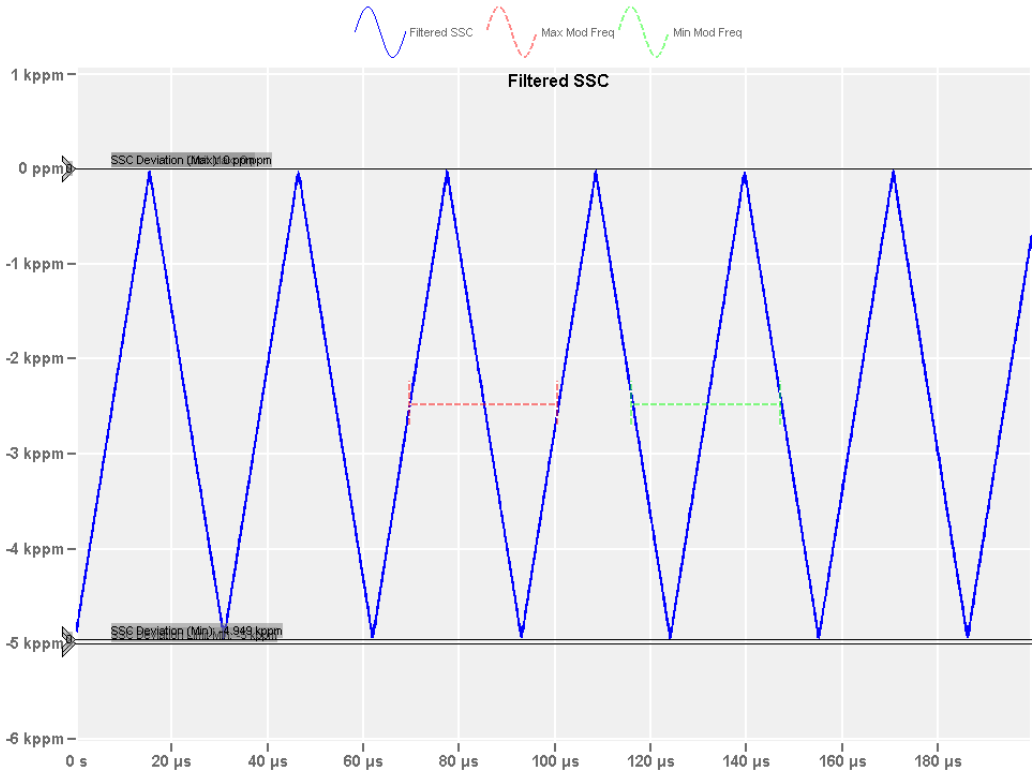
The software measures the SSC parameters as follows:

A sample of DUTs HS clock signaling is captured.

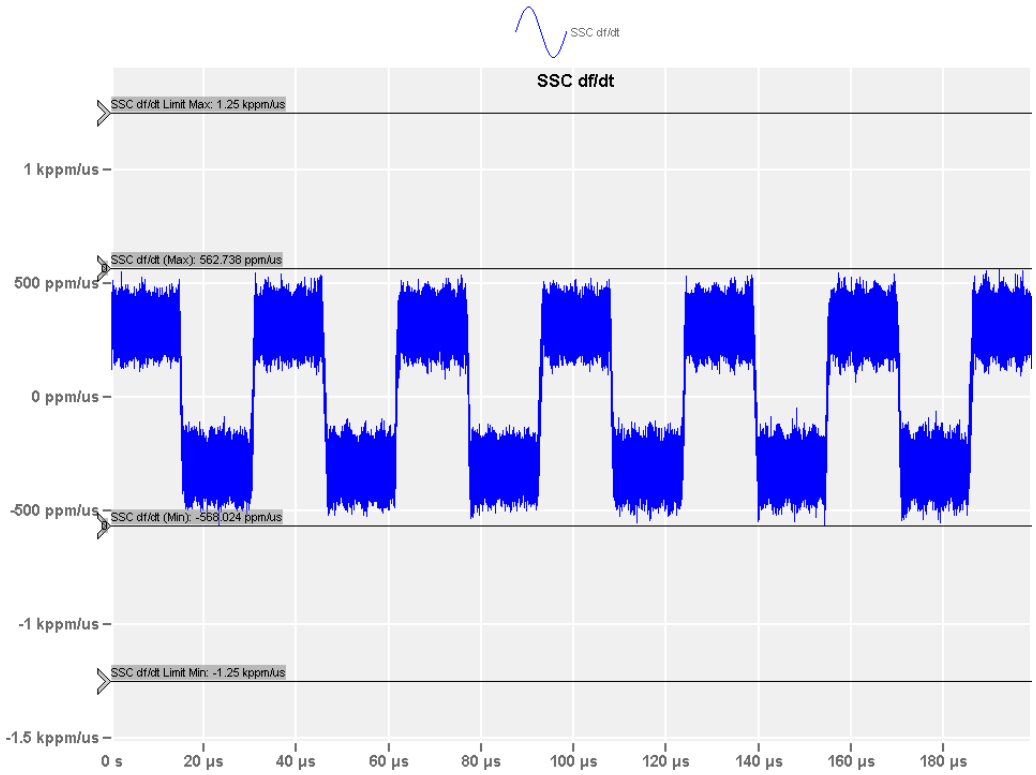
The difference of the positive and negative single-ended clock lane waveforms (V_{DP}-V_{DN}) is computed to acquire the differential Clock Lane waveform.

Difference between successive 0v crossing times of the differential Clock Lane waveform will be measured as UI values. Instantaneous frequency of the clock transmitter is measured as the inverse value of the UI values computed. A 0.222us average window filtering is applied in order to remove the high frequency noise.

The filtered clock frequency is used to analyze modulation rate and deviation as shown in the picture below:



To analyze the df/dt, slope of the filtered clock frequency is calculated for every 0.5us throughout the entire captured signal. The maximum and minimum df/dt must be less than 1250ppm/us to pass the test.



4.6.3.20 Test 1.4.20 – Clock Lane HS Clock Period Jitter

The measurement is available for D-PHY 2.0, 2.1 and 2.5.

The purpose of this test is to verify that period jitter, defined as peak-to-peak variation between successive rising edges of the differential clock, is within 10% of the average clock period.

The software measures the clock period jitter as follows:

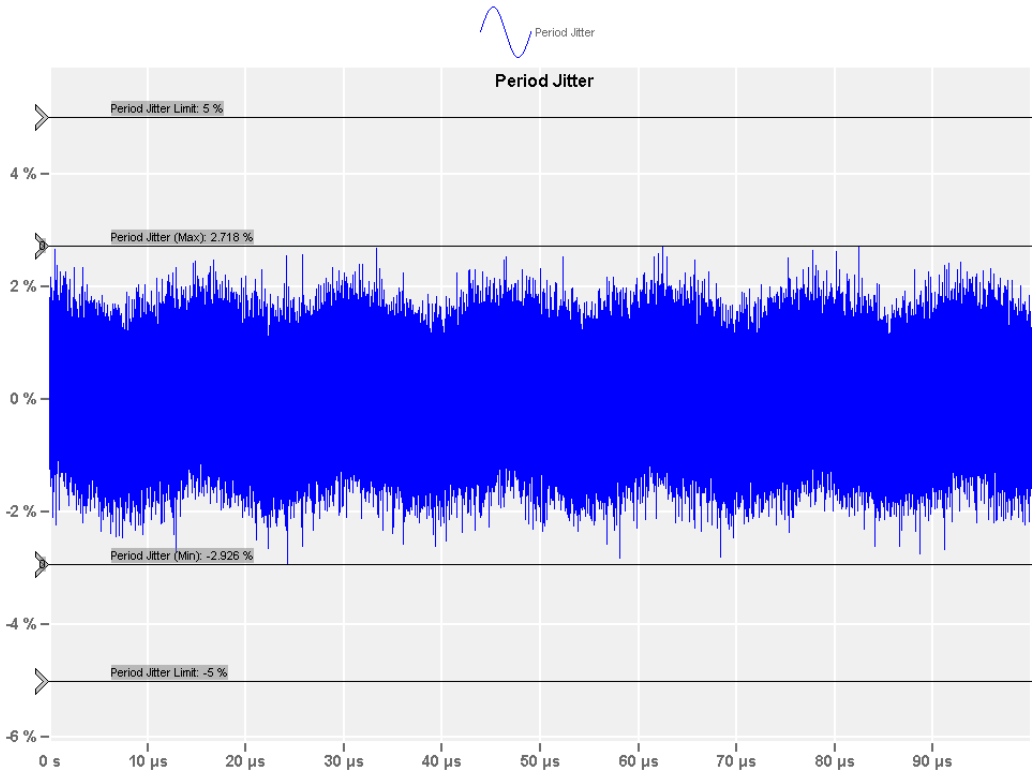
A sample of DUTs HS clock signaling will be captured.

The difference of the positive and negative single-ended clock lane waveforms (V_{DP}-V_{DN}) is computed to acquire the differential Clock Lane waveform.

Difference between successive 0v rising edge crossing times of the differential Clock Lane waveform is measured as clock period.

The variation in clock period is calculated by dividing the peak-to-peak variation by the averaged clock period.

The following picture shows the result of the measured period jitters.



4.7 HS-TX clock-to-data lane timing requirements (Group 5)

The purpose of Group 5 test cases is to verify the various requirements regarding clock lane to data lane timing.

Group 5 consists of four test cases, described in Chapter 4.7.3, "Measurements", on page 102. This group of test cases is only applicable to master devices.

The software is intended to facilitate the execution of a set of several HS-TX measurements on a set of captured HS burst waveforms. This version of the ScopeSuite MIPI D-PHY compliance test software only processes data burst waveforms (also known as non-continuous data waveforms). It does not support partial data burst (where HS Entry and HS Exit are captured separately) or continuous data. However, the software supports clock burst, partial clock burst, and continuous clock.

4.7.1 Test setup

Table 4-6: Equipment for Group 5 HS-TX Clock-to-Data Lane Timing Requirements test

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 / RTP with 4 channels and at least 4 GHz bandwidth	1
Probes	Differential probes: at least 4 GHz bandwidth, or Single-ended probes: at least 4 GHz bandwidth	3/4 (*)
Test fixture	UNH-IOL MIPI D-PHY Reference Termination Board (RTB)[1]	1
DUT	Any MIPI D-PHY CSI-2 or DSI device	1
* In this group of tests, sampling the clock signal requires either 2 single-ended probes or 1 differential probe. Sampling the data signal requires 2 probes: either single-ended, or differential used in single-ended mode. Hence, in total, either 4 single-ended probes or 3 differential probes or combinations thereof are required. [1] Minimum bandwidth of 6 GHz is required to run D-PHY 2.0, 2.1 and 2.5 tests.		
[1] We recommend to use a MIPI D-PHY Reference Termination Board (RTB) test fixture from the University of New Hampshire InterOperability Laboratory (UNH-IOL). Refer to https://www.iol.unh.edu/services/testing/mipi/fixtures.php for details.		

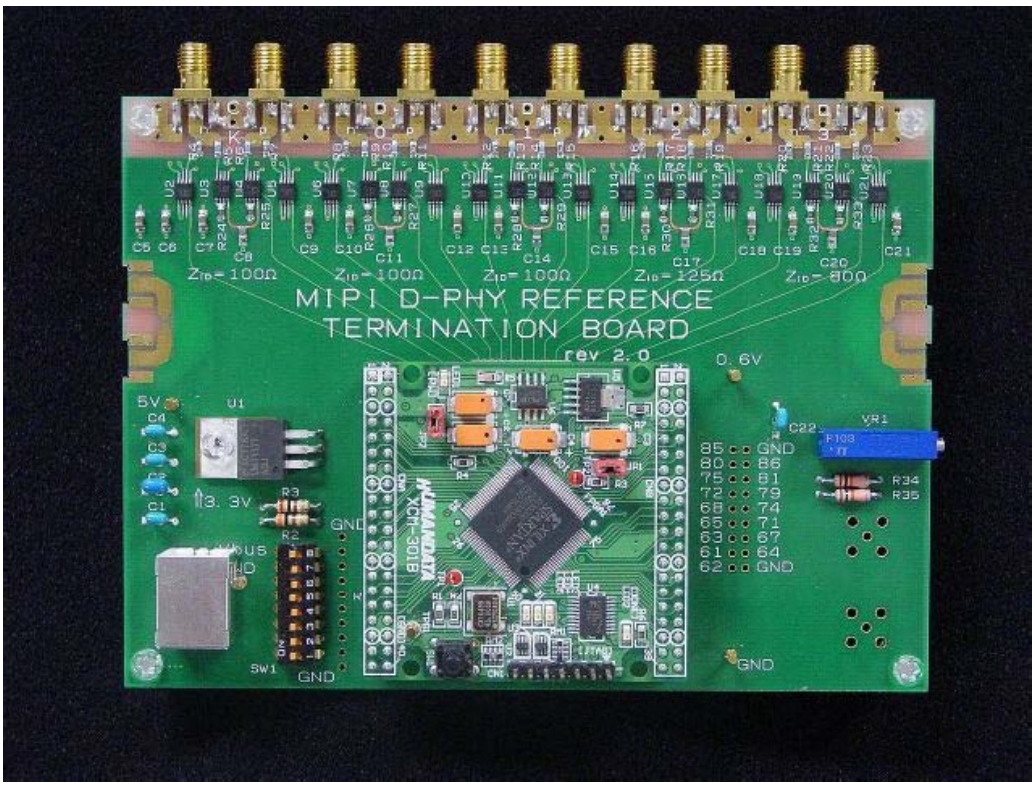


Figure 4-57: MIPI D-PHY Reference Termination Board test fixture from UNH-IOL

Waveform requirements

Group 5 test cases require the DUT to transmit HS clock burst waveforms, as shown in Figure 4-58, consisting of:

- (a) LP-11 (HS Entry)
- (b) LP-01
- (c) LP-00
- (d) HS-ZERO
- (e) HS-SYNC
- (f) HS-PAYLOAD
- (g) HS-TRAIL
- (h) LP-11 (HS Exit)

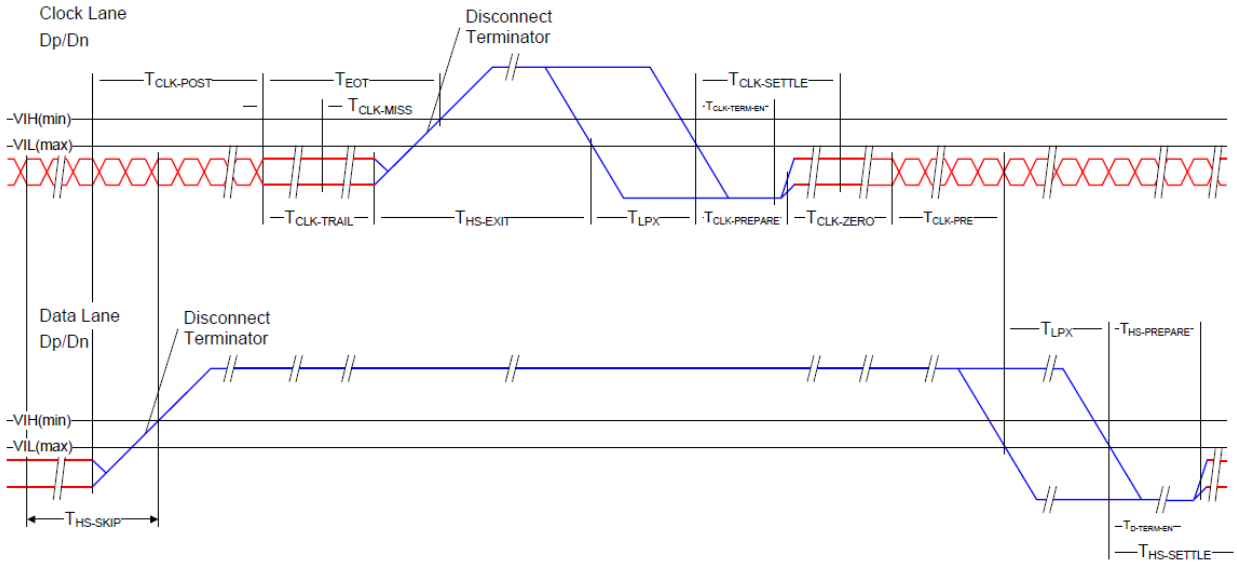


Figure 4-58: A typical MIPI D-PHY HS clock burst waveform (courtesy of MIPI Alliance Specification for D-PHY version 1.1)

The software requires at least one set of complete data burst waveforms for correct processing, to perform the test successfully.

If the clock is set to normal burst mode, the software also requires at least one set of complete clock burst waveforms.

Settings in the " Configuration" dialog box

See also: Chapter 4.2, "Test configuration for D-PHY", on page 20.

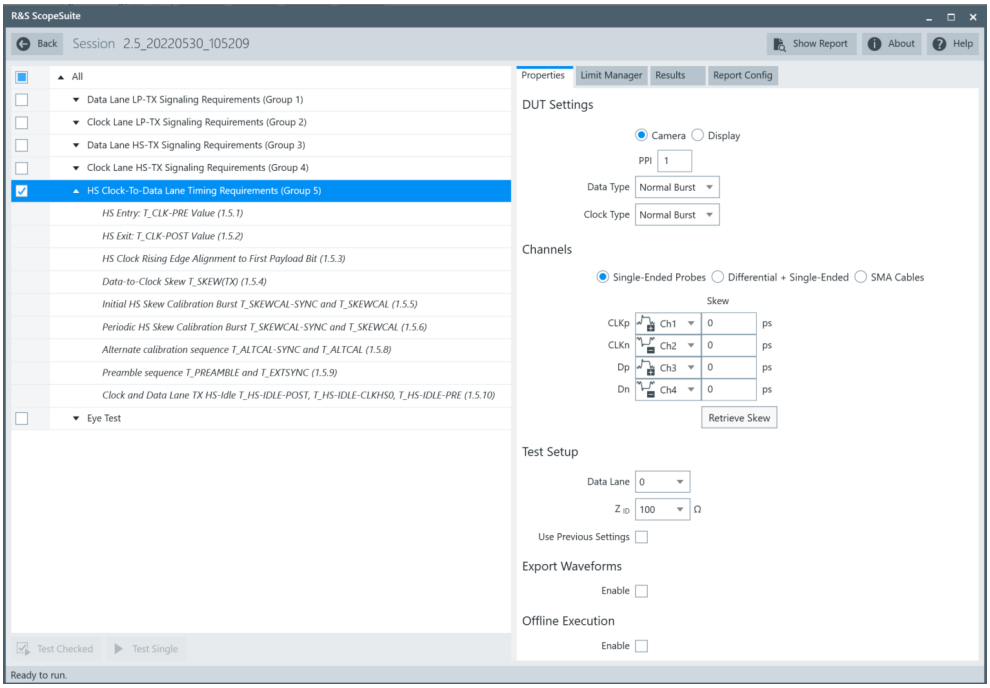
- **DUT Settings**
  Select if the DUT is a "Camera" or a "Display".
  You can also set the "Clock type" according to your device.
- **Channels**
  This setting depends on the probes that are used to capture the clock signals .
  Select the channels for the measurement and set or retrieve the skew.
- **Data Lane**

If the DUT implements multiple data lanes, select which pair of data lanes is to be tested.

- **Z_{ID}**
  Each lane of the RTB board has a specific termination value. According to your test requirements, connect your DUTs to the lane with the corresponding Z_{ID} value.
  For more information about the RTB board, refer to its datasheet.
  Group 5 is performed using the Z_{ID} = 100 ohms termination case, only, and is measured for all data lanes. So the pair of data lanes under test (dat_p and dat_n) and the pair of clock lanes (clk_p and clk_n) have to be terminated with the 100 ohms loads on the RTB. This can be done on the Clock, Data0 or Data1 lanes of the RTB board.

4.7.2 Performing Group 5 test cases

1. Start running the tests as described in Chapter 4.1, "Starting D-PHY compliance tests", on page 20.
2. Select "HS Clock-To-Data Lane Timing Requirements (Group 5)".



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
   This group of tests uses the MIPI D-PHY Reference Termination Board (RTB) test fixture from the UNH-IOL.
   The clock signals can be tapped either from the DUT or RTB, or even on the SMA cables between the DUT and the RTB.

The connections may differ slightly depending on the clock format and the terminations which are applied to the DUT.
When you have finished all steps, the compliance test runs automatically.

Further steps:

- Chapter 3.3, "Getting test results", on page 16

4.7.3 Measurements

4.7.3.1 Test 1.5.1 – HS Entry: $T_{CLK-PRE}$ value

The purpose of this test case is to verify that the time $T_{CLK-PRE}$, during which the high speed clock is driven prior to an associated data lane that begins the transition from low power to high speed mode, is greater than the minimum required value (8·UI).

The state is measured

- beginning at the end of the clock lane $T_{CLK-ZERO}$ interval (at the point where the clock lane differential waveform crosses below the minimum valid HS-RX differential threshold level of ±70 mV), and
- ending at the point where the data lane's V_{DP} LP-01 falling edge crosses $V_{IL,MAX}$ (550 mV).

An example is shown in Figure 4-59 that represents a "PASS" result: $T_{CLK-PRE}$ = 242.9 ns, which is much greater than the minimum required value of 8·UI = 11.2 ns (with UI = 1.4 ns).

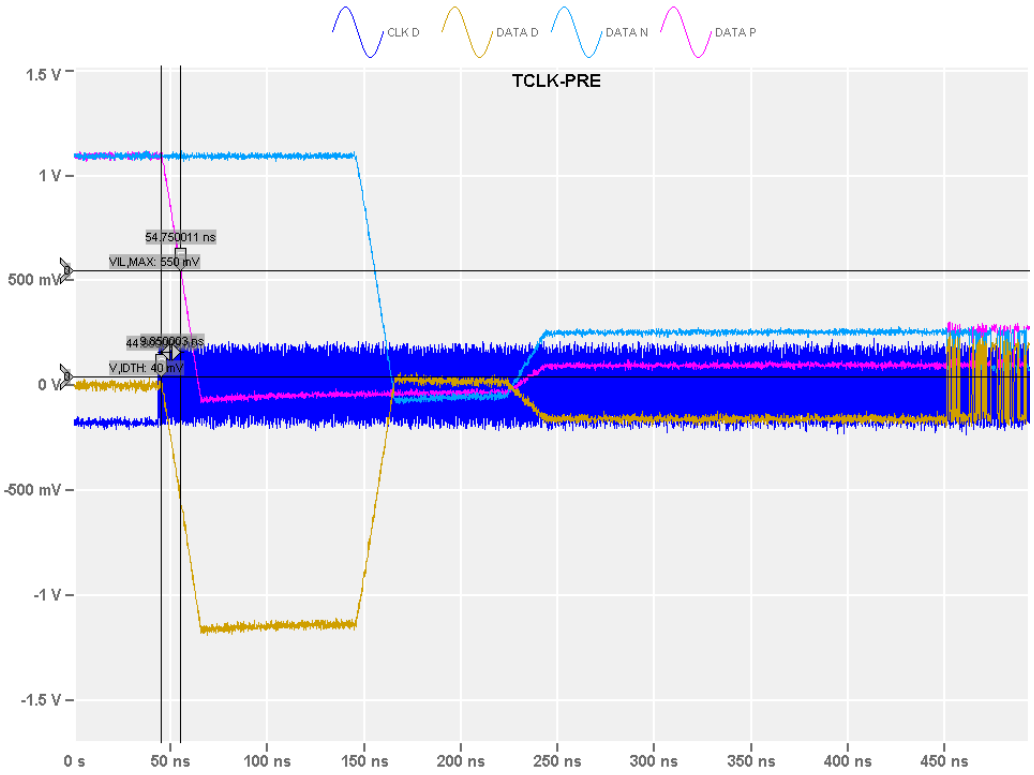


Figure 4-59: Typical result of a measurement of the duration T_CLK-PRE

CLK D = Waveform of Clock+ (V_{DP})
DATA P = Waveform of Data+ (V_{DP})
DATA N = Waveform of Data- (V_{DN})
DATA D = Differential waveform, V_{DP} - V_{DN}
T_CLK-PRE = Duration of HS clock signaling prior to a data lane transition from LP to HS mode

4.7.3.2 Test 1.5.2 – HS Exit: $T_{CLK-POST}$ value

The purpose of this test case is to verify that the DUT's clock lane high speed transmitter continues to transmit clock signaling for the minimum required duration ($T_{CLK-POST}$) after the last data lane switches from high speed to low power mode. $T_{CLK-POST}$ is required to last no shorter than 60 ns + 52·UI.

The state is measured:

- Beginning at the end of the data lane $T_{HS-TRAIL}$ period, and
- Ending at the start of the clock lane $T_{CLK-TRAIL}$ period.

An example is shown in Figure 4-60 that represents a "PASS" result: $T_{CLK-POST}$ = 180.5 ns, which is greater than the minimum required value of 60 ns + 52·UI = 132.8 ns (with UI = 1.4 ns).

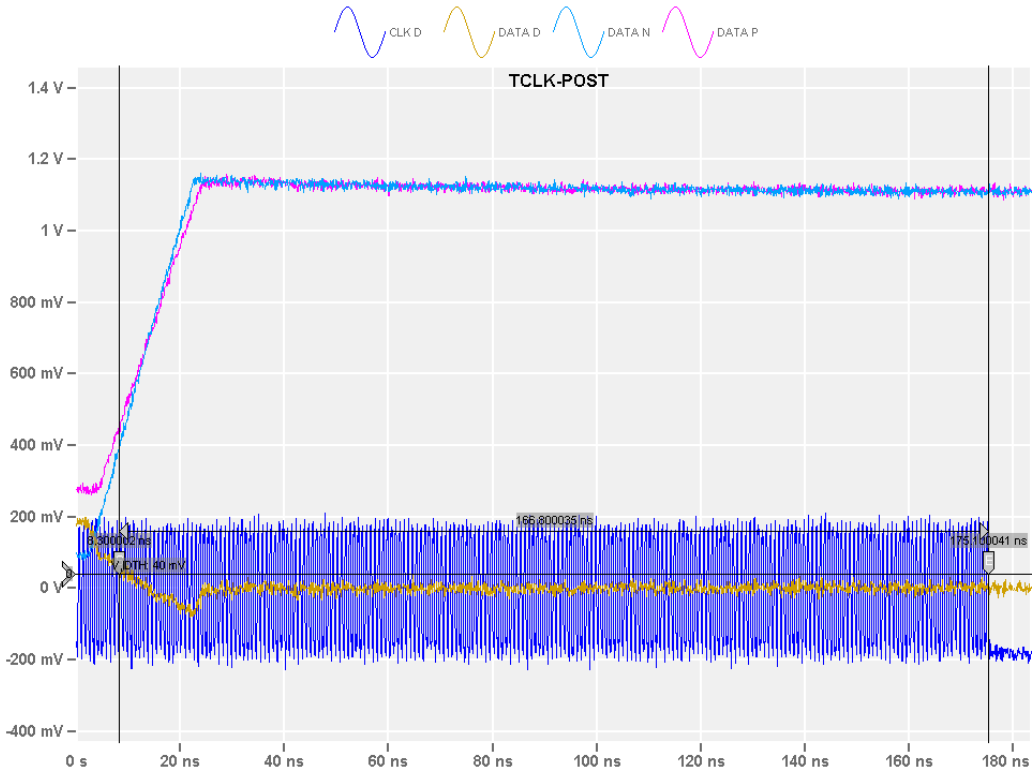


Figure 4-60: Typical result of a measurement of the duration T_CLK-POST

CLK D = Waveform of Clock+ (V_{DP})
DATA P = Waveform of Data+ (V_{DP})
DATA N = Waveform of Data- (V_{DN})
DATA D = Differential waveform, V_{DP} - V_{DN}
T_CLK-POST = Duration of HS clock signaling after the last data lane switches from LP to HS mode

4.7.3.3 Test 1.5.3 – HS Clock Rising Edge Alignment to First Payload Bit

The purpose of this test case is to verify that the DUT's high speed clock is properly aligned to the payload data signaling. The first payload bit of the burst data should align with a rising edge of the DDR clock.

The software checks if the first payload bit of burst data (i.e., the first bit after the Sync byte) aligns with a rising edge of the DDR clock. A "PASS" result is shown in Figure 4-61.

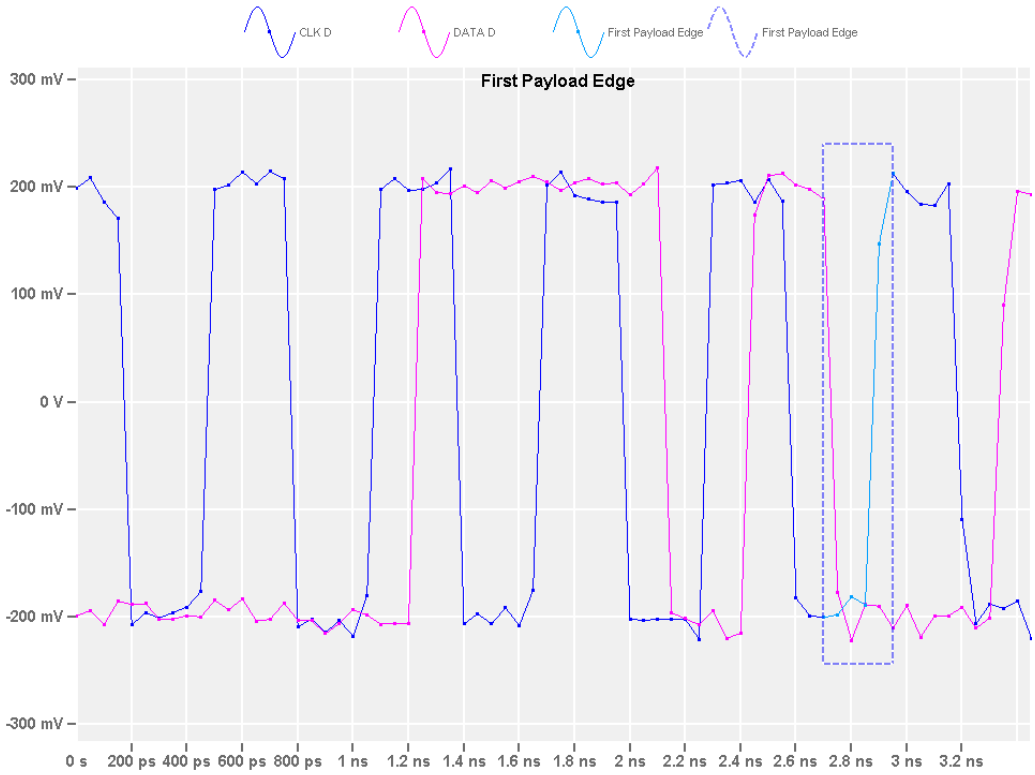


Figure 4-61: Testing the alignment of the first data bit with a rising edge of the clock

CLK D = Waveform of Clock+ (V_{DP})
DATA D = Differential waveform, V_{DP} - V_{DN}

4.7.3.4 Test 1.5.4 – Data-to-Clock Skew ($T_{SKEW[TX]}$)

The purpose of this test case is to verify that the skew between the clock and data signaling, as measured at the transmitter ($T_{SKEW[TX]}$), is within the conformance limits of 15% of the unit interval (UI) duration.

$T_{SKEW[TX]}$ is the permissible deviation of the data launch time to the ideal ½·UI_{INST} displaced quadrature clock edge.

The software measures the timing error $T_{SKEW[TX]}$ between each data lane edge and its corresponding clock lane edge in a minimum sample of 10,000 events, to produce an array of timing error values. The maximum, minimum, and mean timing error values across all observed edges are recorded.

The example in Figure 4-62 shows how the software presents $T_{SKEW[TX]}$ in a report.

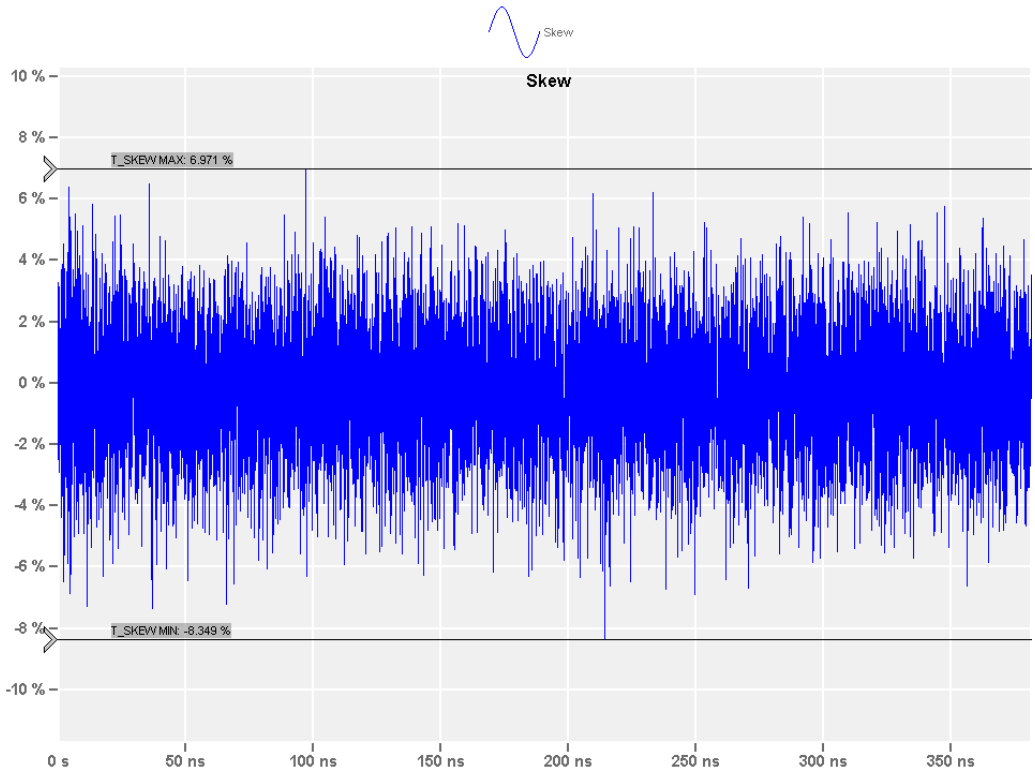


Figure 4-62: Evaluation of the relative skew between clock and data signaling

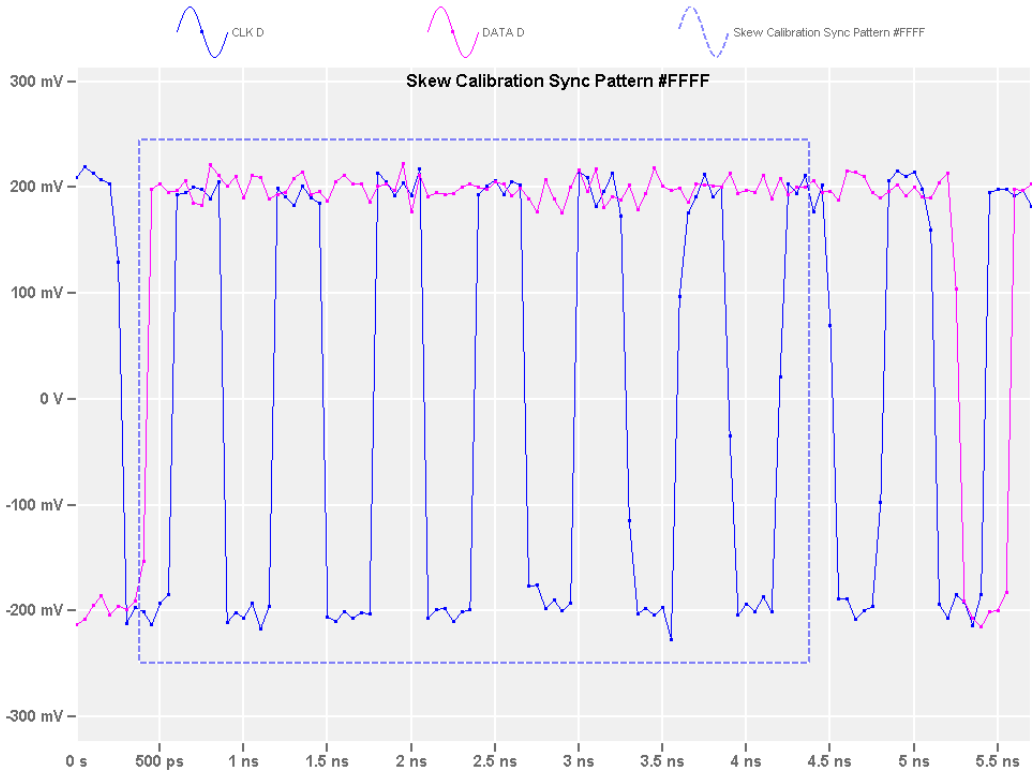
4.7.3.5 Test 1.5.5 – Initial HS Skew Calibration Burst $T_{SKEWCAL-SYNC}$ and $T_{SKEWCAL}$

The measurement is available for D-PHY version 1.2 and higher.

The purpose of this test case is to verify that the DUT transmits a validly formed initial HS skew calibration burst.

It measures the duration of the deskew sync pattern (0xFFFF, $T_{SKEWCAL-SYNC}$) and the duration of the burst payload ($T_{SKEWCAL}$).

For all data lanes the $T_{SKEWCAL-SYNC}$ should be in the range of 16 ±0.25 UI and $T_{SKEWCAL}$ should be at least 32768 (2^{15}) UI. The values are reported in terms of UI, where UI is the mean UI value for the burst.



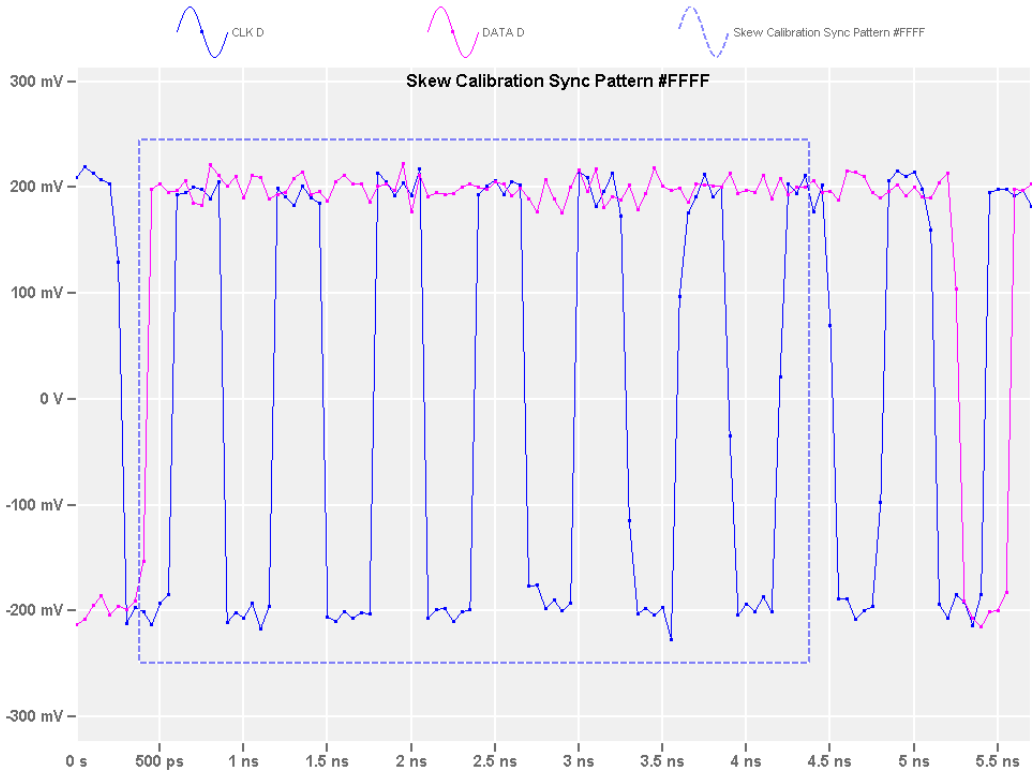
4.7.3.6 Test 1.5.6 – Periodic HS Skew Calibration Burst $T_{SKEWCAL-SYNC}$ and $T_{SKEWCAL}$

The measurement is available for D-PHY version 1.2 and higher.

The purpose of this test case is to verify that the DUT transmits a validly formed periodic HS skew calibration burst.

It measures the duration of the deskew sync pattern (0xFFFF, $T_{SKEWCAL-SYNC}$) and the duration of the burst payload ($T_{SKEWCAL}$).

For all data lanes the $T_{SKEWCAL-SYNC}$ should be in the range of 16 ±0.25 UI and $T_{SKEWCAL}$ should be at least 4096 (2^{12}) UI. The values are reported in terms of UI, where UI is the mean UI value for the burst.



4.7.3.7 Test 1.5.8 Alternate calibration sequence T_ALTCAL-SYNC and T_ALTCAL

The purpose of this test is to verify that the DUT transmits a valid Alternate Calibration Sequence.

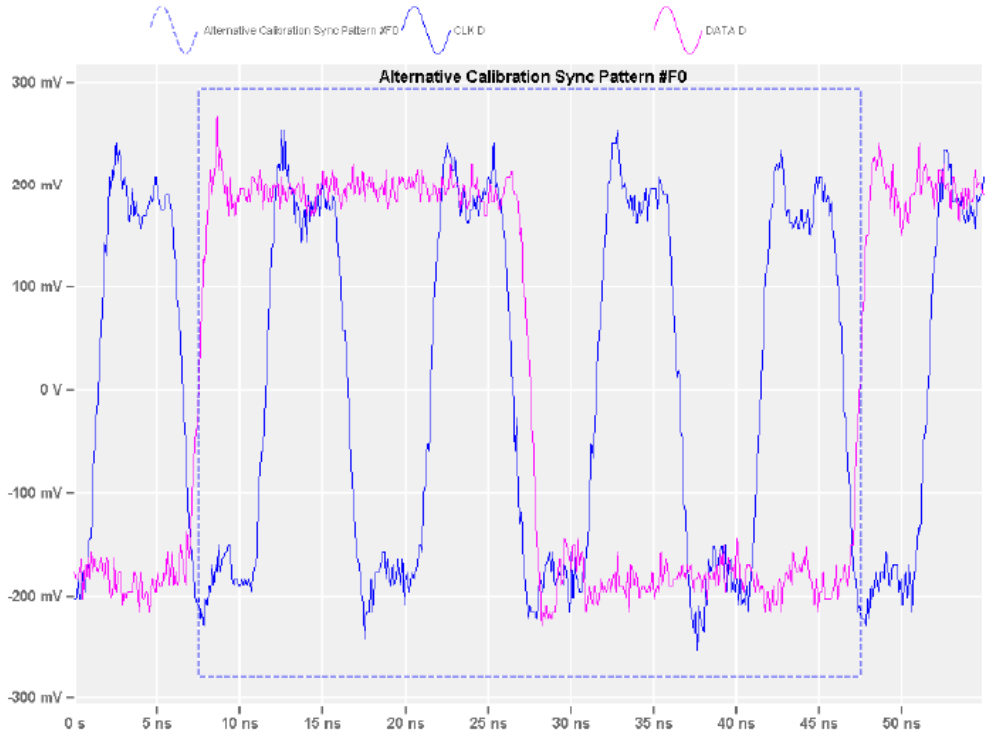
The following criteria must be met in order to pass the test:

- $T_{ALTCAL-SYNC}$ must contain 0xF0 pattern.
- T_{ALTCAL} is within the range from 32768 UI to 100 µs.

The software analyzes the HS Burst captured.

If no HS-SYNC is detected, this HS Burst will try to search for alternate calibration sequence which consists of ALTCAL-SYNC and ATLCAL. If HS-SYNC found the timing parameters related to alternate calibration are measured and reported.

The following picture shows found alternate calibration sync.



4.7.3.8 Test 1.5.9 Preamble sequence T_PREAMBLE and T_EXTSYNC

The purpose of this test is to verify that the DUT transmits a valid formed preamble sequence.

The following criteria must be met in order to pass the test:

- $T_{EXTSYNC}$ is within the range of 8 +/- 0.25 UI
- $T_{PREAMBLE}$ is according to the programmed value (32, 64, 512 UI)

The software analyzes the HS Burst captured.

If no HS-SYNC is detected, this HS Burst will try to search for Preamble sequence and if found the timing parameters will be measured and reported.

The following pictures show found preamble sequence:

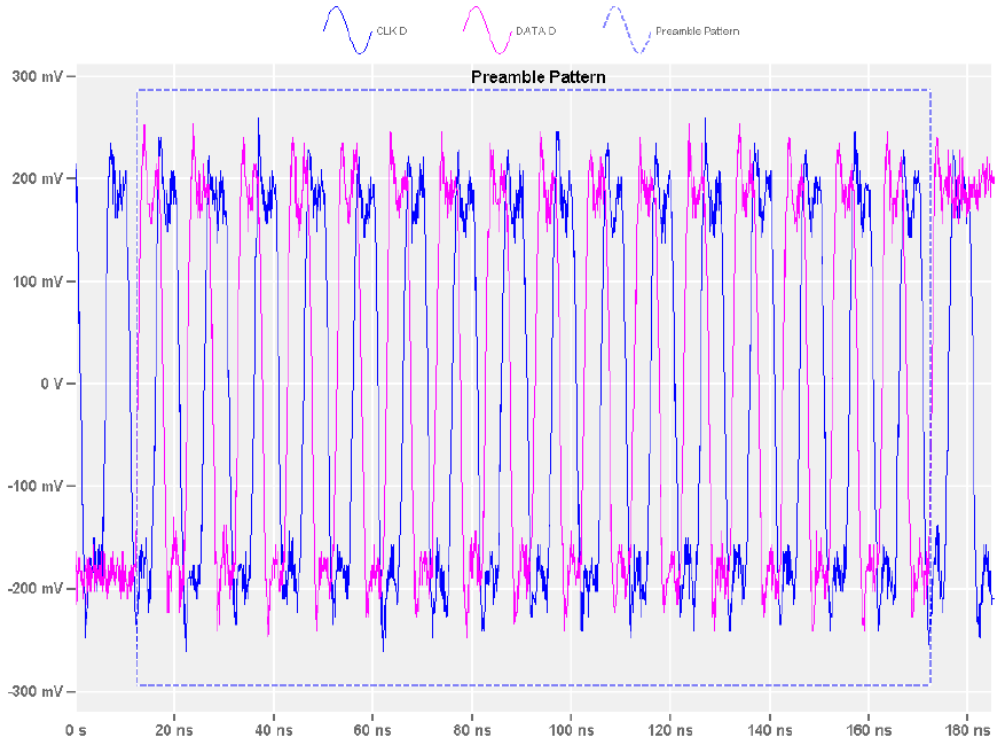


Figure 4-63: Preamble

Figure 4-64: Extended sync pattern

4.7.3.9 Test 1.5.10 Clock and Data Lane TX HS-Idlw T_HS-IDLE-POST, T_HS-IDLE-CLKHS0, T_HS-IDLE-PRE

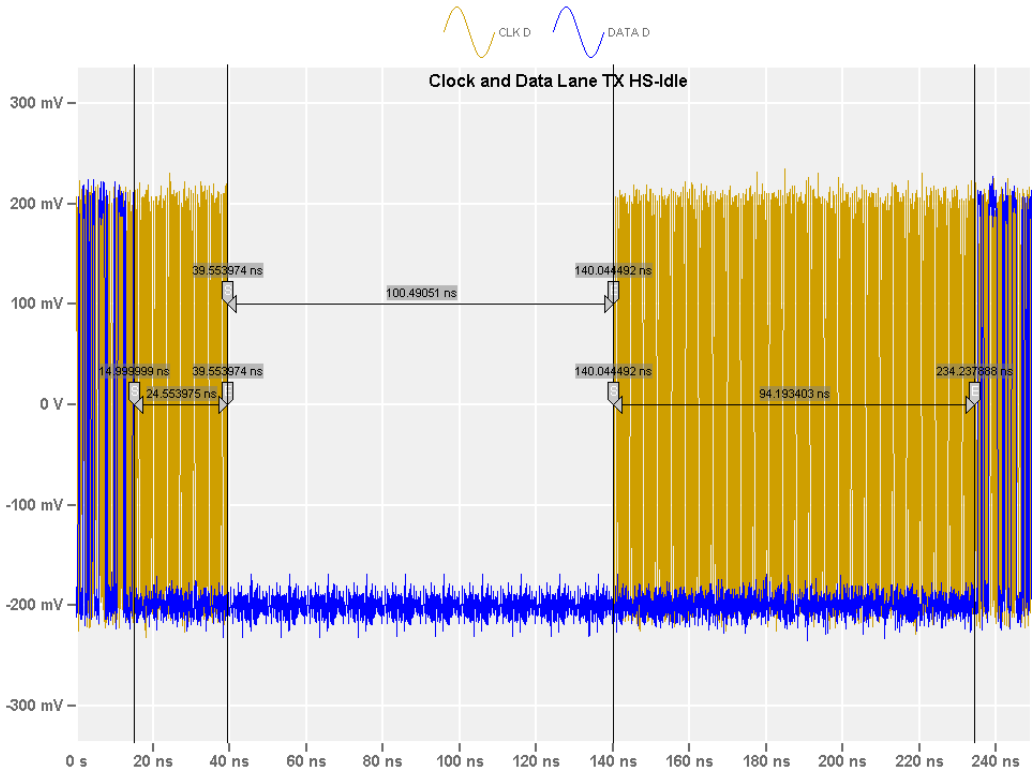
The purpose of this test is to verify that the DUT transmits a valid HS-Idle state.

The following criteria must be met in order for the test to pass:

- $T_{HS\text{-}IDLE\text{-}POST}$ must be within n*8 UI and 512 UI
- $T_{HS\text{-}IDLE\text{-}CLKHS0}$ must be within 60ns and 500ns
- $T_{HS\text{-}IDLE\text{-}PRE+THS\text{-}ZERO}$ must be greater than 4 UI + 60ns + n*8 UI

The software attempts to find HS-IDLE state by looking for HS-SYNC after a long idle state in data lane. If it is found, measurements will be performed.

An example of such measurement is shown in the figure below.



4.8 Eye test

The purpose of Eye Test cases is to verify the requirements regarding clock lane to data lane timing using eye diagram.

The software support various kind of clock and data signal types. The signal type affects number of measurements can be executed. Refer to each individual measurement for the details.

4.8.1 Test setup

Table 4-7: Equipment for Eye Test

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 / RTP with 4 channels and at least 4 GHz bandwidth[1]	1
Probes	Differential probes: R&S RT-ZM	2
Test fixture	UNH-IOL MIPI D-PHY Reference Termination Board (RTB)[2]	1
DUT	Any MIPI D-PHY CSI-2 or DSI device	1

Item	Description, model	Quantity
[1] Minimum bandwidth of 6 GHz is required to run D-PHY 2.0, 2.1 and 2.5 tests.		
[2] We recommend to use a MIPI D-PHY Reference Termination Board (RTB) test fixture from the University of New Hampshire InterOperability Laboratory (UNH-IOL). Refer to https://www.iol.unh.edu/solutions/test-tools/mipi for details.		

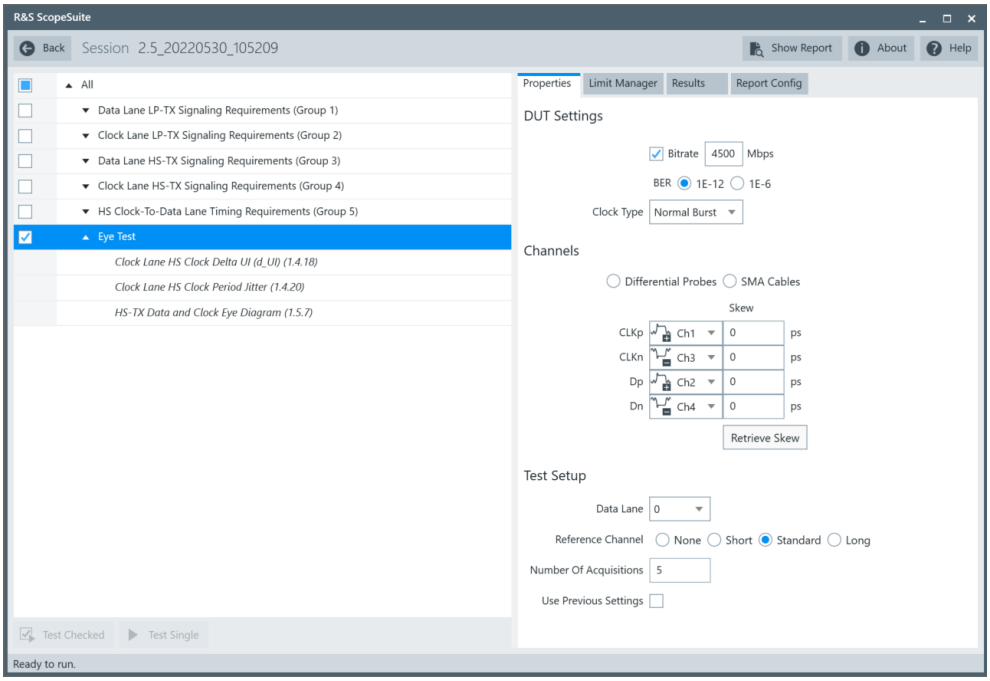
Settings in the " Configuration" dialog box

See also: Chapter 4.2, "Test configuration for D-PHY", on page 20.

- **DUT Settings**
  You can set the "Clock type" according to your device.
- **Channels**
  This setting depends on the probes that are used to capture the clock signals .
  Select the channels for the measurement and set or retrieve the skew.
- **Data Lane**
  If the DUT implements multiple data lanes, select which pair of data lanes is to be tested.
- **Test Setup**
  For the " Reference Channel", select the "Short", "Standard" or "Long" for setting.
  The software the emulate the reference channel when performing HS-TX Data and Clock Eye Diagram. Select "None" if reference channel is present physically.
  Sets the "Number of Acquisitions ": number of UI to construct the eye diagrams.
  Note that a greater value of the setting will require more processing time.

4.8.2 Performing Eye test cases

1. Start the test as described in Chapter 4.1, "Starting D-PHY compliance tests", on page 20.
2. Select the test case group: "Eye test".



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.

Further steps:

- Chapter 3.3, "Getting test results", on page 16

4.8.3 Measurements

4.8.3.1 Test 1.4.18 Clock Lane HS Delta UI (d_UI)

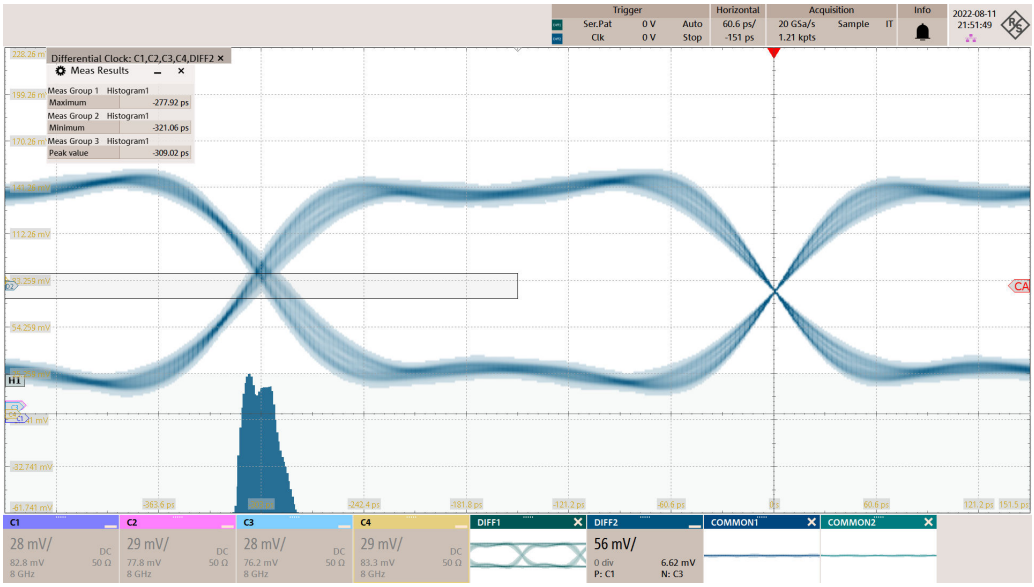
This test applies for "Clock type" = "Continuous".

The purpose of this test is to verify that the ΔUI of the DUT HS Clock meets the following requirements:

- The peak ΔUI is between –5% and +5% at HS bit rate up to 1 Gbps.
- The peak ΔUI is between –10% and +10% at HS bit rate up more than 1 Gbps.

In this test the software will acquire the clock signal and construct clock eye diagram using the both rising and falling edges of the clock signal. Once desired number of UI (set via Number Of Acquisitions) have been achieved, the software will measure peak-to-peak value of left side UI's 0V crossing points using histogram. The measured peak-to-peak value is converted to UI and reported as percentage of the nominal UI.

The following figure shows a Clock Delta UI measurement.



4.8.3.2 Test 1.4.20 Clock Lane HS Clock Period Jitter

This test applies for "Clock type" = "Normal burst"/ "HS Entry and Exit".

The purpose of this test is to verify that the clock period jitter, the peak-to-peak variation between successive rising edges of the differential clock, is within 10% of the average clock period.

In this test the software acquires the clock signal and construct clock eye diagram using only rising edges of the clock signal. Once desired number of UI have been achieved, the software will measure peak-to-peak value of rising edges' 0V crossing points using histogram. The measured peak-to-peak value is converted to Clock period and reported as percentage of the nominal Clock period.

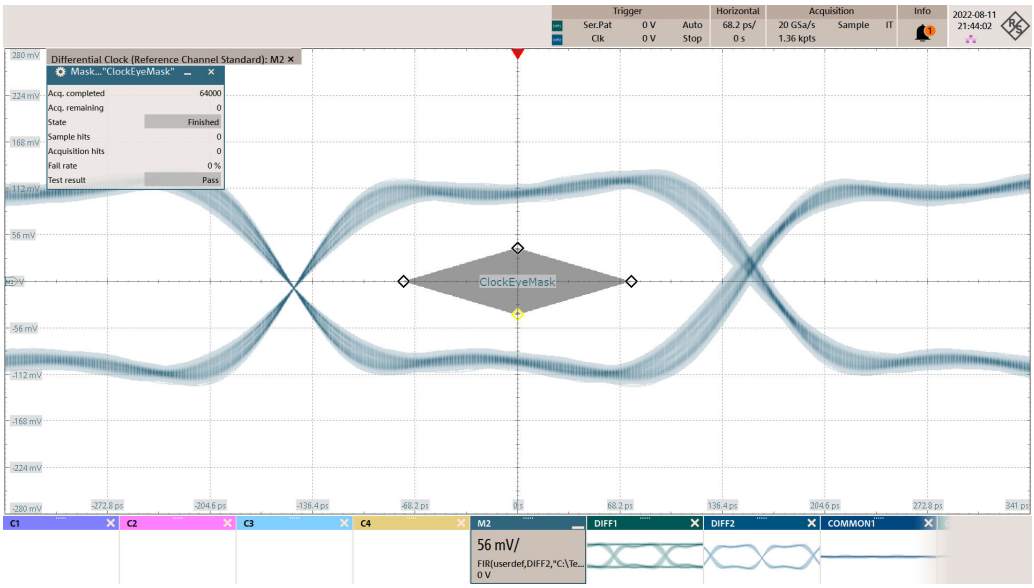
The following figure shows a Clock Period Jitter measurement.

4.8.3.3 Test 1.5.7 HS/TX Data and Clock Eye Diagram

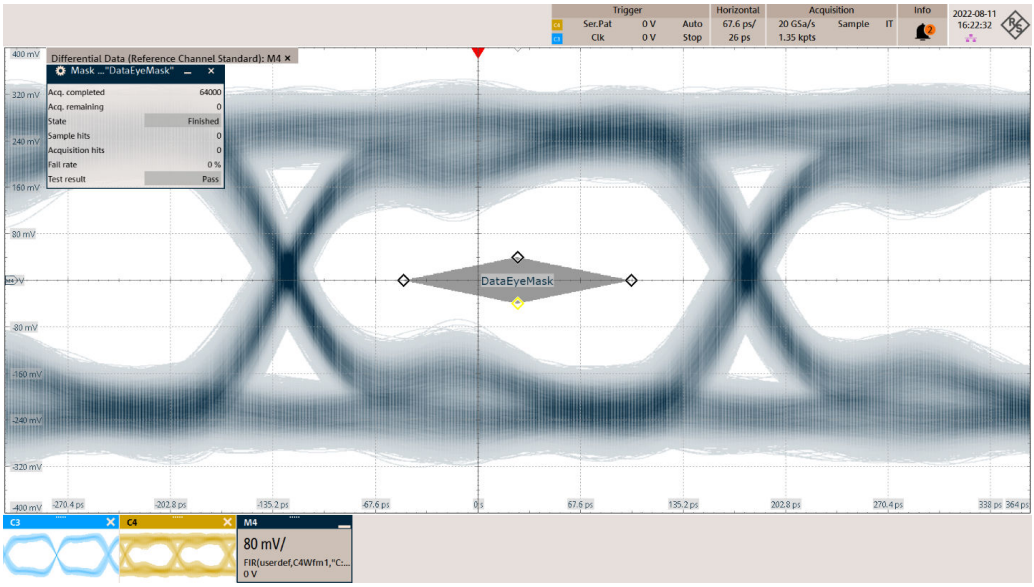
This test applies for "Clock type" = "Continuous".

The purpose of this test is to verify that the DUT's HS-TX meets the requirements for Transmitter Eye Diagram specification defined by T_{EYE_TX} and V_{DIF_TX}. This test is applicable for operating data rates > 1.5Gbps and ≤ 4.5Gbps

The following picture shows a clock eye mask test with Standard Reference Channel:



The following picture shows a data eye mask test with Standard Reference Channel:


Trigger
Horizontal
Acquisition
Info
Ser.Pat 0 V Auto 67.6 ps/ 20 GSa/s Sample IT
Clk 0 V Stop 26 ps 1.35 kpts
2022-08-11
16:22:32
Differential Data (Reference Channel Standard): M4
Mask ... "DataEyeMask"
Acq. completed 64000
Acq. remaining 0
State Finished
Sample hits 0
Acquisition hits 0
Fail rate 0 %
Test result Pass
DataEyeMask
C3
C4
M4
80 mV/
FIR(userdef,C4Wfm1,"C...
0 V